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Real Time Minimum Energy Tracking Techniquies for Digital Load Circuit

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Abstract: ***Minimization of energy consumption is an important constraint in portable electronic devices such as smart phones or tablet PCs, laptops . With reliable energy measurement and estimation methods and tools, it is possible to accurate prediction of minimum energy consumption at different levels i.e., from circuit to architecture, architecture to system software and system software to application. Energy efficient design requires reducing energy dissipation in all stages of the design process without compromising the system performance and the quality of services..***

Index Terms:, Energy efficient, Minimum energy Measurement, System performance..

I. INTRODUCTION

In modern digital integrated circuit design, one of the primary focuses of research is on energy efficient system. Energy efficient[1][10] is boardly defined as completing an application's workload at the lowest possible energy. The application are broken up into two general categories based on performance, high end application are:- servers, desktop computers and laptop computers. Low- end application:- portable media player[3], smart phone, tablets and bio-medical devices.The advance in technology is used to reduce energy consumption at different levels of abstraction by energy reduction techniques in the design flow, and the performance can be increased at each level of abstraction with additional functionalities. The various levels of abstraction are technological, circuit, logical and system level. Process and packing deals with technology level, routing and layout deals with circuit level. The logical level[2] is between the technological level and system level. encoding, clock gating and the use of parallel architecture, state-machines deals with logical level. The system level design which includes, partitioning, , algorithmic, power management, protocol design and programmable hardware, memory organizations which deals with connecting the resources in a correct functionally and efficient fashion.MEP is defined as the amount of energy consumed by a digital circuit at each per desired operation.

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II. DISSIPATION OF ENERGY

Digital circuit dissipates energy in two forms:-dynamic(E_d) and Statistic(E_s).

In general If N_{gate} to reverse logic gates, N_{turn} to accomplish number of times a task therefore E_d [4]can be equated as

$$E_d = N_{gate}\, N_{turn}\, C_L\, V^2_{dd}$$

C_L is the one logic gate of equivalent capacitance

Es can be expressed as

i) $V_{dd} > |V_{th}|$[4]

$$E_s = \frac{N^2_{gate} n_{bit}\, C_L\, I_o \exp(-v_{th}/nV_T)}{2k\mu\, C_{ox}\, W/L} \times V^2_{dd}/(V_{dd}-V_{th})^2$$

ii) $V_{dd} < |V_{th}|$[4]

$$E_s = N^2_{gate} n_{bit} C_L \times V^2_{dd}/\exp(V_{dd}/nV_T)$$

n_{bit} ⟶ bit number of the data
V_T ⟶ Thermal voltage.

$$E_t = E_d + E_s$$

The amount of energy dissipation in digital circuit is the sum of dynamic and statistic energy.

III ENERGY MEASUREMENT

Energy Measurement is defined as dynamic and leakage energy per operation. The charging of the internal load capacitance is the energy consumed[9] which is caused by the transistor switching is the dynamic energy.

$$E_{opdynamic}(V_{dd}) = C_L(V_{dd}) * V^2_{dd}$$

A small amount of quiescent current occurs in transistors due to this energy is consumed the consumed energy is the leakage energy.

$$E_{opleakage}(V_{dd}) = V_{dd} * I_L(V_{dd}) * t_{op}(V_{dd})$$

The consumed energy can be minimized in dynamic and leakage energy by reducing the supply voltage.

IV MINIMUM ENERGY MEASUREMENT TECHNIQUIES

Based on operating condition , technology, characteristics of the design. Minimum energy measurement techniquies can be classified as:

i) Dynamic voltage scaling

ii) Dynamic frequency scaling

iii) Dynamic voltage and frequency scaling

iv) Ultra dynamic voltage scaling

A. Dynamic Voltage Scaling

Based on workload the clock frequency and supply voltage can be reduced without scarificing the performance this technic is known as dyanamic voltage scaling and it consume minimum amount of energy.

There are four types of DVS systems

i) Ideal :- Changes instantaneously its operating voltage

ii) Feasible :- Varies voltage within a maximum rate i.e., V_{min} and V_{max} .

iii) Practical :- Voltage transition waits for new voltage.

iv) Multiple:- It has N number of discrete voltage and can switch from one to another system.

Address the problem about the way a process clk frequency gets modulated, without affecting performance the process can slow down when it has less work.

Ex:- Svaing the energy and meeting the deadline right on time can be achieved by slowing down the processor to 1/10 cycles/sec, if the system has a workload 10 cycles and one task to execute and a deadline of 100 sec.

DVS tries to address by taking into account two important charactertics between performance and battery life.

1. To sustained the average throughtput the peak computing rate must be higher.

2. Processor uses CMOS logic.

All taks are periodic, the task need to be excuted in a way it complete by its deadline, task are independent and non-preemptive.

B. Dynamic Frequency Scaling

The clock frequency of the CPU can be changed during runtime by using dynamic frequency scaling[6] technic.Each task is optimized according to its deadline and the clock frequency can be reduced to minimum according to the task and ensures that all the deadlines are met[7][8]. And the overall energe consumption can be reduced. Performance metric is used for the determination of the performance of a Computer depends upon the application of the computer system.

For example in case of Personal Computing Systems the Response Time is very important and often is the sole basis for the determination of the performance of the computer.

Whereas in case of Servers the throughput i.e. is the amount of work done in a given amount of time is much more important

But 'Performance' we will be concerning ourselves only with the Response Time.

On one hand we can increase the clock frequency of the CPU to reduce its response time and improve its performance but after a certain limit we need to also increase the voltage input to the CPU to maintain its stability at the high clock frequencies which in turn increases the Energy Consumption and Heat Dissipation of the CPU, thereby shortening its lifespan.

On the other hand we can reduce the clock frequency of the CPU below the standard values allowing us to under volt the CPU and hence reduce the amount of Energy Consumption by the CPU, but this has a impact on the CPU performance negatively. Dynamic Frequency Scaling method is used to balance the performance and energy consumption. It refers to a continual variation of the clock frequency to optimize performance and Energy Consumption of a CPU

C. Dynamic Voltage and Frequency Scaling

Depending on the system workloads, both voltage and frequency can be varied during runtime. This Method is known as DVFS using this methods thermal and performance constraints can be achieved

To minimize the energy consumption in frequency dependent and frequency independent workload[8]a technique called Dynamic Voltage and Frequency Scaling is detemind.

Frequency dependent workload(W^{ON}):- is the number of CPU clock cycles which are executed into the CPU.

$$T^{ON}=W^{ON}/f^{CPU}$$

Frequency independent workload[8](W^{OFF}):- is the number of external clock cycles and depends on the external memory clock frequency.

$$T^{OFF}=W^{OFF}/F^{EXT}$$

The sum of T^{ON} and T^{OFF} is total execution time i.e.,

$$T=T^{ON}+T^{OFF}$$

Scaling the voltage/frequency of CPU more than the switching latency time the CPU must be orders of magnitude of two to three[7].

D. Ultra Dynamic voltage scaling

Ultra Dynamic voltage scaling is a extension of dynamic voltage scaling [5]. To achieve UDVS ,the couples of local voltage dithering (LVD) with sub threshold operation is essential. Supply voltage and frequency is energy efficient because it allows scaling across full range, for high performance it combines dithering and minimum energy operation for low performance. UDVS is flexible.

V PROPOSED METHODOLOGY

A Block Diagram

An important challenge in implementing the minimum energy point tracking system is measuring/estimating the power consumption of the circuit in real-time.To design a novel power aware system for dynamic minimum energy operating point tracking of the circuit. The block diagram of the system is shown in the Fig 1.The system consists of a Energy Monitor circuit, Emin algorithm to find the minimum energy point, voltage regulator to change VDD and Voltage source substrate regulator. The voltage regulator is used to vary the VDD and the voltage source-substrate regulator is used to vary the threshold voltage[8]. The voltage regulator consists of DC-DC converter.In real circuits,

the MEOP is not a fixed point and changes with the workload and the operating condition (e.g. temperature).

For this reason a dynamic run-time optimization algorithm is required to track the MEOP and effectively minimize the energy usage.

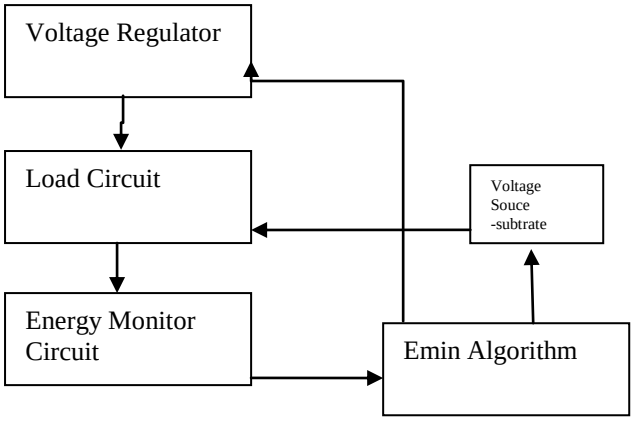

Fig 1: Block Diagram of proposed energy aware system

B. Algorithm

Emin tracking algorithm to find the minimum energy point and the algorithm should be fast for real time application. A dynamic run-time optimization algorithm[1] is required to track the MEOP[3] and effectively minimize the energy usage.

C. Flowchart

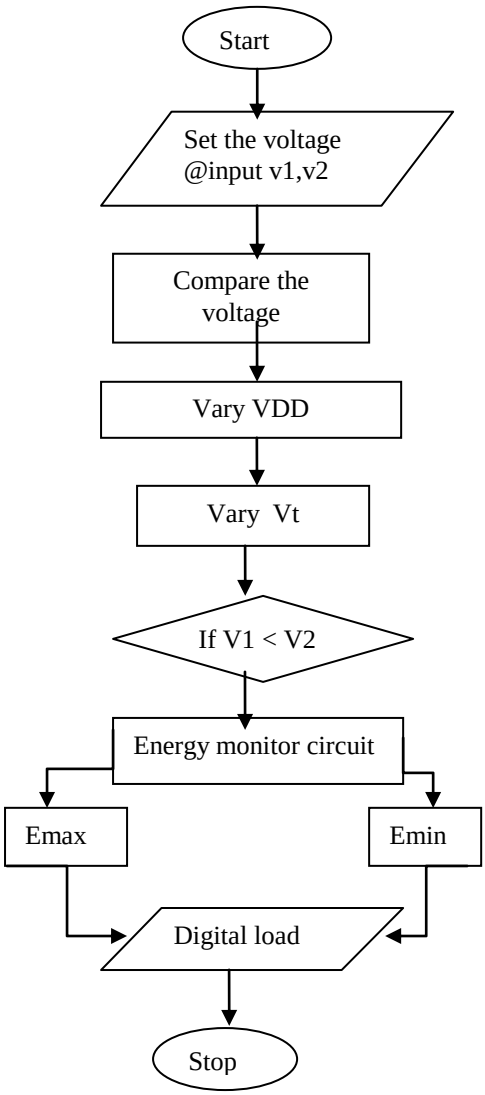

Fig 2 Proposed MEPT flowchart

- **Voltage Regulator:-** The voltage regulator consists of Switched capacitor based DC-DC convertor as it has to consume less energy ,settling time should be fast & it is used to change VDD.
- **voltage source-substrate regulator:-** is used to vary the threshold voltage.
- **Energy Monitor circuit**:- Emin tracking algorithm to find the minimum energy point and the algorithm should be fast for real time application.

VI RESULT ANALYSIS

Design of energy measurement and tracking circuit which will keep track of the energy consumed in the digital circuit and would be a real time energy measuring circuit for digital circuits which consists of optimized DC-DC converter and EMIN algorithm.

VII CONCLUSION

The advance in technology is used to reduce energy consumption at various levels of abstraction by energy reduction techniques in the design flow, and the performance can be increased at each level of abstraction with additional functionalities, and reducing the energy dissipation , efficient energy can be determind by Scaling the frequency and voltage, solution for energy critical applications is achieved at the minimum energy operating voltage for digital load circuit.

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