Design of an Efficient Fault and Congestion Free NoC Design using Adaptive Routing on FPGA

Guruprasad S.P, Chandrasekar B.S

Abstract: ***Manufacturing fault-free System on Chips (SoCs) with performance scaling is a challenging task. The Network on Chip (NoC) architecture offers scalability and reliability to the SoC designs. In this paper, the fault detection and correction mechanism for a congestion-free Router architecture along with Mesh-NoC for different sizes are discussed. The proposed hardware architecture of NoC-Router includes Input registers (which store five -port inputs with Fault injection), Error Correction Code (that encodes the input data) followed by packet formation with Arbitration mechanism (that grants the permission to priority based encoder). The prior packet data is input to the adaptive-XY routing and it operates with the various congestion issues on choosing the shortest route. The detection and correction of the faulty bits from the network are monitored by ECC decoder. This NoC router can tolerate transient fault; provides low-latency and high throughput performance for all MPSoC applications. The Normal –XY Routing algorithm is incorporated in same router for comparison purpose. The synthesis results includes chip area, and maximum operating frequency over Artix-7 FPGA technology. Outcomes are tabulated and they show a marked improvement over previous cases. The performance evaluation is considered in terms of average latency and maximum throughput at different input traffic. It's analyzed for novelty features as well.***

Keywords**:** ***NOC, Fault-tolerant, Error Code Correction, Adaptive-XY, Normal-XY, Mesh-Network, Packet formation, FPGA***

I. INTRODUCTION

The Usage of the processing element (PEs) and Intellectual property (IP) cores on a single chip and the design of SoCs is a complicated task as it calls for many security concerns. During manufacture of fault-free chips, some of the challenging situations are encountered due to the increase in chip density, energy consumption and the decrease in chip reliability. These limitations can be overcome in the shared bus architecture. However, these architectures fail to meet the scalability issues. The NoC provides scalability solutions by replacing current bus-based architecture with an interconnected network for SoC's [1].

To provide high performance and low power requirements in SoC's, the NoC provides the communication platform among the IP cores. The testing of the complete network and its operations during data packets transmission comes with some challenges.

Thus, to test the different components of the network, several test methodologies are documented.

Among these, the structural testing includes the Built-in-self-test (BIST) or scan-chains. These techniques test the stuck-at-faults in a network structure as well. Also, the network functionality testing ensures that the routing and packet delivery is up to the mark. They aim for high-level switching faults and routing in the NoC level. The NoC's testing requirements add more complexity like designing a fault tolerant system, detection ability, finding the fault location, and fault coverage [2-3].

The NoC architectures have to address transient and permanent faults. The transient faults take place due to electromagnetic interferences, power fluctuations, electric noises, radiations, and environmental conditions like temperature, pressure humidity problems. The ECC with retransmission technique along flow control methods are used to avoid the transient faults. The permanent faults occur due to defects in chip making and aging effects. The permanent faults can be avoided by using fault-tolerant routing systems with significant network topology changes. Among the existing NoC technologies, the transient faults are quite difficult to detect and hamper the performance [4].

Various routing algorithms are used in fault-tolerant NoC systems to improve the stability and overall performance. The deterministic-XY routing algorithm is a simple, unique routing path, provides the higher performance and low energy consumption to the networks. The adaptive routing algorithm provides the congestion free network and stable performance [5-6]. The fault tolerant systems must provide the unique routing path for the noted source-destination address, link failures and router presence in the network to improve the scalability and performance [7-8].

In this article, the design of an efficient congestion free NoC Router with fault recovery using ECC-Encoder-Decoder (ECC-ED) is elaborated. The congestion free Routing is performed using Adaptive–XY Routing. A review of previous work on NoC based Fault tolerant and fault recovery methods, its approaches and research gaps with problem identification are elaborated in section II. The Section-III explains an overview of the proposed methodology with the schematic flow. The hardware architecture of the proposed NoC Router using ECC-ED and Adaptive–XY Routing is elucidated in section IV.

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* Correspondence Author

Guruprasad S.P*, Research Scholar, Dept. of ECE, Jain University, Bangalore, India. Email: spgp1306@gmail.com

Dr. Chandrasekar B.S, Director, CDEVL, Jain University, Bangalore, India. Email: cshastry2@gmail.com

Section V deals with the synthesis results and performance analysis of the Proposed NoC router. Finally the analysis of overall work with improvised results and conclusions are scripted in Section VI.

II. LITERATURE REVIEW

A review of the existing works includes different Fault tolerant and fault detection mechanisms for NOC Routers and their applications are reviewed here.

The Poluri et al. [9] has described reliable Chip-Networks which can tolerate Multiple Permanent faults in routing pipeline using MTTF (Mean time to Failure). This model includes Routing computation, Virtual Channel and Switch allocation in a crossbar switch. It only tolerates the faults without attack on specific detection. Bahrebar et al. [10] has a reconfigurable and adaptive fault-tolerant routing NoC. This design is based on deadlock-free routing with Abacus Turn Model. The highlights are the dynamical updates based on the location and congestion faults in the Network. Rerouting is avoided by distributing packets through the available paths and maintaining the Router reliability and deadlock-freedom without the use of virtual channels. The Jojima et al. [11] has explained the fault-tolerant routing technique for 2D- NoC based router components. The Partial fault model is used to replace the fault nodes with routing restrictions which in turn improves node usability and latency in communication. For Mesh topology based NoC’s, the fault tolerant routing is described in Tata’s Et al. [12]. The dimension order (DO) routing is used to reduce the packet loss during runtime. The design supports fault links in the X or Y dimensions along with Deadlock and live-lock freedom with reliability improvements. The Fochi et al. [13] has an online fault detection method at a router level for NoC based MPSoC. The detection of faults at NoC with reconfiguration router provides proper communication between PE (Processing elements). The fault tolerant method is introduced in all the OSI Layers with detection protocol and scalability.

Chatterjee et al. [14] have developed a reconfigurable fault-tolerant algorithm for NoC design which supports multi-core systems. The router model is set to recover the faults by dynamic routing table updation on individual routers. Minimization of the degradation with system performance improvement for single and multiple fault recovery mechanisms are incorporated with network simulator architecture. Yan et al. [15] have achieved the NoC Reconfigurable design which corrects the faulty routers with the avoidance of the PE isolation. The revised XY- Routing algorithms are used to achieve the NoC Reconfiguration as and when the route fails with rerouting the PE. The fault detection method is used between the FIFO's and Crossbar switch in router model with better reliability. The power and area overhead is not encouraging because of the conventional Routing approach. A routing level solution is introduced for fault tolerant, masking and detection NoC’s in Zhang et al. [16]. To address the faults which are severe in the control path with illegal turns, the non-minimal routing algorithm is used with reliable improvements. The fault tolerant transmission method for NoC with low latency is described in Huang et al. [17]. The lightweight error detectors are used in the router’s input port to verify the correctness of header flits. To correct any flit in the packet, the Decoder method is used in Network Interfaces.

Kadeed et al. [18] has presented the real-time soft error resilient NoC router for ASIC platform, along with retransmission and error detection methods. The resilient NoC router here includes cross bar switch allocator with pre-processing input buffers. The resilient NoC router evaluates the area and power overhead with a different application mechanism under error conditions. Wang et al. [19] highlights the BIST (Built-in–self-Test) based NoC to improve the reliability. The quick fault detection and affected data packet detection are achieved using BIST. Due to data dependencies, the relevant performance losses are bound to take place. Yuan et al. [20] explains the principle of send-back router architecture using Error correction code (ECC). In Network Interface, ECC encoder and decoder are deployed to reduce hardware overhead. The router is designed using conventional approaches. The deadlock-free XY-YX Router is designed for NoC by Lee et al. [21], which inhibit the deadlocks, by adding the physical channels as a replacement of virtual channels in a router with the horizontal direction and this also reduces the complexity in a router. The NoC based MPSoC is designed using FPGA by Hassan et al. [22], with minimized router architecture to reduce the gate count and complexity of the system. Totally self-checking (TCS) design for VLSI circuits using error detection coding (EDC) are developed by Natarajan et al. [23]. The TCS permits the hardware faults detection in online configuration. The combinational and sequential Berger technique is used for the comparison in EDC with area and gate code reduction. Kanakala et al. [24] and Killian et al. [25] have elaborated the reliable NoC switch performance using Hamming codes, which detect the transient faults and improve the performance.

It has been noticed from the review of previous documented literature that the significant progress is made on the fault-tolerant and fault detection schemes with the software approaches. Very few of them have looked at the hardware approaches. Also, real time scenarios with hardware approaches have not been considered till date. In this regard, the following research gaps are identified.

- The existing fault tolerant and fault detection based router designs for NoC which are used in MPSOC applications for error-free communication have scalability and reliability problems on hardware platforms.
- Very few hardware-based designs can be located in terms of fault-tolerant and fault detection based NoC routing mechanism.
- Most of the fault tolerant and detection based NoC router on hardware platform have considerable overhead with cost-effective solutions in SoC.
- Most of the conventional routing approaches have failed to provide the congestion free routing which is adaptive in nature.

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- The fault detection with recovery and congestion free routing in NoC router having high-throughput is yet to come with optimized constraints.

Thus, an efficient cost-effective fault and congestion free routing solution is the need of the day.

III. RESEARCH METHODLOGY

This work aims to design a fault and congestion free routing architecture for NoC based systems. To achieve the fault-free routing in a network, the error correction code (ECC) model is introduced in router architecture. The Adaptive routing with reconfigurability is used for congestion-free routing. The hardware architecture shows a marked improvement over the NoC performance with respect to low latency and high throughput. The schematic flow is highlighted in figure 1. The design of fault and congestion free router, which includes the input register with fault injection, ECC Coding, packet formation, arbitration followed by priority encoder, adaptive XY Routing, ECC decoder, and output registers are depicted.

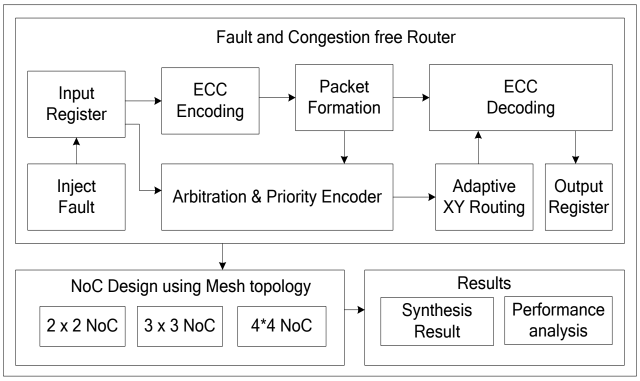


Fig.1. Schematic representation of proposed work

Our router offers transient faults detection and correction by using ECC encoder and decoder (ECC-ED). Modified Hamming codes are used in ECC-ED design. This makes it easy to design and consumes less number of clocks as compared to complete detection and correction mechanism. The arbitration module plays a very important role. It collects the data requests based on priority and permits the data packets to be used in Adaptive –XY Routing module. On designing the fault and congestion free router, the construction of NoC architecture using Mesh topology has been tested. The different network sizes like 2x2, 3x3, and 4X4 NoC Routing architecture are designed by using ECC-ED and Adaptive-XY Routing. For performance analysis, the Normal –XY routing is used with proposed fault and congestion free router and NoC design of different sizes. The outcome includes the synthesis results of the adaptive-XY based Router with Normal –XY Router tabulation with an area and maximum operating frequency improvement. The performance evaluation of this design includes latency and throughput based on packet injection rate. The outcome suggests that it offers low latency and high-speed NoC design with fault and congestion free routing on the low-cost FPGA device. The next section describes the detailed architecture of the proposed NoC router.

IV. CONGESTION AND FAULT FREE NOC ROUTER

This router aims to reduce the hardware complexities along with fault recovery and congestion free routing for the NoC based system. The fault and congestion free router architecture is clearly shown in figure 2. This individual router input ports are 8-bit local (Li), 32-bit East (Ei), West (Wi), South (Si), and North (Ni). Whereas the 8-bit local (Lo), 32-bit East (Eo), West (Wo), South (So), and North (No) are output ports. The augmented 1-bit fault injection input clearly helps in investigating the congestion parameters in the configuration.

The fault injection bit is generated randomly from the linear feed shift register (LFSR) are considered as transient faults and inject the 1-bit fault information to the Input register's 8-bit local input by XOR operation. The input register stores all 5-port inputs (from PE) via Network interface in temporary registers and the local input port is corrupted. The Local 8-bit register output is given as input to ECC encoder. The encoded data and local register outputs are used to frame the 32-bit packet. The packet information and four register ports are inputs to the priority encoder.

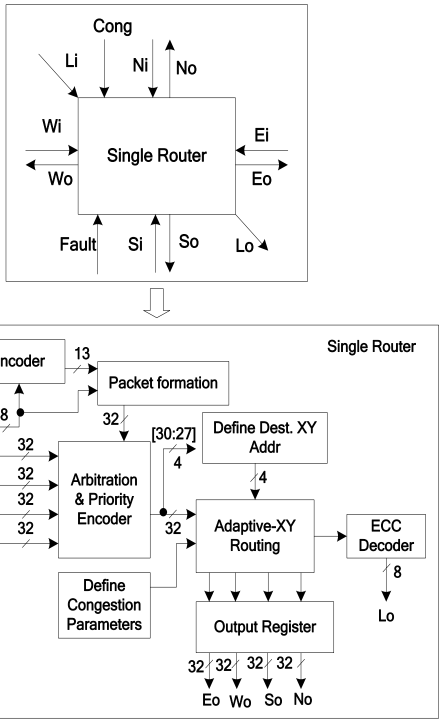


Fig.2. Detailed Fault and Congestion free Router Architecture

Based on arbitration grants, the priority encoder issue the 32-bit packets to Adaptive XY- Routing model where MSB Bit is request Line, the next 4-bits [30-27] are set as destination XY address. In the initial stage, define the current XY address and define the congestion parameters to start the adaptive-XY routing. Based on the routing algorithm, it performs the routing operation and generates the five port outputs as a packet from source to destination based on the address.

The local output information is obtained from the output register and fed to ECC Decoder. The ECC Decoder decodes the fault bit and generates the desired 8-bit output. The following sections give an elaborated information about each module of the NoC Router.

A. ECC Encoder

Any fault in the Router or NoC system leads to error and the error leads to failure of the entire NoC system. The ECC is used to detect the faulty error and correct it. The ECC Encoder uses modified Hamming codes (13, 8), which encodes the 8-bits of local-port data information (d) into 13-bits by adding 5-bit parity bits. The Encoder output (E) which is 13-bits, in that first 8-bit output (E7-E0) is same as 8-bit inputs and the 5-bit parity bit (P) are generated using following relations in equation (1):

$$\begin{aligned} P_0 &= d_6 \oplus d_7 \\ P_1 &= d_3 \oplus d_4 \oplus d_5 \\ P_2 &= d_1 \oplus d_2 \oplus d_5 \\ P_3 &= d_0 \oplus d_2 \oplus d_4 \oplus d_7 \\ P_4 &= d_0 \oplus d_1 \oplus d_3 \oplus d_6 \end{aligned} \qquad (1)$$

The 5-bit parity data information with concatenating with 8-bit local data, to generate the 13-bit encoded data. This encoded data are used for packet formation and ECC decoding to detect and correct the faulty error.

B. Packet formation

The packet formation is framed based on the received encoded data bits and local register outputs. The 32-bit packet contains, 8-bit flit data from the local input (Li), the first (LSB) 6- bits are reserved for future as a request and acknowledge control signals. The 13-bit [26:13] are encoded data, and used in future ECC-decoder for detecting and correcting the faulty error bit. The 2-bit [28:27] Destination Y address followed by 2-bit [30:29] Destination X address and finally 1-bit request line used to provides the prior packet information based on the ports. The packet formation is represented in figure 3.

1-bit	2-bit	2-bit	13-bit	8-bit	6-bit
31	30 29	28 27	26 14	13	5 0
Req	Dest.X	Dest.Y	Encoded Data	Flit data	Unused

32-bit

Fig.3. Packet formation

C. Arbitration and priority Encoder

The arbiter design has 5-bit request input and 5-bit grant output. The priority-based arbiter is designed based on Moore state machine. The arbiter is designed using binary encoding style, next state (combinational) logic and present state (sequential and output) logic. The 4 -states are represented in binary encoding formats like zero one, two, and three. The arbiter design uses 3–process state transition and it is pipeline architecture to improve the timing and speed optimization. The combinational logic of arbiter is designed based on the 5-bit input requests from the MSB (31th) bit of Packet data, East (Ei), West (Wi), South (Si), and North (Ni) with all the next state possibilities. The sequential logic finds the present state based on the next state using combination logic. The output logic generates 5-bit grants based on the present state logic. The arbiter provides 5- bit select line to the priority encoder. If the select line is set to 0 for packet input from the packet frame, 1 for east, 2 for the west, 3 for the south, and 4 for north input data from the input register outputs are selected in the priority encoder. The priority encoder 32-bits are used in adaptive XY routing algorithm as a packet formation and sets the priority encoded [30-27] bits as a destination address.

D. Adaptive XY Routing Algorithm

The performance of the NoC system depends upon the routing algorithm and topology which is used for the design. The Adaptive –XY routing (A-XY) algorithm is considered for Routing the NoC network. It is a normal –XY routing with an adaptive form. The 1st dimension in X –Direction and 2nd dimension in Y-direction with the minimum number of routing node operation is performed and packet information is moved to destination location with less congestion. The less congested adaptive –XY is fully routed in NoC and finds the shortest path based congestion parameter configuration. The Adaptive –XY routing algorithm operational flow is represented in Figure 4.

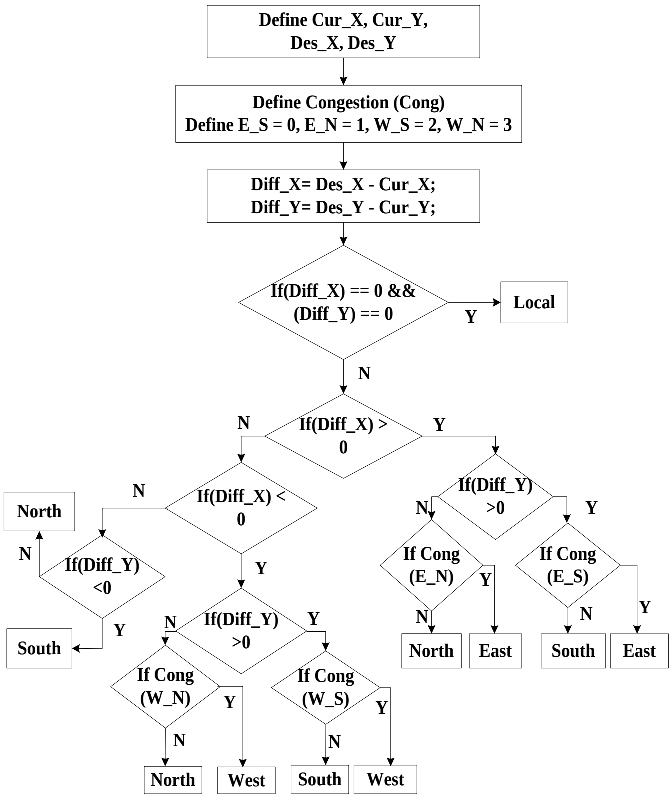


Fig.4. Congestion free Adaptive-XY Routing Algorithm operational flow.

Define the Current-XY (Cur_X, Cur_Y) and destination-XY (Des_X, Des_Y) address as per user request in NoC Router. Configure the congestion parameters between five ports.

For alternative routing paths, Set the Congestion (Cong) between the routing nodes as 0 for E_S (East versus South), 1 for E_N, 2 for W_S, 3 for W_N. Find the Difference between Cur_X and Des_Y, set as Diff_X and similarly for Diff_Y.

If the Diff_X and Diff_Y are zero, the local port is selected, which is having fault information. If the Diff_X and Diff_Y are greater than zero, check the congestion free path using Congestion parameters. If the Cong (0) is set, an east or west port is selected as an alternating routing path. Else Cong (1) is set, for south or east path. Similarly, If the Diff_X is less than and Diff_Y is greater than zero, then Cong(2) else Cong(3) will be set, to choose the alternative routing path has south or west and north or west respectively.

E. ECC Decoder

The ECC Decoder is used to decode the faulty error bit available in Local register output. The faulty error bit is detected by using encoded data and parity bits. The check bits (C) are used as parity bits to check the error status. The 5-bit Check bits are generated using following relations in equation (2):

$$\begin{aligned} C_0 &= E_6 \oplus E_7 \\ C_1 &= E_3 \oplus E_4 \oplus E_5 \\ C_2 &= E_1 \oplus E_2 \oplus E_5 \\ C_3 &= E_0 \oplus E_2 \oplus E_4 \oplus E_7 \\ C_4 &= E_0 \oplus E_1 \oplus E_3 \oplus E_6 \end{aligned} \qquad (2)$$

The error detection (A) is done based on parity and check bits using following relations in equation (3):

$$A = P \oplus C \qquad (3)$$

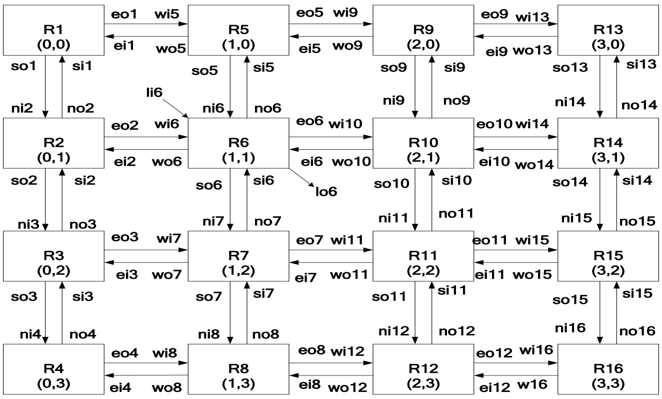
The error correction (O) is calculating based on 'A' and encoded bits using following relations in equation (4):

$$\begin{aligned} O_0 &= (A_3.A_4) \oplus E_0 \\ O_1 &= (A_2.A_4) \oplus E_1 \\ O_2 &= (A_{2.}A_3) \oplus E_2 \\ O_3 &= (A_1.A_4) \oplus E_3 \\ O_4 &= (A_1.A_3) \oplus E_4 \\ O_5 &= (A_1.A_2) \oplus E_5 \\ O_6 &= (A_{0.}A_4) \oplus E_6 \\ O_7 &= (A_{0.}A_3) \oplus E_7 \end{aligned} \qquad (4)$$

The injected fault information is corrected using ECC decoder as considered as final 8-bit local output data [O7-O0]. The proposed router detects and corrects the 1-bit fault information while it detects the 2-bit fault information.

F. NoC Router Using Mesh Topology

An Example of proposed 4X4 NOC Router using Mesh topology is represented in figure 5. The router design is done individually for all 16 nodes. Then the instantiation for all the 16 points are performed to construct the 4x4 NoC Routers. For all the routers R1-R16, local input and local output are the default and not presented in figure 5. The Router (R6) is shown with local in (li6) and local output (lo6) for the demonstration purposes. For each individual router, an identity of current address X and Y have to be fixed. For example, Router-7 (R7) the current address of X and Y is (1, 2) similarly For R16, Current XY address is (3, 3). R1 has 3-port input, default local input along with east input (ei1) which comes from west output (wo5) of R5 and south (si1) input comes from the north output of R2. Similarly, all the individual routers are interconnected, to form 4X4 NOC router. The 3-input ports are used in R1, R4, R13 and R16 router. The 4-input ports are used in R2, R3, R5, R8, R9, R12, R14, and R15 routers. Similarly for the 5-input ports are used in R6, R7, R10, and R11 router. All these intriguing connectivity's have been carefully worked out. The NoC Router easily identifies the dynamic bypass. If the router is faulty then it finds the faulty routing error path and prevents the loss of data packet in NoC from one router to another. If any congestion is present in the router then it automatically finds the alternate shortest path for routing. This is the most important prerogative in the entire design. And adds to the performance improvement.



An example of 4X4 NOC- Router using Mesh topology

V. RESULTS SYNTHESIS AND PERFORMANCE ANALYSIS

A. Result Synthesis

Our fault and congestion free NoC Router is designed and synthesized using Xilinx platform on Artix-7 FPGA Technology and Verilog-HDL is considered for NoC Router architecture designs. The NoC Router is configured to process the data packets of 8 flits from one source router to other destination router based on Normal and adaptive XY-routing. The Synthesis results of Fault-tolerant NoC Router for different designs include Single Router, Mesh 2x2, Mesh 3x3, and Mesh 4X4 is tabulated in Table-I and graphical representation in figure 6.

Table- I: Synthesis Results of Fault-free NoC Designs

Area Utilization	**Slice Registers**		**Slice LUT's**		**LUT-FF pairs**	
NOC Design	***N-XY***	***A-XY***	***N-XY***	***A-XY***	***N-XY***	***A-XY***
Single router	138	76	179	163	126	70
Mesh 2x2	394	313	433	272	366	245

Mesh 3x3	1008	762	1210	718	921	634
Mesh 4x4	1900	1411	2294	1334	1741	1217

The Area utilization in terms of Slice Registers, Slice LUT's and LUT-FF pairs for Normal and Adaptive-XY is presented for different NoC designs. The Single router using adaptive-XY requires 76 registers, 183 LUT’s and 70 LUT-FF Pairs on Artix-7 FPGA. From the analysis, Adaptive –XY (A-XY) Routing based NoC Router consumes less Area overhead than Normal –XY (N-XY) Routing. For Single Router, 44.92% registers, 8.9% LUT's and 44.44 % LUT-FF pairs utilize less area overhead than Normal –XY Routing. Similarly using adaptive –XY Routing for Mesh 2X2 NOC, 20.55%, 37.18% and 33.06%, For Mesh 3x3 NoC, 24.4 %, 40.66%, and 31.16%, For Mesh 4x4 NoC, 25.73%, 41.84% and 30.09% in terms of Slice registers, LUT'S and LUT FF-Pairs utilize less area overhead respectively than Normal –XY Routing.

Fig.5. Comparison Analysis of Area utilization

From the synthesis results, the maximum operating frequency of Fault free NoC Router with different NoC sizes includes Single Router, Mesh 2x2, Mesh 3x3, and Mesh 4X4 is represented in figure 7.

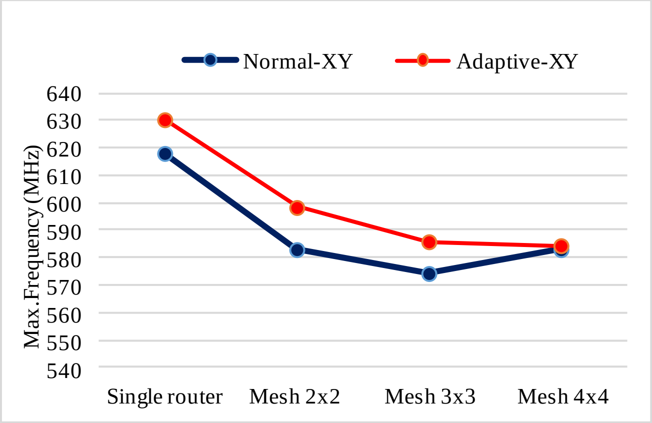


Fig.6. Maximum Operating Frequency of NoC Designs using Routing Algorithms

For Single Router, the Maximum frequency operated up to 630.369MHz on Artix-7 FPGA Technology. Using adaptive –XY routing, on an average 2% faster operating than Normal-XY Routing for single Router and different size NoC Routers. These synthesis results clearly show that the proposed architecture is effectively implemented in FPGA Technology and also stated that better speed and logical resource trade-off has been achieved.

B. Performance Evaluation

The performance evaluation of this work is analyzed in terms of average Latency and throughput with respect to input traffic (load) and different sizes of Mesh-NoC with constant traffic. For analysis purpose, Wormhole switching technique and uniform Traffic patterns are considered.

The Packet Injection Rate (PIR) in a single clock cycle defined as, total numbers of data packets that can be sent. For Example, the Processing element is having a PIR = 0.3, it can send 30 data packet in 100 clocks. The Flit injection rate (FIR) is multiplying the PIR value with the number of flit in each data packet.

The Latency is calculated based on the Number of flits used in the data packet along with ECC operation, arbitration, and Routing logic clock cycles. The minimum latency for a single Router takes 11 clock cycles. For Mesh-NoC, the time taken to forward from source to destination in network is two clock cycles, the number of the PE’s used, Traffic network per packet. In this work, the average latency for a single router, 2X2, 3X3 and 4X4 using Adaptive –XY routing are evaluated with respect to input traffic are represented in figure 8. The average latency for each NoC sizes is represented in terms of clock cycles (ns).

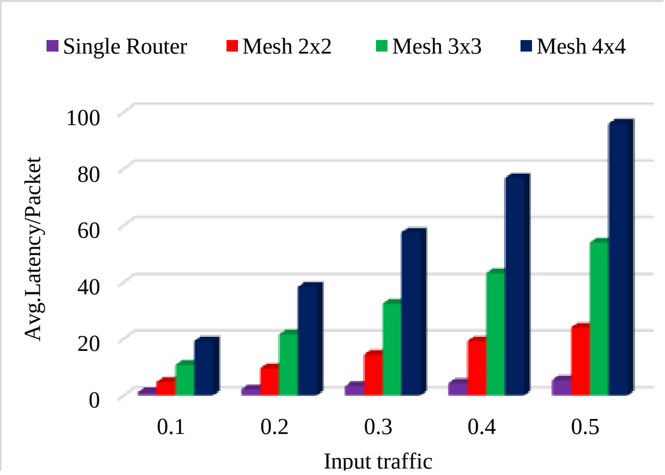


Fig.7. Average Latency v/s Input traffic of NoC Design for different Mesh sizes using Adaptive –XY Routing

The maximum throughput of the NoC is depended on the number of the PE's followed by data packet size, PIR and Maximum operating frequency (MHz) used. An assumption is made that the PEs are connected to NoC boundary.

For an example of 4X4 NoC with a 32-bit data packet size and 16 PE's are connected and the maximum operating frequency of the Artix-7 FPGA technology. The maximum throughput is 149.92 Gbit/sec at 0.5 traffic. Figure 9 shows the maximum throughput of the Single router and Mesh-NoC of different sizes with respect to different input traffics using Adaptive –XY Routing.

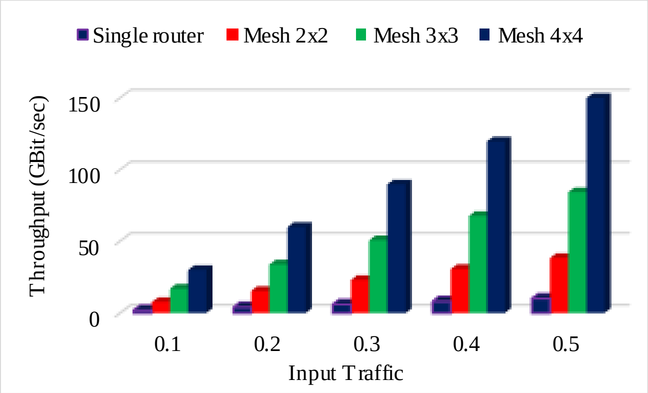


Fig.8. Max. Throughput v/s Input traffic of NoC Design for different Mesh sizes using Adaptive –XY Routing

The average latency of single router and Mesh-NoC with constant Packet inject rate (PIR) = 0.5 for both adaptive –XY and Normal-XY routing is represented in Figure 10. It has been noticed that Adaptive –XY utilizes less average latency in terms of clock cycles than Normal-XY Routing. The 4X4 NoC takes 96 clock cycles using Adaptive-XY than 106 clock cycles using Normal –XY Routing.

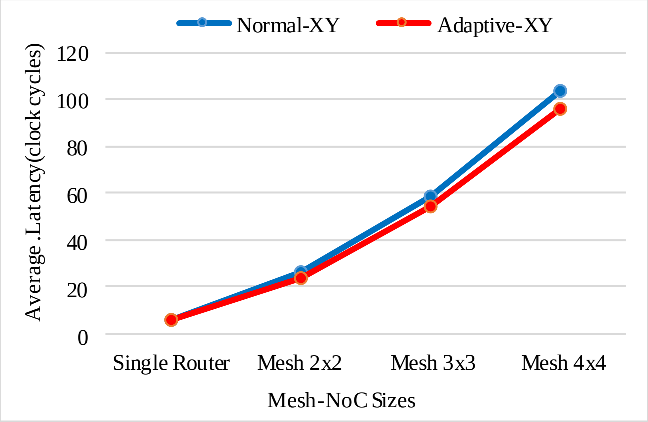


Fig.9. Average Latency of NoC Design for different Mesh sizes at PIR=0.5

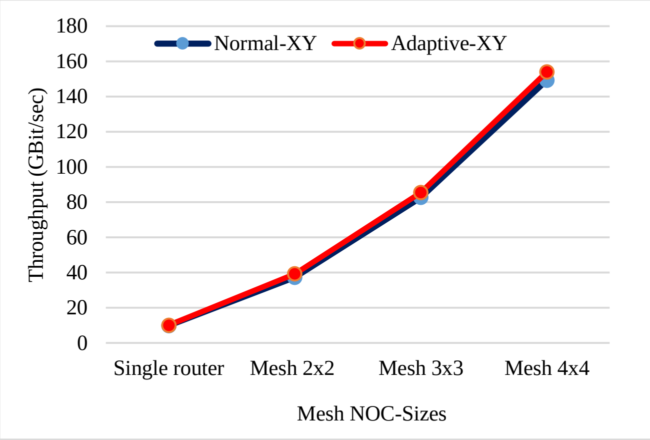


Fig.10. Maximum Throughput of NoC Design for different Mesh sizes at PIR=0.5

The Maximum throughput of the single router and Mesh-NoC with constant Packet inject rate (PIR) = 0.5 for both adaptive –XY and Normal-XY routing is represented in figure 11. It has been noticed that Adaptive –XY works at high throughput than Normal-XY Routing. The 4X4 NoC takes 153.92 Gbits/sec using Adaptive-XY than 148.92 Gbits/sec using Normal –XY Routing.

VI. CONCLUSION

This paper presents the design of Fault detection and correction along with congestion free Router architecture for NoC's. The proposed fault detection and correction can tolerate any transient faults. For Fault detection and correction, the ECC-ED using modified Hamming codes is incorporated in router design while an Adaptive –XY Routing algorithm is used for the Congestion problems. The proposed Router and Mesh-NoC at different sizes using adaptive-XY routing are compared with Normal-XY routing in terms of synthesis and performance analysis. In the synthesis results, the proposed single router and 4X4 Mesh NoC area overhead in terms of Slice registers, LUT's, LUT-FF pairs improved at an average of 31.9% than Normal –XY Routing using Artix-7 FPGA. The performance analysis and comparison of Router and Mesh-NoC includes the average latency and throughput with respect to input traffic and are analyzed with improvements over Normal-XY Routing. This architecture can be incorporated in futuristic researches with the security features to router and NoC to strengthen the data packet from the active and passive attacks as well.

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AUTHORS PROFILE

Mr. Guruprasad S.P received his B.E Degree in Electronics and communication from VTU, Karnataka, India in 2007, Master of Technology in VLSI Design and Embedded System from VTU in 2011. He is working in Private Organization as a Sr. Design Engineer and has 7 years of experience in VLSI Field. He is pursuing his Ph.D. from Jain University, India. His research area includes VLSI Design, Network Elements Design, Computer Network Security, MPSOC, and FPGA Design

Dr.Chandrasekar B.S born in 1965 secured state ranks in his 10th and 12th classes. He acquired B.E (E&C) from BMSCE, Bangalore and proceeded to IISc for his Master's and Doctoral Degrees. He was a Professor / HoD from 1996 to 2000 at BMSCE for both day and evening colleges. During this period, he was also Chairman, BoE (BU) and BoS (VTU). Then on he proceeded to work with Infosys Technologies for 14 years in the 'Telecom Software' domain. Presently, he is Director for Distance Education & Virtual Learning @ Jain Deemed to be University.

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