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Modeling and Simulation of the Flyback Converter using SPICE Model

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Abstract*: *This paper presents to find a sufficient model of integrated passive structures for high frequency analysis and prediction in power electronic circuits. At high frequencies there are many parasitic oscillations that begin to circulate in the power circuits. Some sources of these oscillations include inter-component connections and their environment begin having electromagnetic significance, unmodeled characteristics in the semiconductor devices, Parasitic impedance characteristics of discrete passive components, Interference from an imperfect source and a ground plane and Interference from radiation. A simulation model involving most of these factors can prove valuable in distinguishing between the causes of parasitic oscillations. A designer can modify the parameters of a particular parasitic element, and observe its effect on the oscillations, hence seeing which factors are the most significant.

Index Terms*: *Power electronic circuits, Integrated passive circuits, Higher frequencies, EMI, MOSFET, SPICE Model

I. INTRODUCTION

Traditionally, The flyback converter is an example of switching a clamped inductive load to give a controllable DC-DC converter. In today's energy engineering, any power device has a chief design requirement of being as efficient as possible. Electric energy losses and manufacturing costs must be minimized, and spatial usage should be constrained [1]. A further chief design requirement in power electronic systems is that strict control on stray oscillations must be maintained, because power signals with high-energy content can easily damage the power devices to which they are connected. Electromagnetic compatibility (EMC) is the field of restricting the effect of a power device's noise on the operation of other devices that are electromagnetically coupled to it. An integrated architecture has recently been developed for power converter circuits, with the above requirements acting as the main constraints and driving forces [2]. SPICE supports good models for semi-conductor devices, which are not easily modelled from first principles if one was to construct their own circuit simulator. Parametric studies are also well supported by the PSPICE A/D environment.

The main objective of this paper is to contribute towards the development and verification of a simulation tool that can be effectively and confidently used to predict performance of integrated passive circuits operating in power electronic circuits [3].

This study seeks to gain a confidence as to the extent of accuracy and the boundaries of application of SPICE-compatible models, both in the frequency and time domains. The SPICE-compatible models include the lumped element models, and one solution method for the distributed model [4].

This paper is organized as follows. Section II describes the analysis of flyback converter and defines the operating principles. Section III involves the design of the flyback converter and derives the design equations. Section IV presents the converter measurements in steps. Sections V gives the results and discussions. Finally, Section VI provides the conclusions.

II. ANALYSIS OF FLYBACK CONVERTER

Figure 1 shows the circuit diagram of the ideal discrete-component flyback converter. When the switch is closed, the orientation of the voltage excitation across the inductor on the supply side will result in the diode being reverse-biased on the load side. The constant voltage excitation across the supply-side inductor will result in a rampant increase in the current flowing through it. Thus, the magnetic energy that was stored in the supply side in the switch on-cycle is captured from the load side on turn-off and dissipated at the load in the switch's off-cycle.

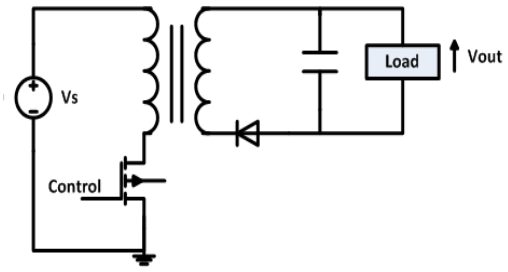

Fig. 1. Basic lumped element model for flyback converter circuit.

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The expected waveforms of ideal operation are shown in Figure 2. This mode of operation, where the load-side current reaches zero before the beginning of the next cycle is known as Discontinuous Conduction Mode (DCM).

The alternative mode is when the load-side current does not reach zero before the switch turns back on, in which case the supply-side inductor recaptures the magnetic energy and begins its ramp up in current from a non-zero initial condition. This is known as Continuous Conduction Mode (CCM).

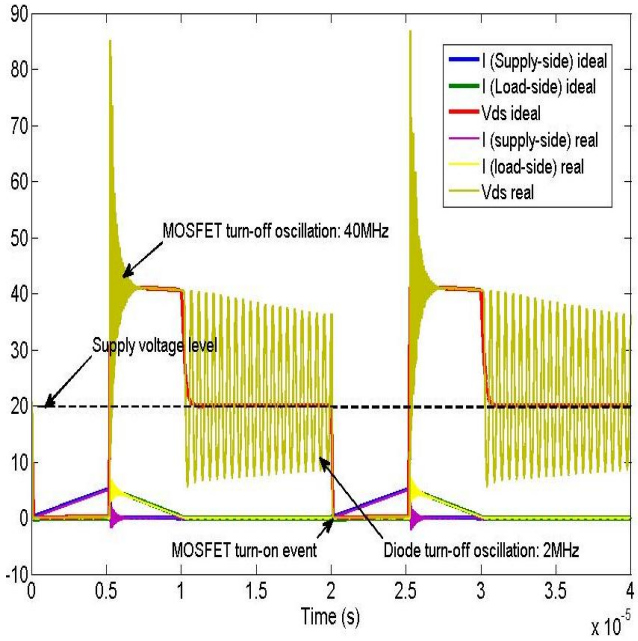

Fig. 2. Waveforms of flyback ideal operation superimposed with typical parasitic effects.

III. DESIGN OF FLYBACK CONVERTER

The design of a flyback converter requires a wide understanding of a variety of components and disciplines. The problems that have to be dealt with during the design process are for instance, magnetics, control loop analysis and power devices such as switches, capacitors, and transformers. Therefore, a theoretical review of the operating principle of a flyback converter, circuit description and operation modes is done [5]. There are three main parasitic effects that must be accounted for in the design of flyback converters. The first, and usually the most critical, is that upon the MOSFET turn-off event, a spike occurs at the MOSFET drain-source voltage. This spike is followed by high-frequency oscillations, which usually attenuates to insignificance within the off-portion of the duty cycle. This effect is caused by the presence of leakage inductance in the couple inductor system. Not all the flux is captured by the load-side circuit, so the remaining current is forced to dissipate through the MOSFET in as fast a time as possible. This rapid change in current is resisted by the leakage inductance in the form of an opposing voltage spike [6]. The inductance of the interconnect path between inductor and MOSFET also contributes to this, and is usually lumped together with the inductor leakage inductance. The oscillation is caused by resonance between this inductance and the junction capacitance of the MOSFET. This oscillation is a high frequency because both the junction capacitance and the leakage inductance are small [7].

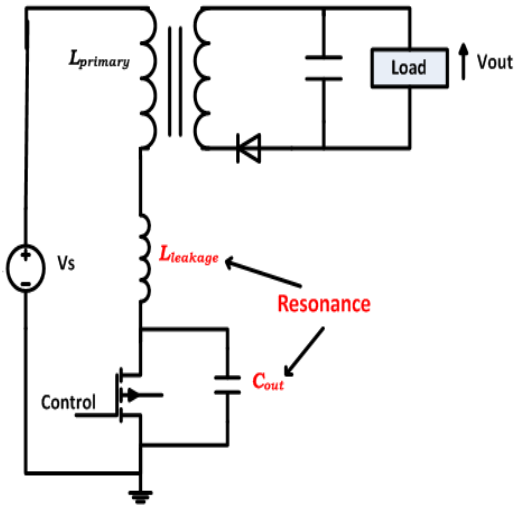

Fig. 3. The parasitic circuit elements that resonate to cause oscillations.

The parasitic circuit elements of a basic flyback converter are shown in Figure 4. The second parasitic effect occurs in DCM, when the diode current reaches zero, and the diode turns off. Resonance occurs between the magnetizing inductance and the junction capacitance of the MOSFET. No current is flowing through the diode, so the parasitic junction capacitance of the diode does not contribute to this oscillation [8]. Since the magnetizing inductance is much greater than the leakage inductance, the frequency of this effect is significantly lower than that of the MOSFET turn-off oscillation. The diode turn-off oscillation is present even under the case of unity coupling between inductors, i.e. zero leakage inductance. These oscillations are characterized by low damping because losses are minimized in such circuits, which requires low resistance. Inserting extra resistance to increase damping will decrease efficiency, which is not acceptable in power electronic converters [9].

The third parasitic effect is a common mode current that flows through the inter-winding parasitic capacitance. This does not reduce the functionality of the converter, nor will it threaten to damage any components, but it must be restricted due to the serious EMI issues it raises. The use of the planar integration technique has some advantages to solve these problems. The much lower leakage inductance can be achieved using this architecture [10]. A lower leakage inductance will decrease the voltage spike upon MOSFET turn-off. It will also increase the frequency of oscillation, but at such high frequencies, the skin effect introduces resistance that will increase damping. Multilayer conductor technology can be used as a high-frequency filter. However, the inter-winding capacitance is now significantly greater.

This capacitance is now

well-controlled, as opposed to the wire-wound structure. Considering this improved controllability, it is recommended as future work for structures to be designed that implement a leakage energy recapture strategy [11].

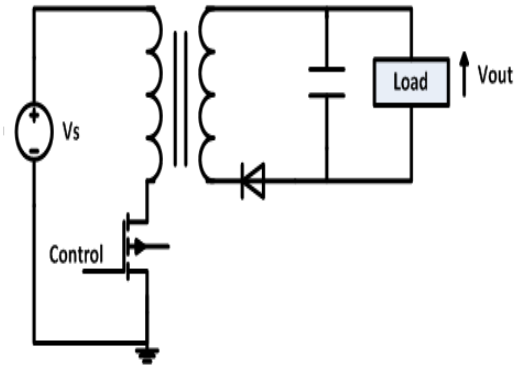

Fig. 4. Discrete component circuit diagram for a basic flyback converter.

The discrete-component circuit diagram of a basic flyback converter is shown in Figure 4. The integrated passive structure will incorporate, as an example, the coupled inductors and DC bus capacitors – four passive components. A possible structure makes use of four parallel planar conductors, enclosed in a magnetic core. Figure 5 shows a connection scheme for the terminals of the structure's conductors.

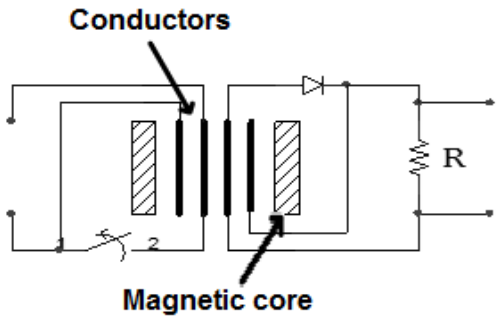

Fig. 5. Connection scheme for proposed structure.

The conductors are enclosed by a magnetic core, resulting in high coupling. As a result, conductors share a common voltage distribution profile, but at different levels with respect to ground. This is illustrated in Figure 5, where a linear voltage distribution is assumed. The orientation of the middle conductors achieves the function of a coupled inductor. Each outer conductor forms a DC bus capacitor with the inner conductor adjacent to it respectively. The outer conductors have one end floating and the other end connected to the rest of the converter circuit.

The inter-conductor capacitances and conductor inductances are related to the structure's dimensions and materials through the following well-known equations:

$$L = \frac{N^2}{lc/Ac\mu_c + lg/Ag\mu_o} \quad (1)$$

$$C = A\varepsilon/d \quad (2)$$

Where l_c is the mean path length that magnetic flux would have to flow around the magnetic core. A_c is the mean cross-sectional area of the magnetic core. A_g is the cross-sectional area of the air gaps in the magnetic core: normally fringing is ignored, so A_g is assumed equal to A_c. Equation 2 determines capacitance for an ideal parallel plate capacitor: A is the area of the parallel surface, d is the distance between parallel plates [12]-[17].

In the process of converter design, L and C are usually determined by the required energy flow and then the structure's dimensions are derived. The DC bus capacitors exist to smooth the output (load-side) and input (supply-side) voltages, ensuring a DC-DC topology. The size of the output capacitance depends on the magnitude of ripple voltage that may acceptably appear across it, and the current being drawn by the load. The supply-side capacitor has a different function. The leads coming from the supply voltage source will have a leakage inductance, which can cause high-frequency oscillations to appear in the DC supply signal. The event that excites such oscillations is the switch (MOSFET) turn-off event, where the current in the supply loop is taken to zero very fast. The supply-side capacitor acts as a low pass filter of these oscillations that appear across the supply-side inductor. The cutoff frequency of this filtering effect should be less than the switching frequency. This requirement is what determines the size of the supply-side capacitor.The required inductance of each conductor is determined by the maximum amount of energy that needs to be stored in the magnetic fields during each switching cycle. Once the required L and C are determined, the structure's geometric dimensions and material properties can be chosen to meet those requirements [18].

The operation of the MOSFET makes the nodes between inductor and switch, and between inductor and diode, to be "hot", i.e. to have rapidly changing signals. The nodes on the opposite ends of the inductors are essentially static voltages – i.e. DC. The floating ends of the outer conductors must be arranged on the same side as the hot nodes [19]. The reason for this can be visualized in two ways that will now be discussed.

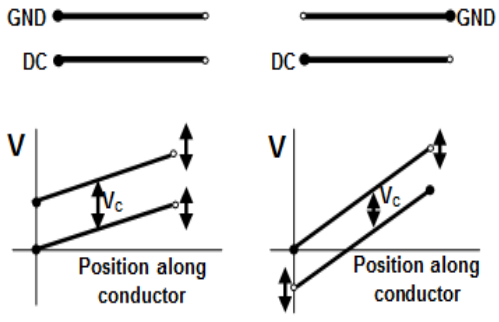

Fig. 6. Voltage profiles along conductors for different connections of integrated DC bus capacitor.

A DC bus capacitor serves as

an energy storage component to provide small energy absorption or release while maintaining a constant voltage.

The voltage is approximately constant because the bulk of the energy stored in the capacitor is constant, small variations are insignificant. The voltage distribution profile diagrams in Figure 6 show how the capacitor energy (proportional to V_C) is constant when the DC node and the ground connection are on the same side, and is varying drastically otherwise. The solid dots represent conductor ends that have a fixed voltage, and the little circles represent conductor ends with varying voltages, hence the arrows on the diagram.

The second visualization method sees any length of conductor as a high impedance path at high frequency (since it is inductive). The DC bus capacitor's function is to sink into the ground some high frequency content appearing at a node which is to hold constant (DC). Therefore, if the ground is connected to the same side as the DC node, any high frequency noise on the DC bus has a minimal inductive conductor to pass through to reach the ground. If connected to the other end, however, high frequency noise has to pass through the full length of the inductive conductors, thus will not be debited readily to the ground. This is illustrated in Figure 7.

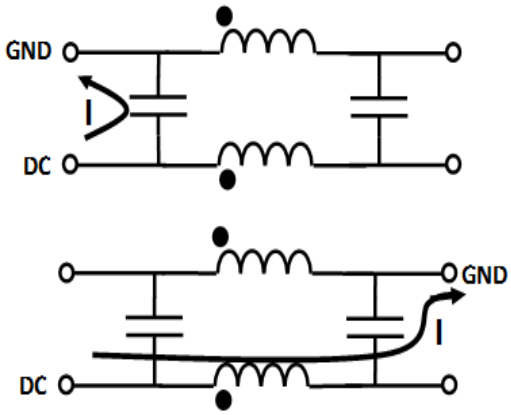

Fig. 7. Path to ground for high frequency content on the DC bus for different connections of integrated capacitor.

The implementation of the interconnections between the passive structure's terminals and the external circuit is also important. The interconnecting conductors should be kept as short as possible to limit layout inductance, and to limit the possibility of unwanted electromagnetic coupling with external circuits. It is therefore advantageous to have both ends of the passive structure's conductors to be close together. To achieve this, as well as to facilitate multiple windings, the planar conductor can be wound around an E-core. The bend in the conductor is ignored; the effect of the portion of the conductors hanging outside the magnetic core is taken as negligible because the energy stored in that portion is very small. For the purpose of this study, the whole winded conductor layer will be treated as a uniform one-dimensional length. This length has a distributed inductance, as well as a distributed capacitance between itself and conductor layers that are immediately adjacent and that have a surface parallel to it.

A concerning phenomenon occurs in the on-cycle of the MOSFET. Figure 8 shows that half-way through the on-cycle oscillations arise across the diode. The oscillations are not being initiated by a switching event, which make it inexplicable. This parasite must be from the numerical solution. Setting the maximum time step lower significantly mitigates this problem, but long simulation times become problematic once the time steps become too small.

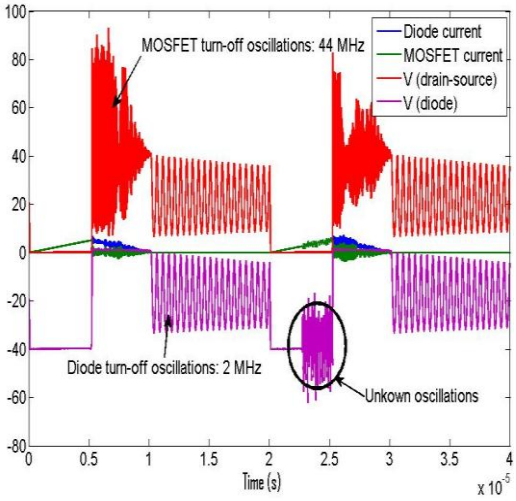

Fig. 8. Flyback simulation with modal decomposition macromodel.

An important observation from Figure 8 is that the simulations using the macromodel have much less damping on both MOSFET and diode turn-off oscillations than in the simulations using lumped elements [20]. The frequency of oscillation is the same as that of the lumped models. The reason for this not well understood. The first thought to come to mind is the lossless nature of the macromodel. However, higher damping is obtained by lumped parameter model even when the lumped resistance is excluded.

Decreasing the maximum time step in the SPICE simulator improves the convergence of the macromodel. Therefore, the inability to converge is arising from a numerical parasitic, which is caused by a sensitivity in the system to round off errors. The main problem with reducing the time step is long simulation times that result. The macromodel was initially preferred because of its fast execution time due to its low number of elements. This advantage is clearly removed by the presence of the parasitic numerical oscillations.

IV. CONVERTER MEASUREMENTS

This section compares measurements made on two physically constructed flyback converter circuits. The first was built using a discrete component architecture, with a wire-wound coupled inductor. The second circuit uses the planar inductor circuit.

A discrete-component flyback converter circuit was constructed. The coupled inductor was constructed using an E30 core, of the 3C30 material, which is standard magnetic material. Ten turns were used to give a magnetising inductance of 17 µH and a leakage inductance of 170 nH. This gives a coupling factor between supply and load side of 0.99. The discrete DC bus capacitors were each 1 mF.

With the same load configuration, the constructed

converter could operate comfortably at a power output of 40 W.

Figure 9: Measured voltages at MOSFET terminals for wire-wound inductor circuit (CH1: $V_{drain-source}$, CH2: $V_{gate-source}$).

The wire-wound coupled inductor was replaced with a planar coupled inductor. A planar E-core was used of dimensions 64mm x 10mm x 50mm. This is a large core and, in terms of spatial usage, this is not an improvement on the wire-wound structure. However, the large core is used to allow the use of only a single turn in the planar case, which simplifies its modelling.

The planar conductors separated by a dielectric material gave an inter-conductor capacitance of 370pF. Impedance measurements indicated a magnetizing inductance of 24 µH and a leakage inductance of 25 nH. This gives a coupling factor of approximately 0.998. This circuit also operated comfortably at an output power of 40 W. The measured waveforms are shown in Figures 11 and 12. One notable feature is that the damping in the planar inductor circuit is significantly greater, which can be observed with a comparison with Figures 9 and 10. The reason for this greater damping is unknown, and can be a subject of interest in future simulation study.

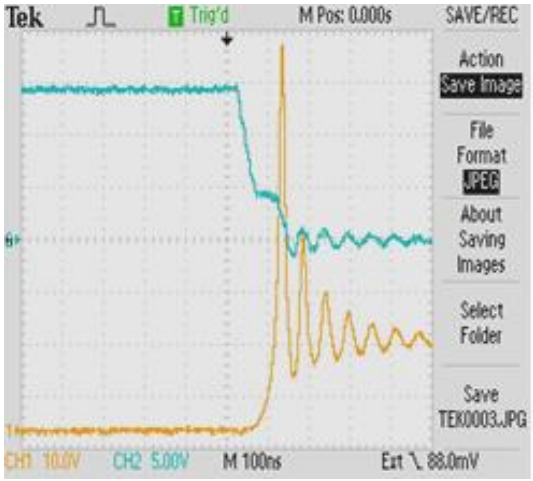

Figure 10: Measured voltages at MOSFET terminals for wire-wound inductor circuit (CH1: Vdrain-source, CH2: Vgate-source)

Figure 11: Measured voltages at MOSFET terminals for planar inductor circuit (CH1: Vdrain-source, CH2: Vgate-source).

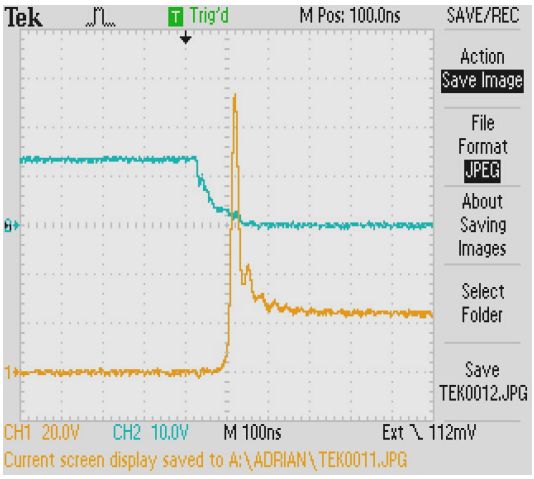

Figure 12: Measured voltages at MOSFET terminals for planar inductor circuit (CH1: Vdrain-source, CH2: Vgate-source)

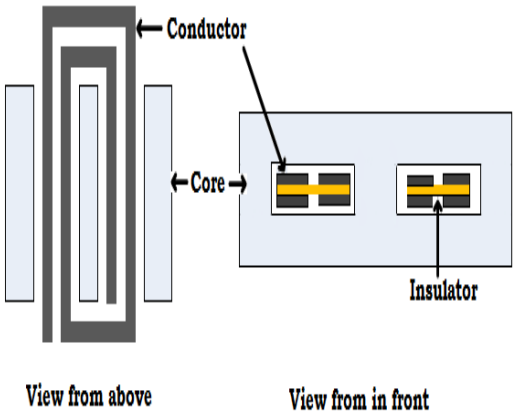

Figure 13: The concept of horizontal windings to increase inductance

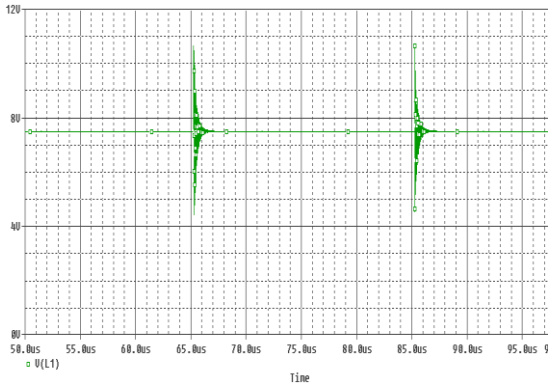

Figure 14: VLoad with an integrated CDC of 2.5 µF, and no external CDC

One objective of using the integrated architecture is to achieve a more compact usage of space. Therefore, the geometrical limit to capacitance is the conductor area (width **x** length); with a further limit of the permittivity of the dielectric. Inductance is limited by the reluctance of the magnetic circuit enclosing it. A core size of 64x10x50 (dimensions in mm) translates into a maximum capacitance of 40 nF, and a maximum inductance of 34 µH. This is not enough for most applications involving a higher power range (i.e. > 40W). A properly functioning DC bus capacitor would need a magnitude of the order of a 1 - 1000 µF, depending on the application of course.

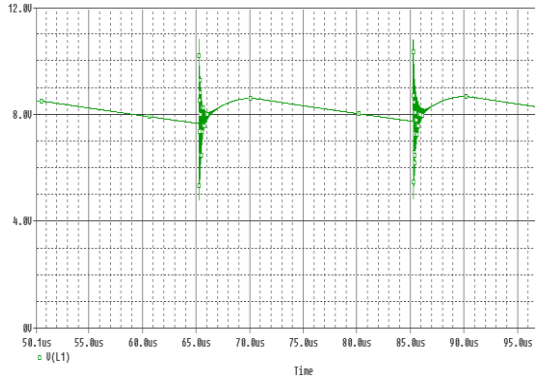

Figure 15: VLoad with an integrated CDC of 2.5µF, and no external CDC

Figures 14 and 15 show the effect of an entirely integrated DC bus capacitor, whose function is to smooth the load voltage into a DC signal. When this capacitance is reduced further, the parasitic oscillations begin to grow in magnitude; but from about 2.5 µF and larger, the parasitic oscillations are not significantly changed. The observed parasitic oscillation is caused by a resonance between the inter-conductor leakage inductance and capacitance.This simulation demonstrates that even for very large integrated capacitance, the filtering effect is limited, i.e. there still exists a parasitic oscillation. This is because of the coexistence of the conductor inductance. Therefore, total integration of the capacitors and inductors does not result in perfect elimination of the problem of a capacitor's ESL.

V. RESULTS AND DISCUSSIONS

The performance of the proposed modelling technique has been validated by simulation. Simulation saves a lot of human effort we can make changes in the circuitry and observe the results thus obtained. Before the implementation step, comprehensive simulations are done to verify the design, also to determine some of the hardware requirements. For example, current ratings of the capacitors, inductors, cables, and so on can be easily determined from the simulation results. For the proposed converter the average value is reduced. Furthermore, it is shown that the magnetizing current becomes negative, thus eliminating the DCM. Note that for the proposed converter for a magnetizing inductance value about lower, the current ripple is higher, thus demonstrating the reduced ripple existing when the two converters employ the same magnetizing inductance value.

VI. CONCLUSIONS

This paper proposes an effective modelling of integrated passive circuits operating in power electronic circuits. Circuit designers would prefer a model that can be interfaced easily with SPICE, because there are many benefits to working in the SPICE environment. SPICE supports good models for semi-conductor devices, which do not easily model from first principles if one was to construct their own circuit simulator. Higher frequencies are involved in the current trend towards fast switching speeds in power electronic circuits. The presence of these frequencies requires a circuit designer to consider the distributed nature of the integrated passive structure. The distributed model for a two-conductor case has been presented; this model is easily extendable to multiple conductors. The solution of this model is not trivial, and there exist several solution methods. The main problem with most of the distributed model's solution methods is that they cannot directly interface with a circuit simulator. This means that the boundary conditions that can be simulated are limited to simple terminal-terminal impedances, and cannot support a complete converter circuit. We also lose the benefit of the SPICE-like environment to switch from time domain to frequency domain.

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