

# THD Analysis of Novel Envelop with a T type (E-T) Multilevel Inverter with reduced number of switches



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**Abstract:** Multilevel inverters are a good choice for medium and low power applications. Multilevel inverters have found a wide place in the market for their good power quality output. This paper proposes a new Envelope with T type Novel Multilevel inverter with unequal sources and with reduced switch count. Working of the circuit is explained. Firing angle calculations are done using simple nested looping technique and later Genetic Algorithm is used to obtain optimum firing angles for Selective Harmonic Elimination technique and improve the THD of the output voltage. Comparison is made between different types of inverters. The proposed inverter can be used for speed control of drives

**Index Terms:** Multilevel Inverter, THD, SHE, GA

## I. INTRODUCTION

Modern day switching has made Inverters into complex circuitry with multiple levels. The overall power ratings of the inverters is improved by individual small powered devices. The unique structure of multilevel inverter (MLI) synthesizes higher voltage levels with lower harmonics, without using transformers or series connected synchronized switching devices. There are mainly three types of Multilevel inverters namely, Neutral point clamped (NPC), Capacitor clamped and Cascaded Multilevel inverter. Neutral point clamped MLI uses voltage clamping diodes. High rated capacitors are connected in series with a neutral point in the middle of the line. Voltage levels are achieved by clamping diodes getting connected to the sources through selected number of switches for every level. In Flying capacitor clamped MLI, capacitors hold the voltages at the desired values. This type of MLI has a number of redundant switching states for the same number of levels. Cascaded MLI uses cascaded full bridge inverter with separate but equal rating DC sources in a modular setup to create a stepped output voltage waveform [1].

Cascaded Multilevel inverters (CMLI) are the most preferred choice among other topologies like neutral point clamped, capacitor clamped because of their ease in control

of switching, quality of output and achieving higher levels by cascading. It is difficult to achieve more than four levels in one quarter of the wave with Capacitor clamped or Neutral point clamped multilevel inverter since the control becomes complicated [2].

Major advantage of CMLI is that, compared to diode clamped and flying capacitor inverters, CMLI requires least number of components to achieve the same or more number of voltage levels. Soft switching can be easily implemented to reduce switching losses and device stresses. Cascaded MLI are used as static VAR compensators, reactive power compensators and used in variable speed drives. Also Cascaded MLI can be used for high voltage and high current output. Since the devices can be switched at lower frequency, the CMLI will have higher efficiency. There is no problem of electromagnetic Interference[1-3]. Continuous improvement has led to a new circuit known as envelope type multi level inverter. An envelope type MLI with 4 sources and 8 switches is explained in [4].

In this paper, a new type of Multilevel inverter is proposed. This inverter uses only 11 switches and 6 sources to obtain 27 level output voltage. Initially firings angles are calculated for uniformly stepped output. An optimization technique, genetic algorithm for Selective Harmonic Elimination (SHE) is used to calculate the optimum firing angle for the least THD in the output. Simulation is done in MATLAB and results with THDs are tabulated.

Fig.1 shows the conventional cascaded multilevel inverter where 2 equal DC voltage sources and 8 switches give a 5 level output [1]. In this method it was shown that by using different combinations of switching sequence, it is possible to connect or disconnect a source to the load and hence achieve a multilevel output. This circuit was modified with unequal sources and a half bridge as in [2]. It is observed that the devices in H-bridge will undergo more stress compared to switches in each half bridge. Uneven stress distribution is observed in the switches since equal numbers of switches are not ON all the time,

Conventional multilevel inverters have evolved into symmetrical or asymmetrical combinational circuits. They are continuously being upgraded into different topologies in order to achieve more output voltage levels and reduced switch count. SHE is explained in [3] and calculation of firing angles for reduced THD is done. Application of GA to SHE is explained in [5].

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Generation of equal step voltage levels, voltage balancing, reducing the number of switches, PSO based SHE, filter design and PWM switching is explained in [6-11]

Fig.2 shows an Envelope type multilevel inverter [4] which gives 13 levels with 8 switches and 4 sources. It can also be seen that only three switches are ON at any level, hence the stress distribution is also uniform.

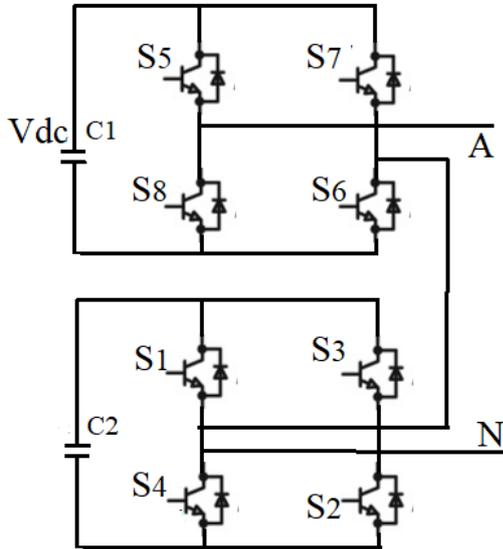


Fig 1. Conventional Multilevel inverter

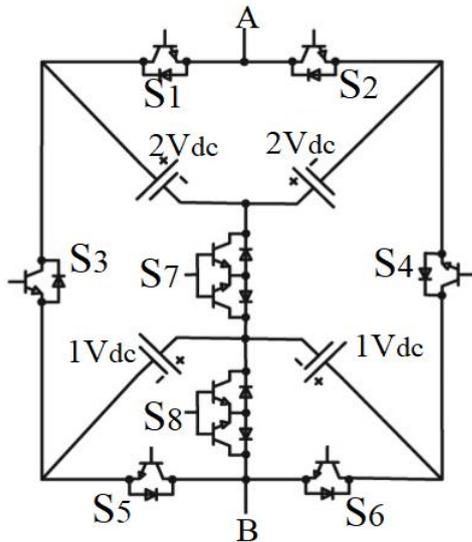


Fig 2. Envelope type Multilevel inverter [4]

II. PROPOSED MULTILEVEL INVERTER

An improvement in the number of levels can be obtained by adding intermediate levels with a ‘T’ circuit to existing ‘E’ type as shown in Fig 3. This topology is proposed as E-T type inverter. The proposed inverter is divided into two parts; one is a regular Envelope Type as in [4] and second is the ‘T’ type to create intermediate levels with 2 sources and 3 switches. This inverter synthesizes 27 levels with only 11 switches and 6 unequal sources. One advantage of this inverter is that only four switches are ON for any level. This implies, at any given time, equal numbers of switches are ON hence the stress on every switch will remain equal. Fig 3a shows the working of the circuit for third level.

The proposed MLI generates 27 levels at 50 Hz as shown in Fig 4. Table I shows the status of switches and output levels. Sources selected are two sources of 24V, two sources are of 48V and two sources are of 96V. A peak value of 312V at 50Hz can be achieved with different combinations of switches. Status 1 means the switch is in ON condition and a status 0 means the switch is in OFF condition.

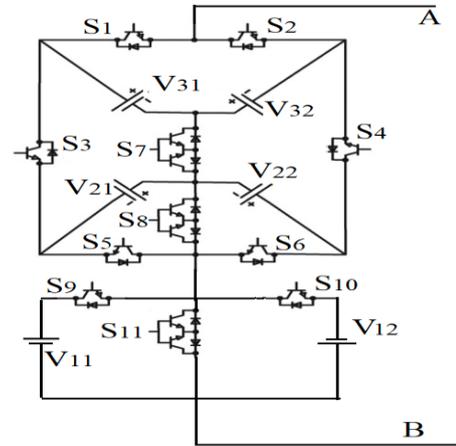


Fig 3. Proposed E-T Multilevel inverter

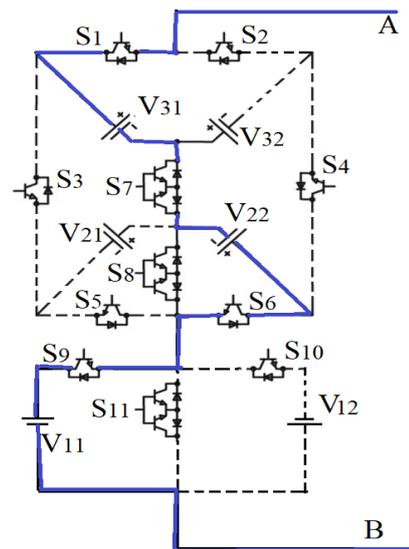


Fig 3a. Working of E-T Multilevel inverter for third level (72V)

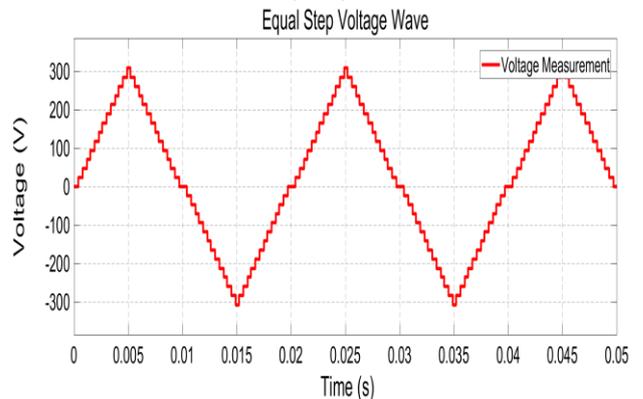


Fig 4. 27 Level output of proposed E-T type Inverter

Table I: Status of switches and output levels

Sl. No	S1	S2	S3	S4	S5	S6	S7	S8	S9	S 10	S 11	V
1	0	0	0	0	0	0	0	0	0	0	0	0
2	1	0	1	0	1	0	0	0	1	0	0	24
3	1	0	0	0	0	1	1	0	0	1	0	48
4	1	0	0	0	0	1	1	0	1	0	0	72
5	1	0	0	0	0	0	1	1	0	1	0	96
6	1	0	0	0	0	0	1	1	1	0	0	120
7	1	0	0	0	1	0	1	0	0	1	0	144
8	1	0	0	0	1	0	1	0	1	0	0	168
9	1	0	0	1	0	1	0	0	0	1	0	192
10	1	0	0	1	0	1	0	0	1	0	0	216
11	1	0	0	1	0	0	0	1	0	1	0	240
12	1	0	0	1	0	0	0	1	1	0	0	264
13	1	0	0	1	1	0	0	0	0	1	0	288
14	1	0	0	1	1	0	0	0	1	0	0	312
15	0	1	0	1	0	1	0	0	0	0	1	-24
16	0	1	0	0	1	0	1	0	0	1	0	-48
17	0	1	0	0	1	0	1	0	0	0	1	-72
18	0	1	0	0	0	0	1	1	0	1	0	-96
19	0	1	0	0	0	0	1	1	0	0	1	-120
20	0	1	0	0	0	1	1	0	0	1	0	-144
21	0	1	0	0	0	1	1	0	0	0	1	-168
22	0	1	1	0	1	0	0	0	0	1	0	-192
23	0	1	1	0	1	0	0	0	0	0	1	-216
24	0	1	1	0	0	0	0	1	0	1	0	-240
25	0	1	1	0	0	0	0	1	0	0	1	-264
26	0	1	1	0	0	1	0	0	0	1	0	-288
27	0	1	1	0	0	1	0	0	0	0	1	-312

The waveform in Fig.4 is considered and an FFT analysis is done in MATLAB. In Fig 5 the FFT window and THD analysis of the proposed novel E-T type MLI is shown. The proposed E-T multilevel inverter was found to have a Total Harmonic Distortion (THD) of 15.22% for a single phase output, which is quite unacceptable in today's context. An attempt is made to reduce the THD by optimizing the firing angles for the Proposed E-T type Inverter by using Selective Harmonic Elimination (SHE) technique.

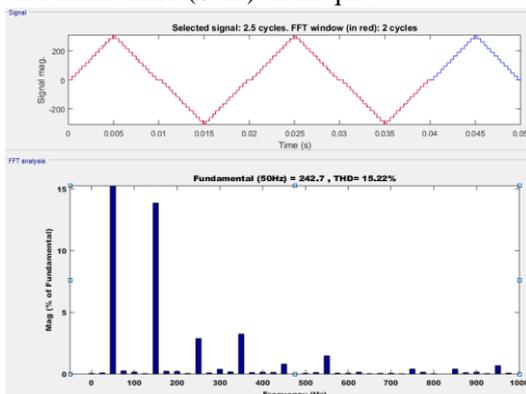


Fig 5. FFT of the proposed MLI with equal step output

### III. METHODOLOGY

Fourier series for any waveform is given by

$$f_k(t) = \frac{a_0}{2} + \sum_{k=0}^{\infty} \left( a_k \cos \left[ \frac{2\pi kt}{T} \right] + b_k \sin \left[ \frac{2\pi kt}{T} \right] \right)$$

As the waveform is symmetrical, even harmonics are zero.  $f_k(t)$ , is available for odd values of k, the equation can be further simplified as

$$f_k(t) = \sum_{k=0}^{\infty} \left( b_k \sin \left[ \frac{2\pi kt}{T} \right] \right)$$

$k=1,3,5,\dots$

Where  $b_k$  is

$$b_k = \frac{4V}{\pi} \sum_{i=1}^{\infty} \sin(k\alpha_i)$$

Modulation index

$$M = \frac{V}{(4nV_{dc})/\pi}$$

Where  $n$  is the number of levels

$V$  is the desired fundamental voltage

$V_{dc}$  is the value of individual voltage source

Selective Harmonic Elimination (SHE) technique is used to lower the odd harmonics, by selecting the suitable values of firing angles from  $\alpha_1$  to  $\alpha_{13}$  to satisfy equation (2) and equation (3).

$$13M = \cos(\alpha_1) + \cos(\alpha_2) + \cos(\alpha_3) + \cos(\alpha_4) + \cos(\alpha_5) + \cos(\alpha_6) + \cos(\alpha_7) + \cos(\alpha_8) + \cos(\alpha_9) + \cos(\alpha_{10}) + \cos(\alpha_{11}) + \cos(\alpha_{12}) + \cos(\alpha_{13}) \quad (1)$$

$$0 = \cos(k\alpha_1) + \cos(k\alpha_2) + \cos(k\alpha_3) + \cos(k\alpha_4) + \cos(k\alpha_5) + \cos(k\alpha_6) + \cos(k\alpha_7) + \cos(k\alpha_8) + \cos(k\alpha_9) + \cos(k\alpha_{10}) + \cos(k\alpha_{11}) + \cos(k\alpha_{12}) + \cos(k\alpha_{13})$$

For  $k = 3, 5, 7, \dots, 27$

$$\alpha_1 < \alpha_2 < \alpha_3 < \alpha_4 < \alpha_5 < \alpha_6 < \alpha_7 < \alpha_8 < \alpha_9 < \alpha_{10} < \alpha_{11} < \alpha_{12} < \alpha_{13} < 90^\circ \quad (2)$$

$$\alpha_{11} < \alpha_{12} < \alpha_{13} < 90^\circ \quad (3)$$

$$THD = \frac{\left( \sqrt{\sum_{n=3,5,7}^{27} \frac{1}{n} \sum_{k=1}^{13} ((\cos n\alpha_k)^2)} \right)}{\sum_{k=1}^{13} \cos(\alpha_k)} \quad (4)$$

A MATLAB program is written to create a number of feasible firing angles to reduce the THD. These firing angles are vectors  $\alpha_1$  to  $\alpha_{13}$  corresponding to 13 firing angles  $\alpha_1$  to  $\alpha_{13}$  are vectors of 10X1 feasible firing angles for every voltage level. The optimum firing angles from the feasible set is selected such that the selected firing angles are less than 90 degrees and using the property of quarter wave symmetry of the expected output.

The program is divided into two parts to calculate the firing angle. First section is used to calculate the initial set of firing angles using nested loops and the second section is used to obtain the optimum value of firing angle using Genetic Algorithm function  $ga()$  available in MATLAB to optimize the firing angles obtained in first section.

In nested Looping method, 13 arrays corresponding to required 13 firing angles are created. Each array is a matrix of size 10X1. Using  $linspace()$  function in MATLAB, array of 10 equally spaced values are created. The range of values can be decided because, between 0 and 90 degrees, 13 angles are to be created.  $90/13$  is approximately 7 degrees. Thus the range can vary between 10% of 7 degrees to 90% of 7 degrees. Advantage of this method is number of equally spaced values can be changed as well as percentage of variation of angle can be changed according to users choice, convenience and available time for convergence. Overlapping of angles can be avoided so that the number of steps can be maintained at desired 27 levels.

After the arrays of firing angles are created, one value from each array is considered and with if loops in the program having conditional statements as in equation 2 is verified. If the condition is true, then it calculates the fundamental output voltage. If the condition is not true, it considers the next set of firing angles and repeats the procedure. The combination of firing angles corresponding to highest value of fundamental voltage is selected as the most feasible firing angles. Using Microsoft Excel the next set of angles from 90 degrees to 360 degrees are calculated and converted to corresponding time domain. It is placed in the MATLAB-simulink file with the circuit to calculate the THD of the wave.

It was observed that the values corresponding to highest

Modulation Index did not give least THD. Thus the combinations of firing angles are so chosen to give least THD with a reasonable Modulation Index.

These feasible firing angles become the initial solution for the Genetic Algorithm  $ga()$  available in MATLAB. Choosing the proper initial firing angles will lead to better and faster solution in Genetic Algorithm.

**A. Algorithm for MATLAB program: Nested Looping method**

- Create an array of firing angles for  $\alpha_1$  to  $\alpha_{13}$ .
- Using nested if loop, search for the combinations of firing angles which gives highest value in equation (1) and satisfies equation (2) for all values of  $k$ .
- Calculate the THD for different firing angles using MATLAB FFT tool.
- Output the result as an array of most suitable array of firing angles that satisfies the equation (1) to (3) with least THD.

**B. Steps for Genetic Algorithm  $ga()$  function in MATLAB**

- Use the results of MATLAB program by Nested Looping method as the initial guess for the array of angles.
- Number of variables = 13, since 13 firing angles are required.
- Fitness Function is implemented for THD expression as in equation (4).
- Variables A, B equalities and inequalities of  $ga()$  are left as empty arrays.
- Inequalities of variable C in  $ga()$  is set as equation (3).
- Equalities of variable C in  $ga()$  is set as equation (2).
- Lower bound and Upper bound values in  $ga()$  for the required firing angles are carefully set so that there are no stray values and GA converges faster.

Table II shows the practical values chosen for batteries and load. These values are set in MATLAB software to evaluate the overall performance of the inverter.

Table II: Practical values considered for batteries, switches and load as parameters for simulation.

Sl. No	Device	Parameters
<b>Battery</b>		
1	V11 and V12	24V
2	V21 and V22	48V
3	V31 and V32	96V
<b>MOSFET - R6012JNJ</b>		
4	Voltage rating	600V
5	Current rating	12A
6	Power rating	160W
7	FET on state Resistance	0.39Ω
8	Internal Diode Inductance	0 H
9	Internal Diode Resistance	1.11Ω
10	Diode forward voltage	0.7 V
11	Snubber resistance $R_s$	10E5 Ω
12	Snubber capacitance $C_s$	Infinity
<b>LOAD- resistance</b>		
13	Voltage	300V
14	Wattage	900W
15	Resistance	100 Ω



IV. MATLAB SIMULATION

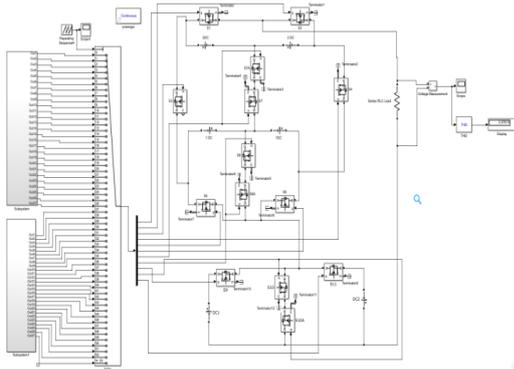


Fig 6. Proposed E-T type Inverter in MATLAB

MATLAB-Simulink is used for simulation. MOSFET - R6012JNJ has characteristics of fast switching and is easily available. MATLAB simulation circuit is as shown in Fig 6 for the proposed E-T type Multilevel inverter. Practical values of sources, switches and load is considered as shown in Table III. The gating signals are generated in the subsystem using a constant value generator with zeros and ones corresponding to switch state. The subsystem is connected to a multiport switch along with a repeating sequence generator. The inputs to the repeating sequence generator are the firing angles converted to time scale for 54 output values corresponding to 2ms.

V. RESULTS

MATLAB simulation for programmed firing angles is shown in Fig.7 and its THD is shown in Fig 8. It is observed that there is an improvement in the THD of the output compared to equal step output. To further improve the THD, Selective Harmonic Elimination is used by adopting Genetic Algorithm. MATLAB simulation results for SHE using Genetic Algorithm with 27 level output waveform is shown in Fig 9, and its THD is calculated and shown in the FFT window of MATLAB as in Fig 10.

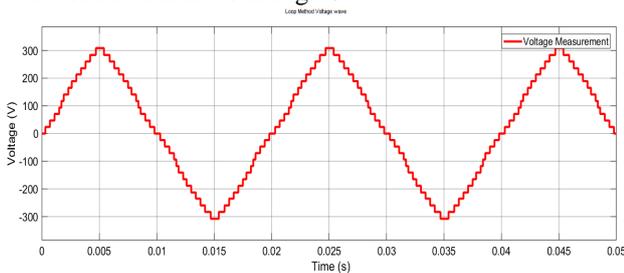


Fig 7. 27 level output E-T type MLI using looping

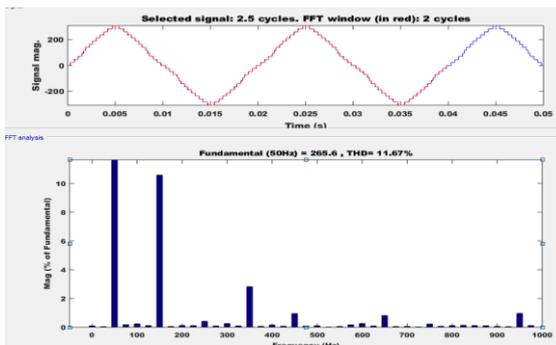


Fig.8. FFT of the E-T type MLI with looping method

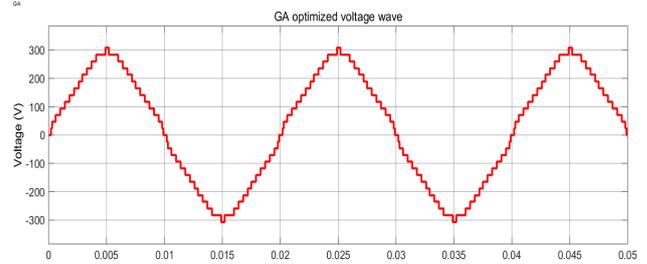


Fig 9. 27 level output E-T type MLI with SHE using GA

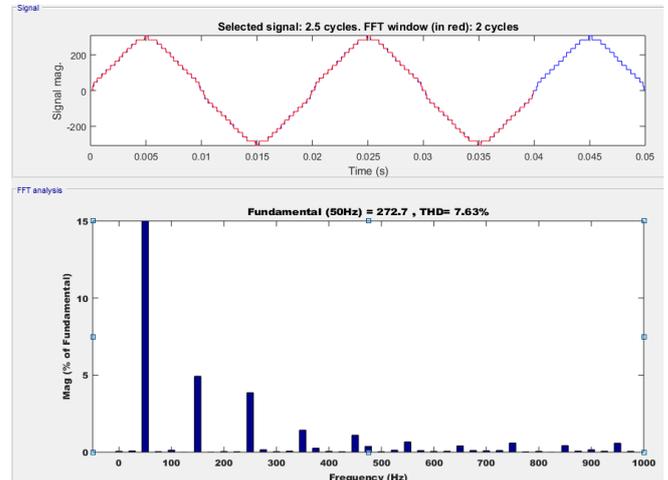


Fig 10. FFT of the E-T type MLI with GA

Optimum Firing angles and THD obtained are as shown in Table III. Equal step refers to firing angles at equal intervals. It is observed that as the firing angles are optimized, THD is improved in every stage.

Table III: Optimized firing angles.

	MATLAB Programs		
	Equal step method	Nested Looping Method	SHE with GA optimization
	Angle in Degrees	Angle in Degrees	Angle in Degrees
a1	3.461516	4.497708	3.598167
a2	10.38541	11.76853	3.632544
a3	17.3077	18.68984	10.55959
a4	24.23079	25.61688	17.4809
a5	31.15382	30.34377	24.40222
a6	38.07691	32.88197	31.32926
a7	45	39.80901	38.25057
a8	51.92762	46.73033	45.17189
a9	58.84618	53.65164	52.0932
a10	65.76921	60.22918	59.02024
a11	72.6923	67.5	65.94156
a12	79.61539	74.42131	72.86287
a13	86.53848	84.45951	86.67685
<b>THD (%)</b>	<b>15.22</b>	<b>11.63</b>	<b>7.63</b>

Results of all the three types of waveforms are shown in Table IV. It is observed that as the THD is reduced and the Fundamental voltage peak is also improved.

**Table IV: Comparison of THDs in different techniques**

	Frequency (Hz)	Fundamental Voltage (Volts)	THD (%)
Equal Step	50	242.7	15.22
Nested Looping Method	50	265.6	11.63
GA	50	272.7	7.63

**VI. CONCLUSION**

The proposed E-T type inverter is compared with conventional and E type inverter. It is observed that with an additional auxiliary circuit, intermediate levels can be generated which increases the number of voltage levels. Hence the number of voltage levels is double the E type inverter [4]. Table V shows the comparison of different multilevel inverters. It is seen that the proposed E-T type MLI uses least number of switches and sources to generate higher number of voltage levels.

**Table V: Comparison of Proposed E-T type Multilevel inverter with various inverters.**

Type of circuit	Number of DC Sources	Number of Switches	Number of output voltage levels
Conventional MLI	13	52	27
Envelope Type	8	16	25
Proposed E-T Type	6	11	27

It can be concluded that the proposed E-T Type inverter circuit uses less number of semiconductor switches compared to previous circuits. The stress on each switch is equal at all levels. The optimum firing angles were calculated for the inverter switches using Genetic Algorithm to apply Selective Harmonic Elimination technique. In this method, the number of voltage levels has increased and the THD values have comparatively improved. MATLAB program for Nested Looping method creates a number of feasible firing angles. The solution from the nested Looping method can be used as initial guess values in Genetic Algorithm which helps it to converge faster. This way the random values as initial guess for GA can be avoided. Though Selective Harmonic Elimination technique is used, the significant harmonics like third and fifth may not be completely zero, since large numbers of variables are involved. The triplen harmonics (those which are multiples of 3) will further be reduced in a three phase network. The proposed E-T type inverter can be used to synthesize three phase waveform also and can be used to control the speed of a 3 phase induction motor.

**REFERENCES**

1. J.-S. Lai and F. Z. Peng, "Multilevel converters-a new breed of power converters," IEEE Transactions on industry applications, vol. 32, pp. 509-517, 1996.
2. Rashmy Deepak, Dr B R Lakshmikantha, Dr. Y R Manjunatha , Vishnu S Kasturi, Lepakshi Sarkar, " Novel Multilevel Inverter with reduced number of switches and Batteries", IEEE Conference , CCUBE 2013.
3. P Mamatha, Challa Venkatesh, "Performance Improved Multilevel Inverter with Selective Harmonic Elimination", 2017 International Conference on Recent Trends in Electrical, Electronics and Computing Technologies.
4. Emad Samadaei, Sayyed Asghar Gholamian, Abdolreza Sheikholeslami, and Jafar Adabi, " An Envelope Type (E-Type)

Module: Asymmetric Multilevel Inverters With Reduced Components " ,IEEE Transactions on Industrial Electronics, Vol. 63, No. 11, November 2016

5. Aniruddho Chatterjee, Adarsh Rastogi, Rajat Rastogi, Ajay Saini, Sarat Kumar Sahoo , "Selective Harmonic Elimination of Cascaded H-Bridge Multilevel Inverter using Genetic Algorithm", International Conference on Innovations in Power and Advanced Computing Technologies [i-PACT2017]
6. N.Vinoth kumar, V.Kumar Chinnaiyan, Pradish.M, MS Divekar, "Enhanced Power Quality of MLI using PSO based Selective Harmonic Elimination", 2015 International Conference on Green Computing and Internet of Things (ICGCIoT)
7. Manjunatha. Y.R. Dr. M. Y.Sanavullah "Generation of Equal Step Multilevel Inverter Output Using Two Unequal Batteries" International Journal of Electrical and power engineering Vol. I No. (2) 2007, pp-206-209.
8. D. A. Ruiz-Caballero, R. M. Ramos-Astudillo, S. A. Mussa, and M. L. Heldwein, "Symmetrical Hybrid Multilevel DC-AC Converters With Reduced Number of Insulated DC Supplies," IEEE Transactions on Industrial Electronics, vol. 57, pp. 2307-2314, 2010.
9. R. Ramos and D. Ruiz-Caballero, "New Symmetrical Hybrid Multilevel DC-AC Converters–Single-Phase Circuits," 9th Brazilian Power Electronics Conference, 2007, pp. 511-516.
10. F. Z. Peng, "A generalized multilevel inverter topology with self voltage balancing," IEEE Transactions on Industry Applications, vol. 37, pp. 611-618, 2001.
11. Rashmy Deepak, Sandeep M P, "Harmonic Analysis & Filter Design for a Novel Multilevel Inverter", International Electrical Engineering Journal (IEEJ) ,Vol. 7 (2016) No.5, pp. 2259-2265 ISSN 2078-2365

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