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Single Stage 180nm CMOS Low Noise Amplifier Topologies and Optimization Algorithms for S Band Frequency

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Abstract*: Low Noise Amplifier (LNA) plays an important role in radio receivers. It mainly determines the system noise and intermodulation behavior of overall receiver. LNA design is more challenging as it requires high gain, low noise figure, good input and output matching and unconditional stability. Further, designing a Low noise Amplifier requires active device selection, amplifier topology, optimization algorithms for superlative results. Hence this paper presents performance analysis of CMOS LNA based on different topologies and optimization algorithms for 180nm RF CMOS design in S band frequency. Here the best results, various limitations in each topology are reviewed and required specifications are determined in each designing. Further this best topology is used for designing LNA circuit which could be used in Indian Regional Navigation Satellite System (IRNSS) applications in dual band frequency.

Keywords* : Low Noise Amplifier (LNA), CMOS, Radio frequency (RF), Noise Figure, Gain, Stability ,IRNSS.

I. INTRODUCTION

In recent modernized technologies mobile cellular, WLANs rules the entire universe. The delicacy of any receiver circuit is very critical as they are designed using RF components like antennas, filter circuits, low noise amplifier, mixers and converters. In radio receiver Low Noise Amplifier (LNA) designing is a challenging aspect as its design is very critical with high density integration. In general an amplifier increases both signal and noise at its input. The noise obtained from outside signal gets added with the inbuilt noise of the amplifier. This leads to decrease in SNR ratio at the output of the amplifier as shown in the equation (1).

$$SNR = \frac{Gain * Signal\ power}{Gain * Noise\ power + Amplifier\ Noise} \quad (1)$$

This SNR value degrades the performance of amplifier in the receiver circuit. In general the noise from the transmitted signal cannot be minimized effectively but the noise which is inbuilt in the device can be turn down. Hence an amplifier circuit (LNA) is designed to provide minimum noise. LNA mainly amplifies very low power signal with remarkably not reducing the SNR ratio. The basic requirements of LNA are to minimize the noise coming from the device, provide high Linearity, very low power consumption, maximum Gain and matching. The main aim of Low noise amplifiers are to amplify the signal obtained from antenna as they are placed very close to the detection device and also reduce the noises. LNAs are widely used in applications such as ISM radios, cellular and PCS handsets, WLANs, GPS receivers, cordless phones and automotive remote keyless entry devices. The amplifier boosts the antenna signal in order to compensate for the feed line losses going from the antenna to the receiver. Here the Low Noise Amplifier (LNA) design is reviewed based on various topologies for 180nm RF CMOS technology. This survey is mainly done to determine which techniques would be useful for designing LNA that could be used in space applications.

This paper is organized as follows. Section II provides LNA specifications such as active device simulation, LNA parameters and different topologies. Section III discusses about the literature survey based on different topologies and different optimization algorithms. Finally section IV presents the conclusion.

II. LNA SPECIFICATIONS

Device performance and its limitations, amplifier topologies, CAD design tools, Environmental impacts and testing techniques are the main aspects to be considered in order to design a perfect amplifier circuit. Here LNA specifications are mainly targeted on different topologies, LNA parameters and the active device simulation. Basically LNAs are designed using various techniques such as single ended, resistive termination, Differential, Balanced, Cascode topology, feedback topology, and gm boosted topologies.LNA parameters to be calculated are Gain, Noise figure, input and output reflection coefficient, Linearity, Stability factor, reverse isolation factor and power consumption. The third important specification is the active device selection where generally CMOS, SiGe HBT, GaAs/InP HBT, MESFET, HEMT devices are considered.

III. LITERAURE SURVEY

It is very essential to study the existing techniques proposed by various researchers in respective fields.

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A literature review is done on LNA designing using different topologies and optimization algorithms to design a perfect 180nm RF CMOS LNA. Review is carried out by considering various research works on 180nm technology and tabulation is provided with the LNA parameters determined in each designing. The following literature review discusses all the different techniques.

A. Based on Topologies

Single-stage Cascode low noise amplifier (LNA) is proposed in [1] for S-band frequency specifically for cryogenic applications. In this paper, the LNA design has been realized with UMC 180 nm technology considering cryogenic environment conditions. This LNA achieves power gain of 15.8 dB , +2 dBm IIP3, and 1.6 dB noise figure (NF) at 2.075 GHz providing 7.66 mA current from a 1.8 V supply.

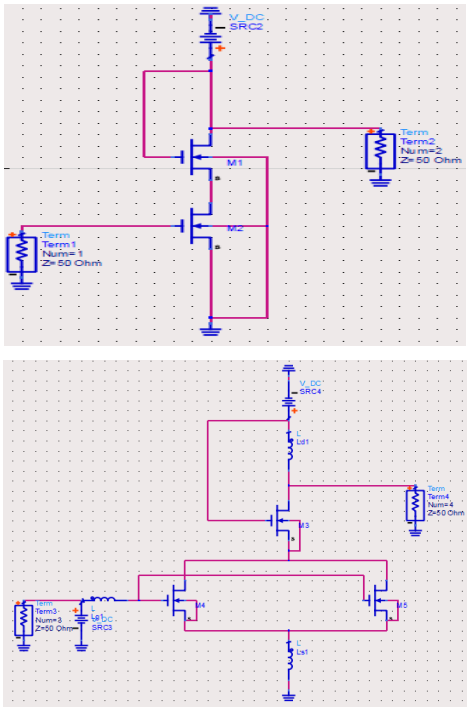

Fig. 1. (a) Basic Cascode topology, (b) Modified Cascode topology [2].

Comparison between basic Cascode and modified Cascode topology as shown in figure 1(a) and 1(b) are proposed in [2]. Basic cascode topology provides high performances due to the common source stage in it, but it reduces the noise figure parameter in LNA. Hence a modified cascode topology is designed in this paper by adding additional transistor to the common source stage. This modified cascode LNA provides 10% high gain and low NF than basic cascode design. It provides19.2 dB gain and 0.416 dB NF at 2.4 GHz.

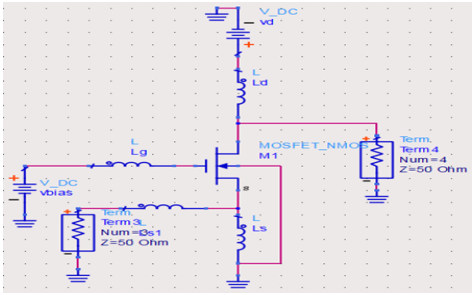

Fig. 2. Common Gate Topology

Common Gate LNA (CGLNA) as shown in figure 2 bestows wideband input matching. This topology is mainly considered for better impedance matching and more desirable gain. CGLNA has a major drawback of larger Noise Figure and unstable linearity. This could be overcome with the help of differential ended method as proposed in [3] where capacitor cross coupled technique is used for providing minimum noise figure with better linearity performance. The common-gate LNA provides larger bandwidth and are often used in high-frequency application.

A common-gate (CG) amplifier with transconductance nonlinearity cancellation technique is employed in [6] which are mainly used for wideband applications. CGLNA are mainly considered for its attractive isolation and impedance matching features. Linearity issues are the major drawback of CGLNAs which is mainly caused due to the transconductance in the transistors. Hence usage of multigate transistor, feedback techniques is employed in common gate design to overcome its limitations.

A CS-CS Current reuse LNA [4] is proposed. This proposed work involves the design of LNA with common source topology with current reuse technique as shown in fig 3. Current reuse structure mainly achieves maximum gain with minimum power consumption. This technique is carried out using cascaded LNA where the second stage reuses the bias current of the first stage to save power.

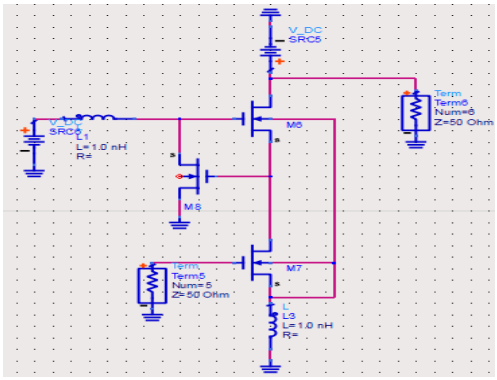

Fig. 3. Current reuse Topology

A Unique dual band concurrent fully integrated LNA with current reuse topology is proposed [10]. Concurrent LNAs are provided as they achieve narrowband gain and matching at multiple frequencies. The current reuse topology adopted here has two stage cascade amplifier where the first stage is CS amplifier and cascode amplifier as the second stage which eliminates the miller effect and provides a better isolation from output signal.

High gain and better noise performance are achieved by Common Source (CS) stage inductive degeneration topology as shown in fig 4 is proposed in [5]. In general this topology is mainly considered attractive and highly efficient as it provides proper matching, higher gain and lowest Noise Figure when compared with other topologies. But it provides certain failures which could be overcome by Differential ended method. Reduction in input noise is the most explicit property of differential operation. This method rejects common mode noise components and it is very less sensitive to the gate induced current noise.

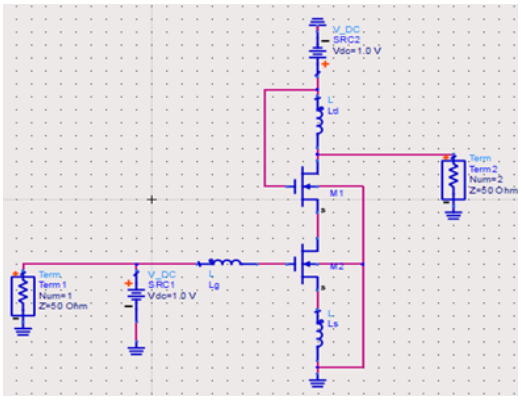

Fig. 4. CS Inductive degeneration Topology

Design of two different LNA's is proposed for WiMax applications [7]. Cascode common source (CS) amplifier and shunt feedback topology as shown in fig 5 is adapted in this paper. Common source amplifier is proposed using cascode topology which is mainly used since it provides higher gain due to its increase in output impedance. Feedback LNA is designed using shunt feedback topology which has various benefits as it provides very high linearity and it could be a great choice in wide band application. But shunt feedback topology is not considered when compared with CS cascode topology because it provides higher noise figure.

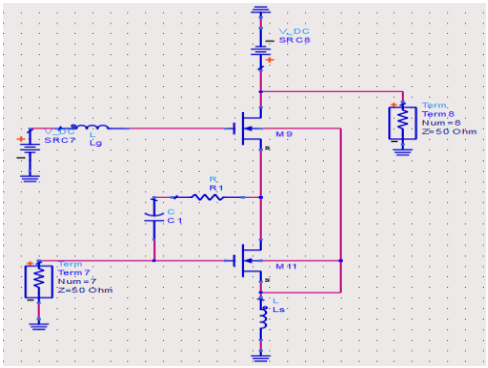

Fig. 5. Shunt Feedback Topology

Low Noise Amplifier for WLAN front end applications using enhancement mode technology has been proposed [8]. This design adopts feedback and balanced topology. Feedback topologies are mainly used to overcome input matching network problem as it fails to achieve minimum VSWR and low noise figure concurrently. Hence feedback techniques solve these problems by inserting modest value of inductor to the ground. Balanced topology as shown in fig 6 is adopted to provide better stability and meet failures in return loss specifications due to large mismatch on the input and output.

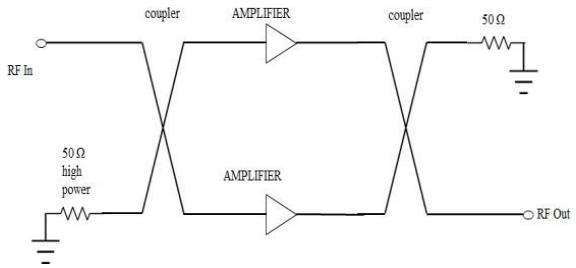

Fig. 6. Balanced Topology

An Inductorless wideband LNA for software defined radio is presented [9]. Shunt–shunt LNA with active feedback technique is adopted for first stage and CS amplifier as digitally tunable variable gain reconfigurable second stage. This proposed circuit provides better bandwidth and high gain performance. Variable gain remains challenging to be achievable in feedback amplifier without disturbing its input matching. Hence digitally tunable second stage is mainly adapted to provide variable gain to maintain linearity in the design.

B. Based on Algorithms

This performance analysis is carried out on the designs where different optimization algorithms are implemented. Various algorithms like particle swarm optimization, noise cancellation technique, geometric programming (GP) method and NSGA-II algorithms are been reviewed.

- Fabrication of inductorless LNA with Noise Cancellation technique is proposed [12]. In this proposal a cascode topology is used where Common source amplifier is followed by CG amplifier. CS stage is mainly used as it provides higher gain and CG path is adopted for better input impedance matching. Here this CG path contributes enough noise in the circuit, thus noise cancellation technique is used to reduce noise contributed by CG path.
- Low Noise Amplifier design with Inductive source degeneration topology with Particle swarm optimization technique is proposed [13]. This technique is an iteration process where multiple candidate solutions will be taken and each will be considered as a separate particle. Each particle has its own position and velocity, thus at each iteration the particle updates its position and velocity. This LNA design provides a gain of 32 dB with 0.52 Noise Figure.
- A Convex optimization approach is proposed [14] for designing LNA in deep submicron CMOS process. CS with inductive source degeneration topology is employed with convex optimization method (a form of geometric programming). This optimization method is employed to reduce the noise figure in the design. It mainly concentrates on the short channel effects such as excess thermal noise and this optimization procedure will perform optimal selection of device parameters.
- A design and optimization of LNA for wireless applications is proposed [15] where Elitist Non- Dominated Sorting Genetic Algorithm [NSGA-II] is been used to determine various values of components in the design. This optimization genetic algorithm is used over single ended LNA where it provides different parameters like isolation probability, population size, crossover probability and number of generations.
- Narrowband LNA in 180nm CMOS technology using Simulated Annealing algorithm with cross over operator is proposed [16].This method uses simulated annealing algorithm which reduces local minimums by saving promising solutions of each design. Low Noise Amplifier design on 180nm CMOS technology with close to 1.8 V power supply mainly targeted for 1-3 GHz frequency range is considered here. Different topologies and optimization algorithms were compared to provide results for the given specifications.

Table I: 180NM CMOS LNA based on Topologies.

Ref	Year	Freq (GHz)	Topology	Gain (S21) dB	NF (dB)	Power Supply (V)	IIP3 (dBm)	S11	S22
1	2017	2.075	Basic cascode Topology	15.8	1.6	1.8	2	−19.2	−21.7
2	2016	3	Modified Cascode Topology	19.2	0.416	1.8	-8.42	-13.74	-0.87
3	2017	1.6	Capacitor cross coupled Common Gate topology	19.5	2.1	2.2	8.3	<-10	NA
4	2015	5.4	CS-CS current reuse technique	12.554	0.423	1.2	NA	-23.847	-17.479
5	2015	1.6	Inductive Degeneration Topology	19	1.1571	1	NA	- 13.152	NA
6	2009	2.4	Common Gate Topology with Noise Cancellation Techniques	10	4	1.8	OIP3= 2 6.5	NA	NA
7	2013	5.9	Cascode CS Topology	15.7	1.85	1	-5.5	-9.5	-14.4
			Shunt Feedback Topology	19.9	2.63	1	-5	-11.2	-22.8
8	2012	2.4	Feedback Topology	10.024	1.53	5	28.07	-14.757	-17.093
			Balanced Topology	17.112	0.846	5	NA	-30.412	-30.679
9	2010	2	Shunt-shunt LNA with active feedback Topology	16	3.5-4.5	1.8	NA	NA	NA
10	2010	2.4	Current Reuse Topology	21	2.5	1.8	NA	-12.7	-12.7

Table II: 180NM CMOS LNA based on Algorithms

Ref	Year	Freq (GHz)	Topology	Algorithms/ Methods	Gain (S21) dB	NF (dB)	Power Supply (V)	IIP3 (dBm)	S11	S22
12	2017	0.1-1.8 GHz	Cascode Topology	Noise Cancellation Technique	14.5	3.0-3.8	1.8	0.25	<-7.8	NA

13	2016	2.4 GHz	Cascode Inductive source degeneration topology	Particle Swarm Optimization	32	0.52	1.8	-14.7	-14.63	-11.55
14	2015	4 GHz	Common Source Inductive source degeneration topology	Geometric programming (GP) optimization method	10	0.8229	2	NA	NA	NA
15	2014	3-5GHz	Cascode LNA with inductive source degeneration	Elitist Non-Dominated Sorting Genetic Algorithm (NSGA-II)	14.49	1.897	1.8	NA	NA	NA
16	2013	2.45 GHz	Cascode topology LNA with inductive degeneration	Simulated Annealing algorithm and an automatic weight adjustment technique	13.6	1.95	1.8	-10.5	-17	-12

Based on the survey regarding topologies and algorithms , Table I and Table II provides the consolidated comparative values and provide us the different LNA parameters values such as Gain, Noise Figure, return loss while applying different topologies and algorithms having 180nm CMOS technology as common value. Here Figure 7 provides the Gain and Noise Figure outcome for the discussed topologies and algorithms.

The graph is constructed by reading Gain and Noise Figure (NF) results of various topologies from Table I and II. The X axis of the graph represents different topologies and Y axis shows Gain and NF in dB range. Performance analysis of topologies and optimization algorithms are analyzed where Cascode inductive source degeneration technique provides a high gain of >30 dB and noise figure of < 1 dB. Common gate topology provides reasonable gain around 20 dB with a drawback of > 3 dB noise figure. Even common gate provides linearity issues which could be overcome by feedback topologies. Feedback topology is used to provide high linearity and better NF values as mentioned in the above graph. Optimization of CMOS LNA for minimizing the noise figure is analyzed here. Quality factor and impedance matching circuits are mainly considered for optimization methods. The NF values in the graph from [13] to [16] references in y axis shows better results more or less equal to 1 dB which is achieved by considering various iteration values which improves the LNA specifications. Hence concluding Cascode Inductive source degeneration topology with particle swarm optimization algorithm is best suited for 180nm CMOS technology for L and S band Frequency.

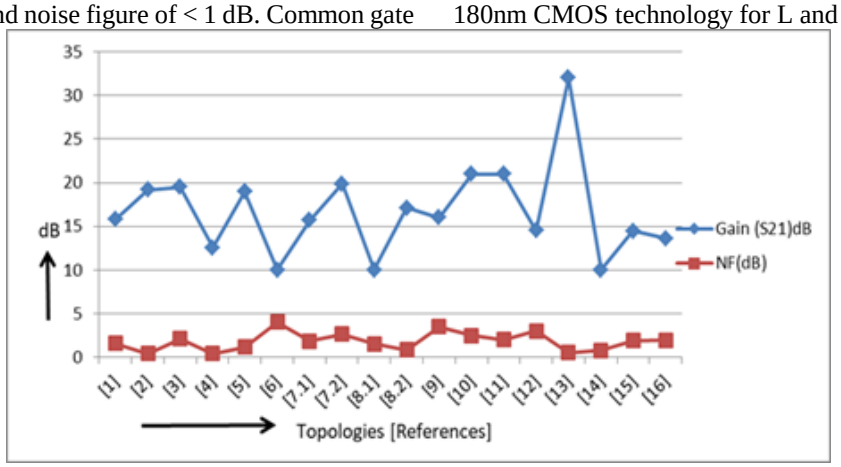

Fig. 7. Gain and Noise Figure results of different topologies and Algorithms

IV. CONCLUSION

Low Noise Amplifier (LNA) is reviewed based on different topologies, its performance and limitations. Analysis based on Cascode topology, current reuse technique, Cascode inductive source degeneration topology, feedback technique and balanced technique is performed.

This analysis mainly focuses on 180nm CMOS technology and performance of each topology is elaborated. Various optimization algorithms for better results are also been reviewed. Hence by concluding Cascode inductive source degeneration topology remains most effective to provide higher Gain, lowest Noise Figure and best matching results for this 180nm CMOS technology at S band frequency and particle swarm optimization technique remains best for this technology. Further this topology and algorithm may be used to design LNA circuit for dual band frequency.

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