Low Power, High Speed and Low Area of Fin FET 4:1 Multiplexer VLSI Circuit Design in 18nm Technology

Sudhakar Alluri, N.S.S.Reddy, B.Rajendra Naik

Abstract: In this paper, a Fin FET 4:1 Multiplexer utilizing 24 transistors has been proposed. The proposed Fin FET 24T 4:1 Multiplexer is developed utilizing in Cadence 18 nm innovation. The proposed outcomes are contrasted and the prior real structure. We have diminished two transistors by utilizing Morgan’s laws contrasted and the prior real plan. Customary of Fin FET 4:1 Multiplexer utilizing 26 transistors as far as power, postponement and zone. It is played out the Dynamic power is diminished by 47.77%, Leakage Power is diminished 29.09% and Static Power is diminished by 14.61%. It is likewise understood that the postponement is diminished by 94.13% and territory is diminished by 40.74% for 24 transistors Fin FET 4:1 Multiplexer in Cadence 18nm Technology.

Keywords: Fin FET 4:1 Multiplexer, fast, low power and Low zone, VLSI, DSP.

I. INTRODUCTION

The underlying periods of innovative work endeavors in VLSI configuration were situated towards accomplishing rapid and scaling down. At present, the developing patterns in versatile reckoning and remote applications request the necessity to lookout new advances and configuration circuits that expend low power. this needs the necessity to rearrange the exploration towards drop-off power spread in VLSI circuits. Late patterns within the development and advancement of battery management led versatile and moveable reckoning gadgets need the necessity for extended battery life and after lesser battery control consumption[1].

The battery life is to boot cut by the use of quick processors and large recollections in them. Likewise, the greatness of intensity scattering per unit territory within the incorporated circuits of gift day chip and recollections ar quickly increasing due to the enlarged speed and flexibility. This declines the problem of heat evacuation and cooling (Kaushik Roy 2000)[2].

In this work is planned as look for when category II these days Literature study on Fin FET 4:1 electronic device class III these days the philosophy for Fin FET 4:1 electronic device and moreover talked regarding the High speed, low power and low zone. Classification IV demonstrates the reenactment results and that they ar processed clearly, when the work is closed with category V.

II. LITERATURE REVIEW

Data-paths of various bit-widths square measure of needed in terribly giant scale integrated (VLSI) circuits from processors to application specific integrated circuits (ASICs). The performance of microprocessors and computers heavily depends upon the performance of the varied data-paths used. Such information methods embrace information registers that hold operands and results and combinative logic units that manipulate and method information values [3], [4]. numerous combinative logic units square measure adder, multiplier, divider, barrel shifter and arithmetic logic unit (ALU) circuits. the choice of a specific data-path depends upon the progressive in digital style. the foremost necessary and wide accepted metrics for measuring the standard of data-path styles square measure propagation delay, space and power [5], [6]. Minimizing space and delay has continually been necessary, however reducing power consumption has additionally gained importance recently thanks to increasing levels of integration and also the desire for move ability. Moreover, the progress in battery technology is slower as compared to the ever-increasing power demand thanks to advances in electronic circuits; the battery technology is unable to produce an answer to the facility drawback, therefore, Associate in Nursing correct estimation of “average power dissipation” is needed to estimate battery life; additionally, the right estimate of “peak power dissipation” is needed to review circuit dependability. The 3 major sources of power dissipation in Very-large-scale integration (VLSI) circuits are: (i) switching part of power, that is increasing thanks to increase in on-chip clock rates (ii) part of power thanks to direct-path short-circuit current in circuits, that depends upon the increase and fall times of signals and (iii) part of power thanks to discharge current that is increasing at Associate in Nursing threats rate thanks to skinny gate compound and tiny pure mathematics effects like tunneling and drain iatrogenic barrier lowering that square measure dominating thanks to device scaling.

Revised Manuscript Received on September 15, 2019
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The short-circuit dissipation of complementary metal compound semiconductor (CMOS) electrical converter with and while not load (for equal \( t_r \) and \( t_f \) times of input and output signals) is just a fraction (< 20%) of the full dissipation. Various combinational logic units are adder, multiplier, divider, barrel shifter and arithmetic logic unit (ALU) circuits. The selection of a particular data-path depends upon the state-of-the-art in digital design. The most important and widely accepted metrics for measuring the quality of data-path designs are propagation delay, area and power [7], [8]. Furthermore, the progress in battery technology is slower as compared to the ever-increasing power requirement due to advances in electronic circuits; the battery technology is unable to provide a solution to the power problem, therefore, an accurate estimation of “average power dissipation” is required to estimate battery life; also, the correct estimate of “peak power dissipation” is required to study circuit reliability [9]. The three noteworthy wellsprings of intensity dissemination in VLSI circuits are (i) switching component of power, which is increasing due to increase in on-chip clock rates (ii) major of intensity because of direct-way impede in circuits, that depends upon the \( t_r \) and \( t_f \) of signals and (iii) fundamental of power due to leakage current which is increasing at an alarming rate due to thin gate oxide and small geometry effects like tunneling and drain induced barrier lowering which are dominating due to device scaling [10]. The short-circuit dissipation of complementary metal oxide semiconductor (CMOS) inverter with and without load (for equal \( t_r \) and \( t_f \) of input and output signals) is only a fraction (< 20%) of the total dissipation.

### III. DESIGN METHODOLOGIES

#### 3.1 4:1 Multiplexer

*Figure 1: 4:1 MUX circuit diagram*

It is observed from the Figure 1, CMOS 4:1 MUX circuit diagram, four inputs like \( A, B, C \) & \( D \) and input control signal are \( S_0 \) & \( S_1 \) getting single output.

*Table 1 4:1 multiplexer truth table*

<table>
<thead>
<tr>
<th>( S_0 )</th>
<th>( S_1 )</th>
<th>( Q_n )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>A</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>B</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>C</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>D</td>
</tr>
</tbody>
</table>

*Figure 2: 4:1 MUX Logic diagram*

In material science, a device (or MUX) could similarly be a gadget that picks one in every one of the couple of straightforward or propelled data banner and advances the picked commitment to one line. A device of 4 wellsprings of data has two data control signals, that unit of estimation used to pick that information line to send to the yield. Multiplexers square in a general sense used to extend total the proportion of data which can be sent over the framework among an unmistakable proportion of it moderate and learning measure. A device is what's more called accomplice information selector. Multiplexers will even be adjusted execute man of science components of different variables.
It is seen from the Figure 3, Ordinary Balance FET 26T 4:1 Multiplexer, A multiplexer of four information sources has two data control signals, which are utilized to pick which information line to send to the yield.

Table 2 4:1 Multiplexer Truth Table

<table>
<thead>
<tr>
<th>$S_0$</th>
<th>$S_1$</th>
<th>$\overline{S}_0$</th>
<th>$\overline{S}_1$</th>
<th>$Q_n$</th>
<th>$\overline{Q}_n$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>A</td>
<td>$\bar{A}$</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>B</td>
<td>$\bar{B}$</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>C</td>
<td>$\bar{C}$</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>D</td>
<td>$\bar{D}$</td>
</tr>
</tbody>
</table>

$Q_n = S_0\bar{S}_1A + S_0\bar{S}_1B + S_0\bar{S}_1C + S_0\bar{S}_1D$

$Q_n = (S_0 + S_1 + A)(S_0 + S_1 + B)(S_0 + S_1 + C)(S_0 + S_1 + C)$

Figure 4: Proposed of Fin FET 24T 4:1 Multiplexer.

It is seen from the Figure 4, Ordinary Blade FET 24T 4:1 Multiplexer, A multiplexer of 4 inputs (A, B, C and D) has 2 select lines ($S_0, S_1$), which are used to pick which data line to send to the yield. We reduced two transistors by using Karnaugh map.

3.2 Power Dissemination

Low power circuit vogue has show up as a general subject within the gift business, within the past, serious problems among professionals and planners for composing formed circuits were on area, speed, and cost, whereas no mandatory spatial relation was paid to regulate spread.

$P_{Static} = I_{Static} \cdot V_{dd}$  \hspace{1cm} [4]

$P_{Dynamic} = \alpha \cdot c_L \cdot V_{dd} \cdot f$  \hspace{1cm} [5]

$P_{Shortcircuit} = I_{SC} \cdot V$  \hspace{1cm} [6]

$P_{Leakage} = V_{dd} \cdot (I_s + I_g + I_d)$  \hspace{1cm} [7]

$P_{Total} = P_{Dynamic} + P_{Leakage}$  \hspace{1cm} [8]

$P_{Total} = (\alpha \cdot c_L \cdot V_{dd} \cdot f) + V_{dd} \cdot (I_s + I_g + I_d)$  \hspace{1cm} [9]
IV. SIMULATION RESULTS

It is determined from the Figure five. The phvt and nhvt transistors schematic chart comprise of Fin Pitch ar 48nm, Load capacitance is 10fF, at provide voltage from 1Volts. Customary of Fin FET 26T 4:1 multiplexer schematic chart was completed utilizing Cadence 18nm innovation.

<table>
<thead>
<tr>
<th>Specification</th>
<th>nhvt</th>
<th>phvt</th>
</tr>
</thead>
<tbody>
<tr>
<td>Library name</td>
<td>gpdk (ff)</td>
<td>gpdk (ff)</td>
</tr>
<tr>
<td>Fin pitch</td>
<td>48nm</td>
<td>48nm</td>
</tr>
<tr>
<td>Drawn Gate Length</td>
<td>18</td>
<td>18</td>
</tr>
<tr>
<td>Number of Fins per Finger</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Number of Finger</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Multiplier</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Load Capacitance</td>
<td>10 fF</td>
<td></td>
</tr>
</tbody>
</table>

It is seen from the Figure 7, We have decreased two transistor by utilizing Karnaugh map. The phvt and nhvt transistors schematic chart comprise of Fin Pitch ar 48nm, Load capacitance is 10fF, at provide voltage from 1Volts. Proposed of Fin FET 24T 4:1 multiplexer schematic outline was completed utilizing Cadence 18nm innovation.

Figure 5: Fin FET 26T 4:1 multiplexer Schematic

Figure 6: Conventional of Fin FET 26T 4:1 Multiplexer Output Waveform at 20MHz.

As appeared in figure 6 Conventional of Fin FET 26T 4:1 multiplexer reproduction consequence of yield waveform at 1Volts at the recurrence 20MHz in 18nm innovation.

Figure 7: Proposed 24T 4:1 Multiplexer schematic

Figure 8: Proposed 24T Multiplexer output waveform in 18nm Technology at frequency 20MHz.

As appeared in figure eight projected of Fin FET 24T 4:1 Multiplexer reproduction consequence of yield waveform at 1Volts at the recurrence 20MHz in 18nm innovation. We have diminished two transistor by utilizing Karnaugh map.
Table 4: Simulation Results for Fin FET 4:1 Multiplexer with 1 V supply in 18nm Technology

<table>
<thead>
<tr>
<th>Design</th>
<th>Dynamic power (µW)</th>
<th>Leakage power (nW)</th>
<th>Static power (µW)</th>
<th>Delay(µs)</th>
<th>Area(µm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fin FET</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Conventional 4:1 MUX [1]</td>
<td>6.797</td>
<td>20.07</td>
<td>56.66</td>
<td>1017</td>
<td>52.92</td>
</tr>
<tr>
<td>Fin FET</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

It is determined from the Table four, projected Fin FET 4:1 Multiplexer. We have diminished two transistor by utilizing Karnaugh map then Dynamic Power Reduced 47.77%, Leakage Power Reduced 29.09%, Static Power Reduced 14.61%, Delay decreased 94.13% and Area Reduced 40.74% utilizing Cadence 18nm Technology.

Figure 9: Comparison of conventional and proposed 4:1 Multiplexer in 18nm Technology.

It is determined from the Figure nine, projected Fin FET 4:1 Multiplexer. We have diminished two transistor by utilizing Karnaugh map then Dynamic Power Reduced 47.77%, Leakage Power Reduced 29.09%, Static Power Reduced 14.61%, Delay decreased 94.13% and Area Reduced 40.74% utilizing Cadence 18nm Technology.

V. CONCLUSION

In this paper, a Fin FET 4:1 Multiplexer utilizing 24 transistors has been proposed. The proposed Fin FET 24T 4:1 Multiplexer is built utilizing in Cadence 18 nm innovation. The proposed outcomes are contrasted and the prior genuine structure. We have decreased two transistors by utilizing Morgan’s laws contrasted and the prior real structure. Regular of Fin FET 4:1 Multiplexer utilizing 24 transistors as far as power, deferral and territory. It is played out the Dynamic power is diminished by 47.77%, Leakage Power is diminished 29.09% and Static Power is diminished by 14.61%. It is likewise understood that the deferral is diminished by 94.13% and territory is diminished by 40.74% for 24 transistors Fin FET 4:1 Multiplexer in Cadence 18nm Technology.

REFERENCES

9. NVIDIA Pascal micro architecture and Infinite Compute for Infinite Opportunities.