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An Analogy of VSC with MMC Topology for HVDC application

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***Abstract*—This paper deals with the detailed description and understanding of the effect of an HVDC system when VSC and MMC are used. It describes the working principle of each type and its comparison when applied to a HVDC system. Steady state and transient analysis has been done and its results have been discussed in detail.. It also gives an idea of the harmonic changes done by FFT analysis. The simulation has been carried out using PSCAD/EMTDC software. The results are given accordingly.**

***Index Terms*— VSC-HVDC, MMC, multilevel inverter, FFT analysis.**

I. INTRODUCTION

The classical HVDC system employs converters with thyristors and depends on the ac voltage provided by the ac network for satisfactory operation. In line commutated converters (LCC), thyristors can be turned on and off only with the help of commutating voltage [1]. The main disadvantage with LCC-HVDC system is commutation failure, which can be overcome in a HVDC system that uses voltage source converters (VSC).

The Voltage Source Converters (VSC) based systems uses IGBTs, where the switch can be turned on as well as turned off by an external voltage pulse [2]-[3]. A diode connected in antiparallel with the IGBT enables the switch to conduct current in both directions. The greater flexibility of VSC-HVDC finds applications in supply to remote locations and supply to passive networks. It is ideally suited for connection of renewable sources to the grid. It provides variable frequency operation and bidirectional flow of active and reactive power [4]. Advancements in VSC HVDC have led to parallel developments in FACTS devices.

One of the thrust areas in VSC HVDC is that of converter topology, which has been an area of active research since the early days of VSC-HVDC [5]. From the details of VSC, it can be observed that there is a need for going into modular multilevel converters [6].

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Few drawbacks of VSC is that it has more losses and an uneven distribution of losses in both the outer and inner devices. It uses diodes which transfers some amount of voltage, hence reduces the stress on other electrical devices.

The cascaded topology is best suited for high power applications because of its modular structure which enables high voltage operation. The MMC is composed of single-phase two-level voltage source converter (2L-VSC) legs, which are also known as half-bridges [6]. MMC is a type of cascaded topology which will overcome the defects in the VSC system [7]. Research is perpetuating in MMC field, to increase the voltage level and to minimize the harmonics. The control strategy is very complex, hence time-consuming and tedious [8]-[11]. The present work deals with comparison of steady state and transient state analysis of VSC and MMC-HVDC system. Modeling and simulation of both the systems are done in PSCAD environment.

II. BASIC PRINCIPLE OF VSC MULTILEVEL CONVERTER

A VSC-HVDC system consists of two converter station built with multi-level-converter topologies. The two level VSC converter topology has an IGBT switch, anti-parallel diode. The anti-parallel diode is required for the four quadrant operation of the converter. The dc bus capacitor stores energy so that the power flow can be controlled and offers filters the dc harmonic [2].

The control strategy adopted in a VSC-HVDC system is SPWM (sinusoidal pulse width modulation). Independent control of reactive and active power is achieved through SPWM. The power is controlled by changing the phase angle between the sending end and the reactive power is controlled by varying the modulation index. The modes of controls used in the system are as follows:

- Control of AC voltage at the sending end which is achieved by the exciter of 75 MVA synchronous generator.
- Power flow is obtained by controlling the phase angle of the ac side voltage of the sending end converter.
- The dc voltage is controlled by adjusting the phase angle of the ac side voltage of the receiving end converter.
- Reactive power that is generated by the sending end converter is made low by adjusting the magnitude of the voltage on the ac side of the sending end converter.

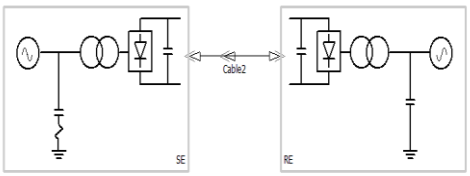

Fig 1: VSC-HVDC system

III BASIC PRINCIPLE OF MODULAR MULTILEVEL CONVERTER (MMC)

The MMC sub-module consists of two IGBT switches (half-bridge) and four IGBT switches (full bridge). The sub-module produces a voltage level, hence it is easier to increase the number of levels by adding extra modules to the circuit and taking care of the controls [7]. MMC is modular in structure and the structure is as shown in Fig 1.

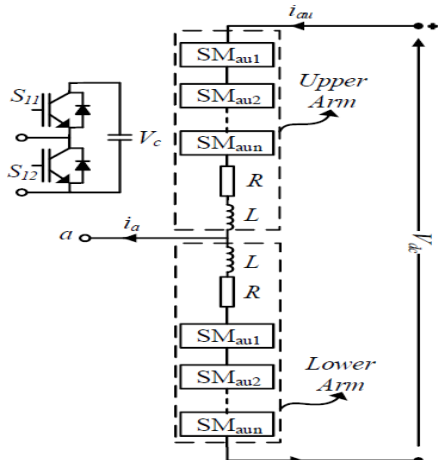

Fig 2: MMC Topology

- Each phase of MMC has two arms i.e.; upper arm and lower arm, which are connected in series across the dc link
- Each arm has 'N' half bridge sub modules connected in series and an arm inductor (L)
- The modeled resistors 'R' are resistive losses in the converter
- The ac terminal is located at the midpoint junction between the two arms
- The purpose of arm inductors is to limit fault currents and parasitic currents. The value of the inductance is very small

From the sub module (SM) diagram as shown in Fig 1, it can be seen that each SM is a simple chopper like cell composed of 2 IGBT switches (S_{11} and S_{12}), 2 anti-parallel diodes and a capacitor C. Figure 2 shows the operation of a sub module. Depending upon the switching action, the output of SM is either V_C or 0 as shown in Table 1.

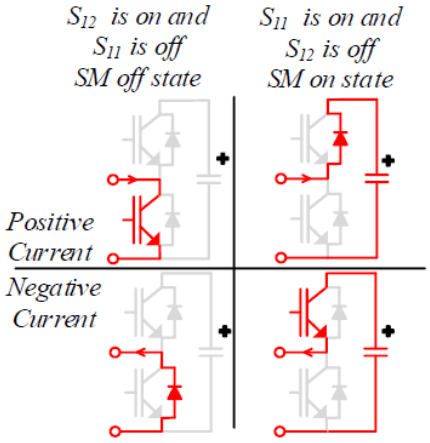

Fig 3: State of SM and current path

TABLE 1:SUB MODULE VOLTAGE AND CURRENT STATE

S_{11}	S_{12}	V_0	Capacitor voltage	
			I>0	I<0
1	0	V_C	Increases	Decreases
0	1	0	No change	No change

The modulation strategy used is carrier phase shift, it requires (n-1) carrier signals of the same amplitude and frequency, phase shifted by 360/ (n-1) degrees from one another to generate an n-level inverter output phase voltage. The main advantages of MMC when compared with other converter are as follows:

- Flexibility for scaling to different power and voltage levels
- Lower Harmonic Distortion, thus decreasing the filter size and cost
- Higher Efficiency
- High redundancy due to modular structure (A faulty module can be either by-passed or replaced without much of an effort)
- High switching frequency of the converter through low switching frequency of the modules
- Limitation of AC side current in case of a dc-link short-circuit due to arm inductor
- Low voltage rating of the semi-conductor device, limited by the sub-module capacitor voltage (Vdc/N)

The VSC (2-level) and MMC topology converters will be applied to a HVDC system in the following section.

IV APPLICATION OF VSC TO A HVDC SYSTEM

The VSC-HVDC transmission system is a two terminal monopolar system designed for ±33kV, 48MW transmission capacity and transmits power from sending end to receiving end through a cable. The distance between the sending end and receiving end is 100km. Since it is a monopolar system cable is used for transmission and ground is used to return current. It consists of two co-axial cables with resistivity of 100[ohm*m].

The topology implemented in this system is a two-level VSC (voltage source converter). The converter is typically controlled through sinusoidal PWM (SPWM) and the harmonics are directly associated with the switching frequency of each converter leg. The carrier frequency used is 33 kHz. Figure 2 and 3 shows the two-level topology used in the VSC system at both the rectifier and inverter end.

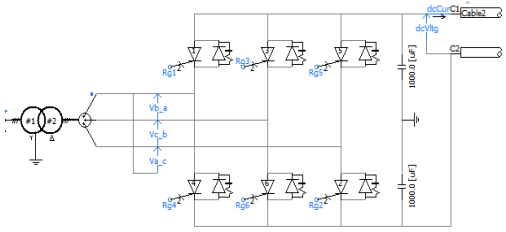

Fig 4: VSC 2-level -HVDC system, rectifier end

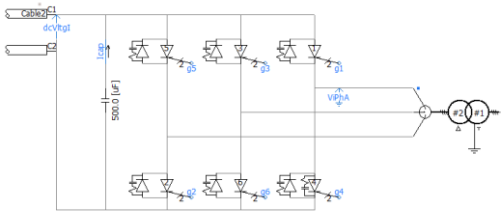

Fig 5: VSC 2-level -HVDC system, inverter end

V APPLICATION OF MMC TO A HVDC SYSTEM

The PSCAD model of MMC (2-level) in HVDC system is as shown in Fig 4 and Fig 5. The capacitor voltage indicates the energy stored in the upper and lower arms. Here, PI controller is used to determine additional dc component. The integral part eliminates static errors in the average energy level. The modulation strategy used is the carrier phase shift PWM. The controller provides a unique reference signal for each sub-module, without considering the state of other sub modules in the arm or leg. The ratings of the system is 1MVA rated power with input voltage (L-L) of 500kV and rated current of 2kA. The fundamental frequency is 60Hz and the carrier frequency is 1650Hz. The sub-module capacitance used is 600uF, arm inductance value is 0.0036H and sub-module resistance is 5kΩ. These ratings are used to understand the working of the test system and it can be upgraded to higher voltages. Figure 4 shows the rectifier side model and consists of dc link capacitors of 100uF value, which is used to provide dc supply to the inverter side. Figure 5 shows the inverter side HVDC system with dc link capacitors of 100uF value. The same control strategy issued and the same carrier based phase shift PWM method is employed here. The arm inductors are used to limit the fault current. It does not use filters on either side.

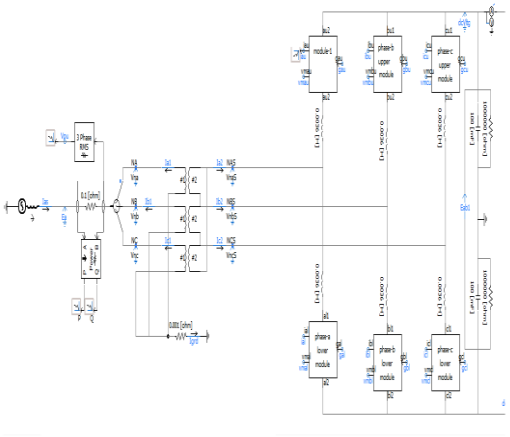

Fig 6: MMC 2-level -HVDC system, rectifier side

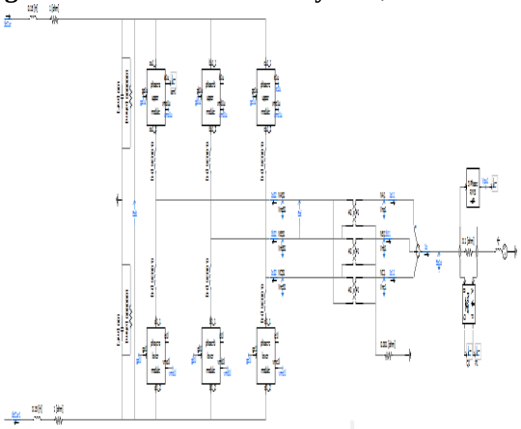

Fig 7: MMC 2-level - HVDC system, inverter side

VI RESULTS AND DISCUSSION

A. STEADY STATE OPERATION OF VSC-HVDC SYSTEM

The complete VSC-HVDC system is modeled using PSCAD/EMTDC environment. The voltages and current waveforms at the rectifier and inverter terminals, the dc voltage and currents have been observed as shown in Fig 8-12 and Fig 18-22 respectively . Generator operates as a voltage source at its terminals for the period 0 to 1 second during the start-up. After 1.0 second, the generator operates as a synchronous machine with its terminal voltage determined by its exciter. PWM with carrier frequency up to 33 times fundamental has been used; its value has to be dividable by three and an odd number. Total power of 48.42 MW is received at the inverter station

B. STEADY STATE ANALYSIS OF MMC-HVDC SYSTEM

The complete MMC-HVDC system is modeled using PSCAD/EMTDC environment. The ac bus voltage is as shown in Fig 13. It shows that the output voltage (L-G) is 408kV (i.e., 500kV/√3=288.68kV, 288.68*√2 = 408kV). The rectifier side ac bus current and its FFT analysis is as shown in Fig 14 and Fig 15. It shows the value of the bus current to be 0.2kA.

The FFT analysis shows the fundamental rms voltage to 0.144kA, the 3kA. 3rd harmonic is 0.00015kA. Figure 25 shows the inverter side bus voltage. It shows that the bus voltage (L-G) is 408kV.

The fundamental rms voltage is 288.6kV, 3rd harmonic is 0.0031kV. The inverter side bus current and its FFT analysis is as shown in Fig 23 and Fig 24. The inverter bus current is 0.2kA. The fundamental component is 0.131kA, 3rd harmonic is 0.0010kA. The dc line voltage and current are shown in Fig 16 and Fig 17. It shows that the voltage is settled at a voltage of 33kV and the current has settled to a constant value at 1.75kA. The sooner the dc value settles, the better is the system performance. The inverter side line voltage is as shown in Fig 25. The phase voltage has two levels i.e; +22kV and -22kV. The line voltage has three voltage levels i.e.; 44kV, 0kV, -44kV. When an arm inductor is introduced in the HVDC system, it smoothens the waveform and it gives additional protection to the system.

C. TRANSIENT STATE ANALYSIS OF VSC BASED HVDC SYSTEM

In order to study the unbalanced condition in VSC-HVDC system, a single line to ground fault is created at the inverter AC bus at t = 4.3 sec with fault duration of 0.05 sec. The system is simulated for a duration of 8 sec. Further it was observed that during 1 phase fault at the receiving end AC bus the voltage dropped to zero and there was a overshoot in the current waveform as shown in Fig 28 and Fig 29 respectively. For cable transmission the DC line to ground fault is not possible. The fault currents are too high in case of VSC-HVDC overhead transmission. The rectifier ac bus current rises to 6.51.kA and attains steady state in 0.373s thereby increasing by 30%, but the inverter ac bus current shoots up to a peak value of 7kA and settles down in 0.12s The current rises to a certain limit and attains steady state. The dc bus voltage and dc bus current under 1 phase fault are as shown in Fig 28 and Fig 29. The dc bus voltage reaches a peak value of 58kV and reaches steady state in 0.23s. The dc current shoots up to a value 2.4kA and reaches steady value in 0.25s.Similarly, Fig 31 and 32 shows the results with 3 phase fault.

D. TRANSIENT STATE ANALYSIS OF MMC BASED HVDC SYSTEM

Transient analysis is mainly done to determine the over current and overvoltage values, so as to determine the ratings of protection devices. When a fault is introduced into the system, there is a rise in current for certain duration of time and then it settles back to its steady state value. For an MMC-HVDC system 1 phase fault at inverter bus side for duration of 0.05s is introduced. Initially the fault introduced is a 1 phase fault, where only fault in phase C is enabled. The fault is initiated at 4.3 sec for a duration of 0.05s. Figure 35 shows the inverter bus currents under 1 phase fault condition. There is very little difference in the rectifier ac bus current, it rises to 0.25kA and attains steady state in 0.3s thereby increasing by 25%, but the inverter ac bus current shoots up to a peak value of 1kA and settles down in 0.3s, increasing by 75%. The current rises to a certain limit and attains steady state. The dc bus voltage and dc bus current under 1 phase fault are as shown in Fig 33 and Fig 34. The dc bus voltage reaches a peak value of 35.8kV and reaches steady state in 0.3s, increasing by 54%. The dc current shoots up to a value 2.24kA and reaches steady value in 0.4s. Similarly, Fig 36 and Fig 37 shows the results with 3 phase fault

VSC SYSTEM STEADY STATE RESULTS:

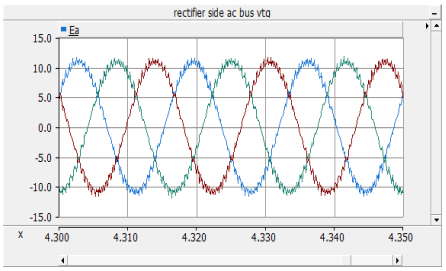

Fig. 8 Steady state rectifier voltage (VSC)

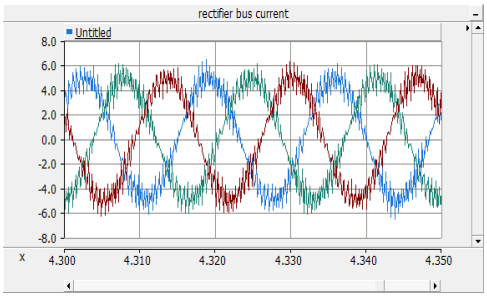

Fig. 9 Rectifier side ac current (VSC)

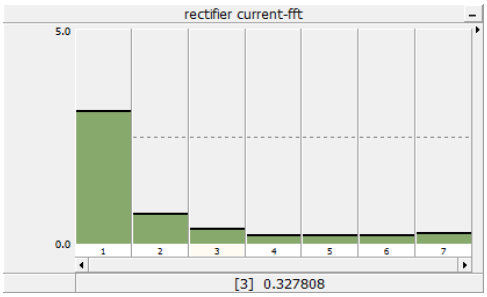

Fig 10: Rectifier side current FFT analysis(VSC)

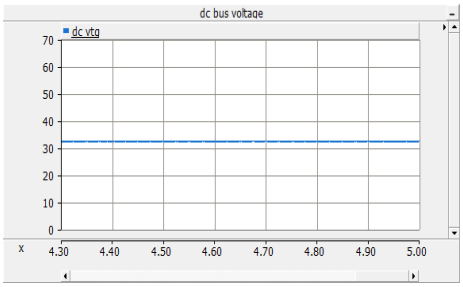

Fig. 11: Steady state DC Voltage (VSC)

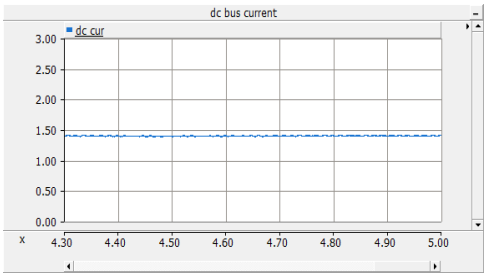

Fig 12: DC bus current (VSC)

MMC SYSTEM STEADY STATE RESULTS

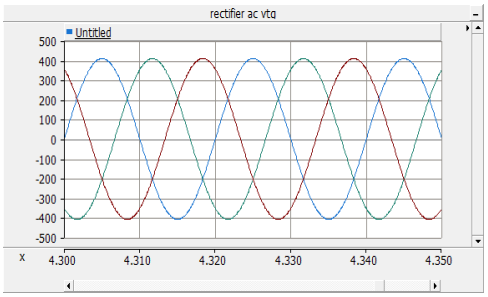

Fig 13: Steady state rectifier voltage (MMC)

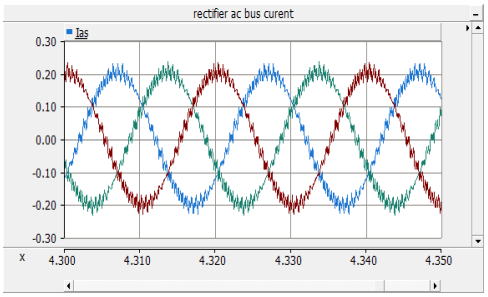

Fig 14: Rectifier side ac current (MMC)

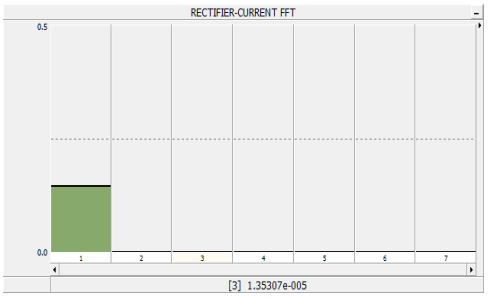

Fig 15: Rectifier side current FFT analysis (MMC)

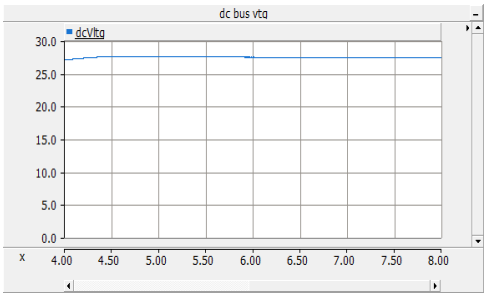

Fig 16: Steady state DC bus voltage (MMC)

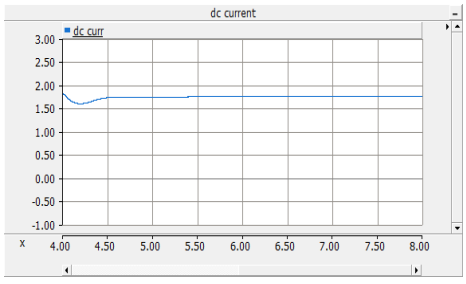

Fig 17: DC bus current (MMC)

VSC SYSTEM STEADY STATE RESULTS

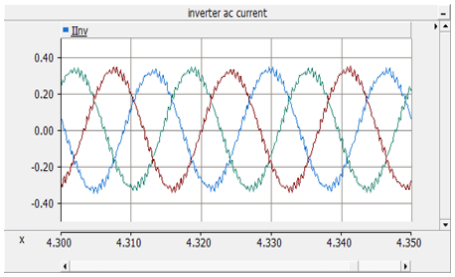

Fig.18: Inverter side current (VSC)

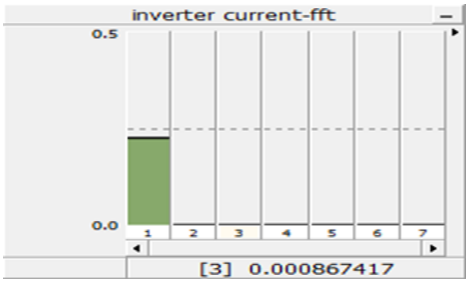

Fig. 19: Inverter side current FFT analysis (VSC)

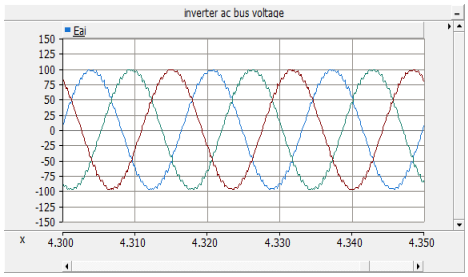

Fig 20: Inverter side voltage (VSC)

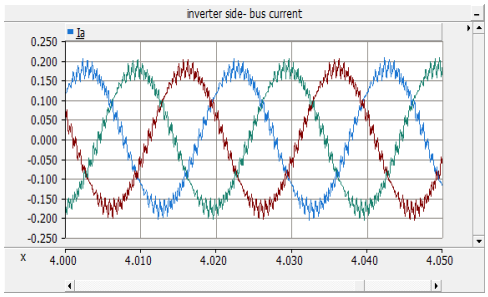

Fig 21: Inverter side current (VSC)

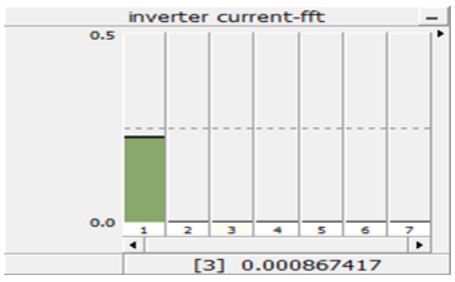

Fig. 22: Inverter side current FFT analysis (VSC)

MMC SYSTEM STEADY STATE RESULTS

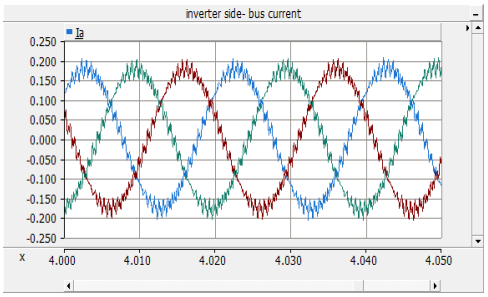

Fig 23: Inverter side current (MMC)

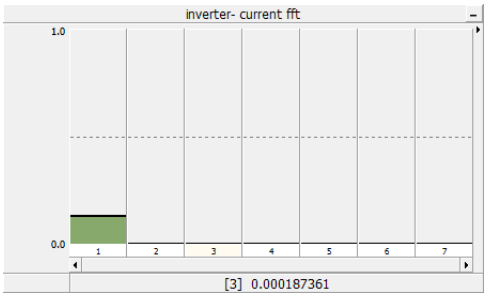

Fig 24: Inverter side current FFT analysis (MMC)

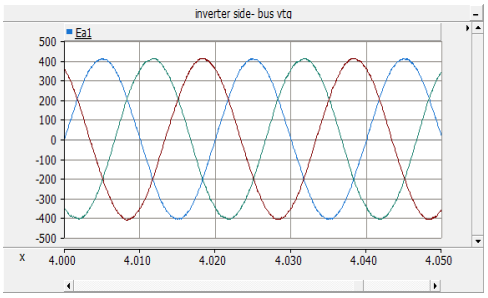

Fig 25: Inverter side voltage (MMC)

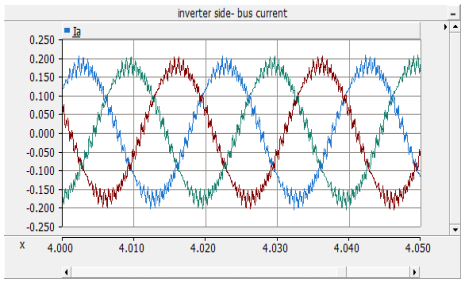

Fig 26: Inverter side current (MMC)

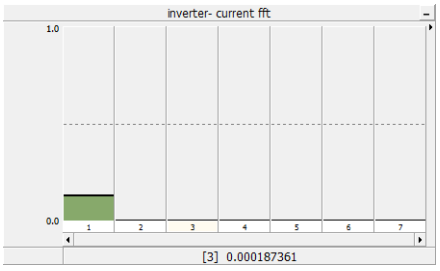

Fig 27: Inverter side current FFT analysis (MMC)

VSC SYSTEM TRANSIENT STATE RESULTS

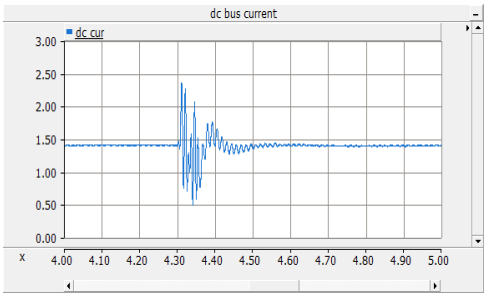

Fig 28: DC bus current for 1 phase fault (VSC)

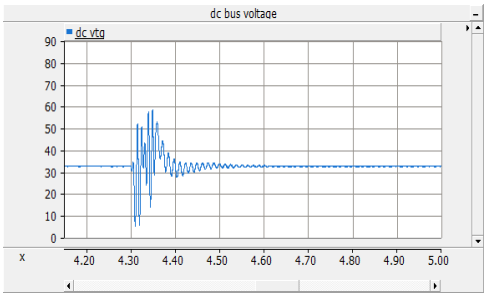

Fig 29: DC voltage for 1 phase fault (VSC)

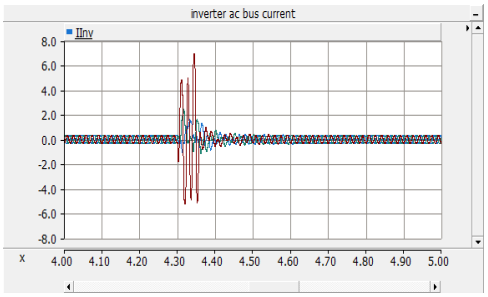

Fig 30: Inverter bus current for 1 phase fault (VSC)

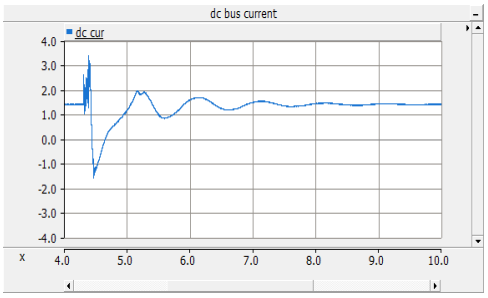

Fig 31: DC bus current for 3 phase fault (VSC)

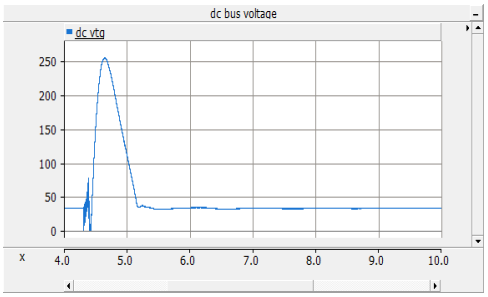

Fig 32: DC voltage for 3 phase fault (VSC)

MMC SYSTEM TRANSIENT STATE RESULTS

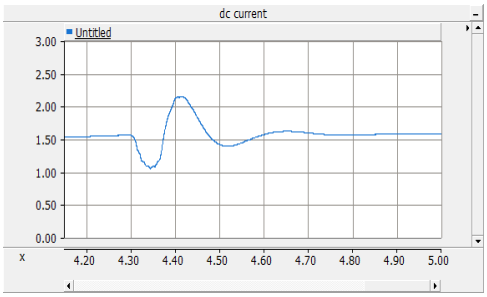

Fig 33: DC bus current for 1 phase fault (MMC)

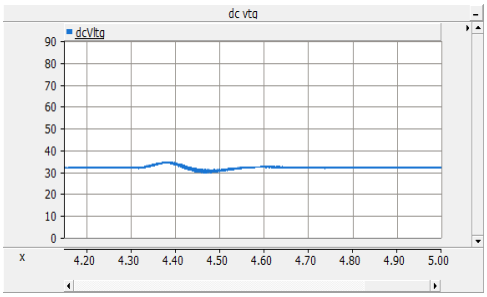

Fig 34: DC voltage for 1 phase fault (MMC)

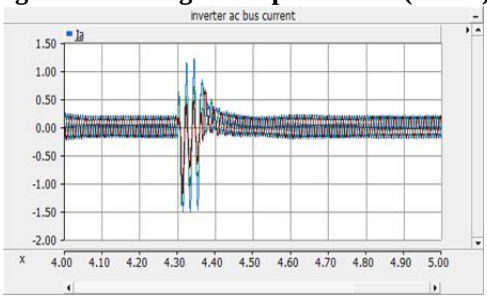

Fig 35: Inverter bus current for 1 phase fault (MMC)

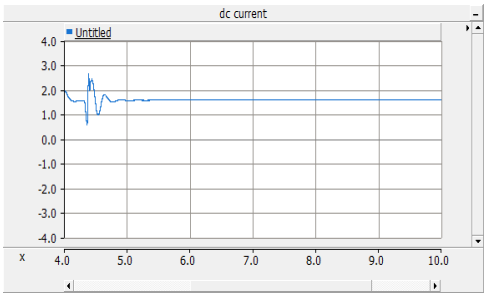

Fig 36: DC bus current for 3 phase fault (MMC)

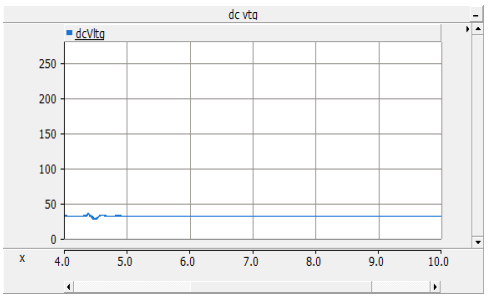

Fig 37: DC voltage for 3 phase fault (MMC)

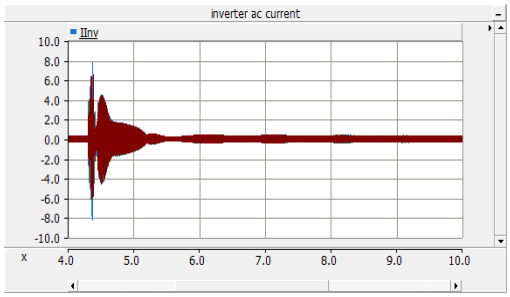

Fig 38: Inverter bus current for 3 phase fault (VSC)

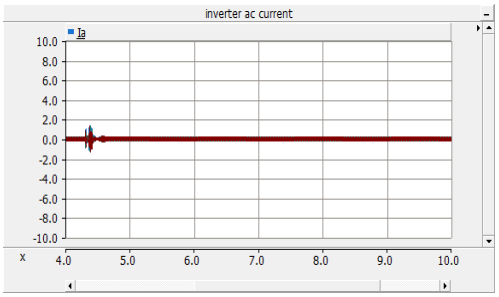

Fig 39: Inverter bus current for 3 phase fault (MMC)

VII. CONCLUSION

In this paper the VSC and MMC systems are understood in detail and the performance is analyzed. The steady state and transient state analysis were carried out on both VSC and MMC systems and the results were compared. Different parameters are observed and compared for the two systems.

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