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Simulation of Switched Capacitor Inverter Topology with Boost Facility

R. Saravanan, A. Hanumaiah, M. Venkatesan, K Balachander

Abstract: ***Simulation of switched capacitor inverter topology with boost facility is presented in this paper. The main merits of this inverter topology with boos facility are highly adaptable for Photo Voltaic (PV) applications. The inverter is capable of boosting up low voltage DC into high voltage DC and then invert it to the required voltage level with a single stage. The switched capacitor inverter has a special extended structure, which minimizes the number of components and devices when compared to the other inverter is switched by the means of level shifting carrier based Pulse Width Modulation (PWM) technique. Further, some of the switches in the topology operate in the low frequency and this resulted in a reduction in switching losses thereby increasing the efficiency. This maintains the capacitor voltages at a balanced level. The simulation results are verified through MATLAB/Simulink.***

Keywords**: *Switched capacitor inverter, boost facilities Level shift PWM, THD.***

I. INTRODUCTION

In recent years, multilevel inverter (MLIs) structure has grown to be an attractive area among researches and industrials, who work in the area of which includes renewable energy integration and high power converters etc. [1]. MLIs are capable of generating nearly sinusoidal waveforms, which can solve of power quality problem. Primarily, MLIs produces a high quality AC output from a different DC voltage sources. MLIs are classified into diode clamped, capacitor clamped and cascaded H-bridge. The drawbacks of diode clamped inverter topology are that it shares unequal voltage between series connected capacitors and also it requires more diodes to produce more number of voltage levels at the output. Some of the advanced diode clamped inverter topologies are presented in [2]-[7]. In those topologies diodes are replaced with active devices, but this result in increased conduction losses because of high total conduction voltage at zero vectors. A cascaded MLI has many H-bridges which are connected in series at the output side. Each H-bridge requires an independent input DC source. If the magnitude of DC sources of all the H-bridge is equal, then the configuration is called as symmetrical configuration, whereas if the magnitudes of DC sources are different then the configuration is called as asymmetrical configuration. Asymmetrical configuration can generate more number of levels at the load when compared to symmetrical configuration. But controlling the asymmetrical configuration is highly complicated when compared to symmetrical one. Furthermore, both configurations a number of DC source. To generate higher level, utilization of the device is also increased. Many researchers have been designed using single DC source instead of separate DC sources for solving many problems in this paper [8, 9]. In Photovoltaic (PV) applications, generally a DC-DC converter is used to obtain high voltage from a low DC voltage. This high DC voltage is again inverted into AC voltage through MLIs. Hence, it is necessary for two stages of conversion. Thus this two stage conversion increases the system complexity and reduces the efficiency of the system. This paper proposes a new extendable capacitor clamped MLI using switched capacitor topology. Further, the proposed inverter uses a level shifting carrier based PWM to trigger the devices of the inverter. The main advantage of the system is that, components utilization of the system has been reduced due to its combined structure.

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* Correspondence Author
R. Saravanan*, EEE, Associate Professor at Balaji Institute of Technology & Science, Laknepally, Warangal ,Telangana 506330.
A. Hunumaiah, EEE, Professor, Vignan's Lara Institute of Technology and Science, Guntur, India.Email: appikatlahanumaiah1965@gmail.com
M. Venkatesan, EEE, Associate Professor, Vignan's Lara Institute of Technology and Science, Guntur, India. Email: drmvenkatesan_vlits@vignan.ac.in
K. Balachander, EEE, Associate Professor, Karpagam Academy of Higher Education , Coibatore.

II. POWER CIRCUIT DIAGRAM

Figure 1 shows the circuit diagram of a proposed inverter. It comprises a conventional H- bridge inverter along with switched capacitor network.

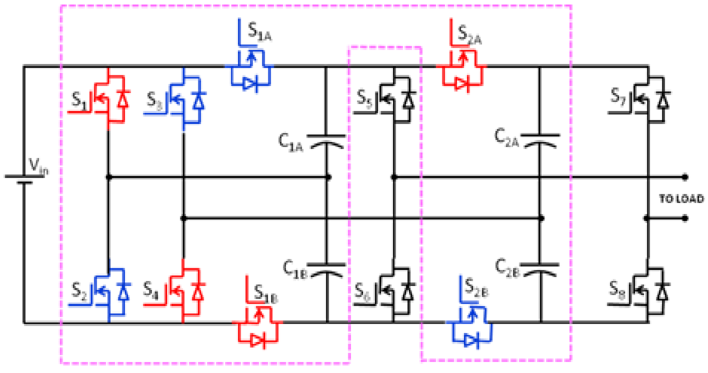

Fig.1 Power circuit diagram

The SCT has four capacitors and eight power devices. Switches S_1, S_4, S_{1B}, S_{2A} are named as S_P switches and S_2, S_3, S_{1A}, S_{2B} is named as S_N switches.

The circuit operates in two states such as state A and B. In state A, S_P switches are turned ON and in state B S_N switches are turned ON as shown in Figure 2(a) and 2(b) respectively.

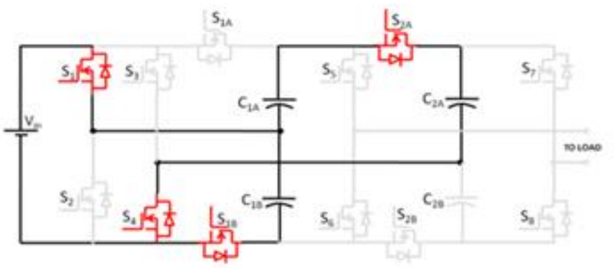

Figure 2(a)

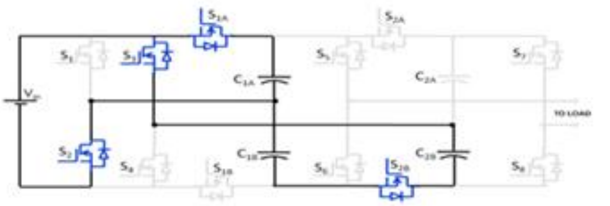

Figure 2(b)

A. Switching Pattern Generation

The inverter switching patten of the inverter is shown in Figure 3. In order to generate switching proper switching sequence, a sinusoidal reference signal is compared to the four high frequency carrier signals. In order improve the switching losses; four switches are made to operate the lower switching frequency. From table 1, it observed that, U_s & U_c represents a modulated signal and carrier signal respectively.

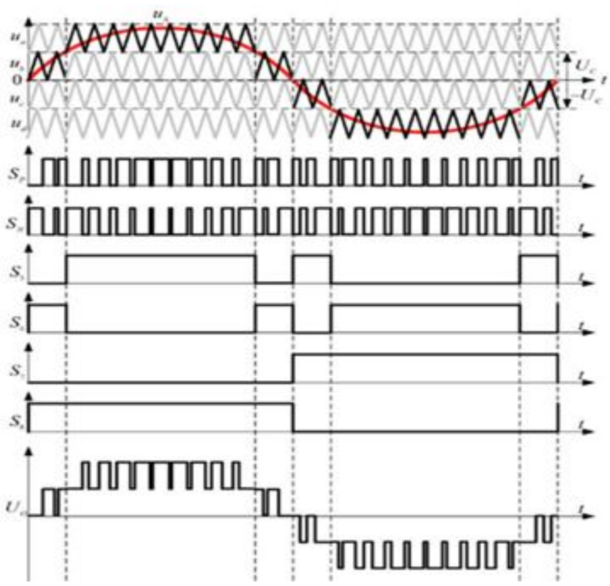

Table I Switching pattern

Condition for Modulation and Carrier Wave		S_P	S_N	S_5	S_6	S_7	S_8
$U_S >= U_C$	$U_S >= U_A$	1	0	1	0	0	1
	$U_S < U_A$	0	1				
$0 <= U_S < U_C$	$U_S >= U_B$	1	0	0	1	0	1
	$U_S < U_B$	0	1				
$-U_C <= U_S < 0$	$U_S >= U_C$	1	0	1	0	1	0
	$U_S < U_C$	0	1				
$U_S < -U_C$	$U_S >= U_D$	1	0	0	1	1	0
	$U_S < U_D$	0	1				

III. SIMULATION RESULTS

The switched capacitor inverter topology with boost facility has been verified using MATLAB/Simulink and results of the inverter are discussed. The input voltage is applied to the inverter circuit is 100V and then it is enhanced into approximately 375V peak value as shown in Figure. 5. Switching sequence of the inverter (S_P & S_N) is given in Figure. 7. Similarly, Figure 8 shows the switching patterns of the switches S_5 and S_6. Finally the switching patterns of the switches S_7 and S_8 are given in Figure 9.

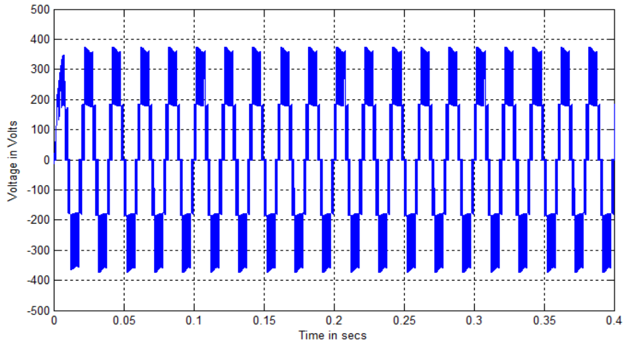

Figure 5 Load voltage waveform

The proposed inverter can be suitable for high voltage and high power applications as shown in Figure 6 as the current delivered to the load is nearly 30 A peak value.

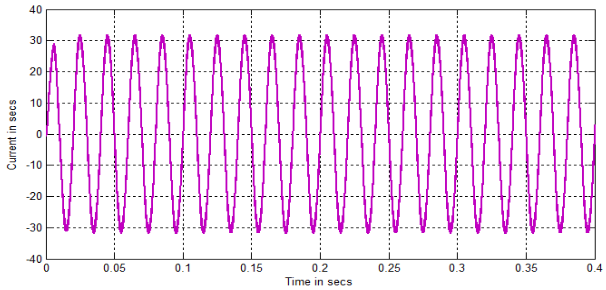

Figure 6 Load current waveform

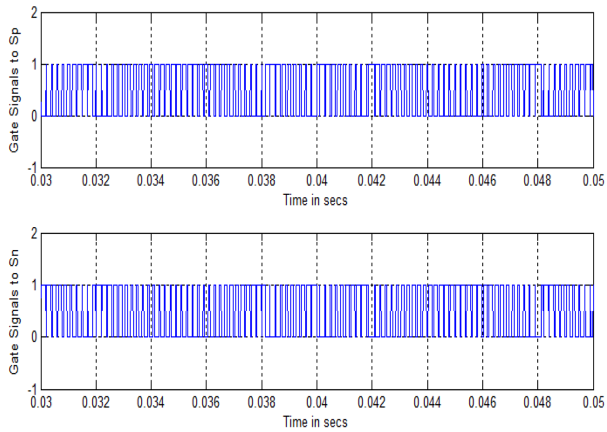

Figure 7 Switching pulses for S_P and S_N Switches

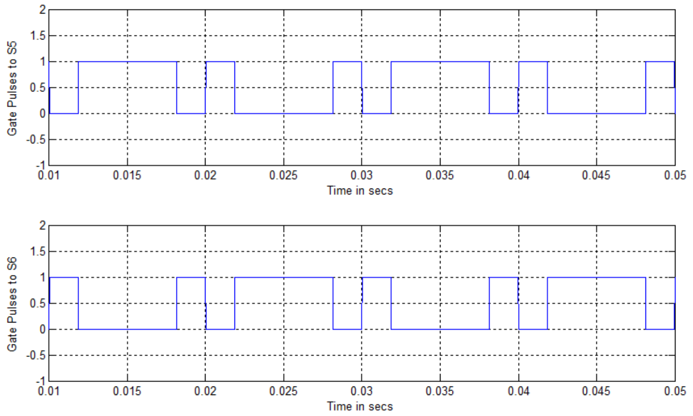

Figure 8 Switching pulses for S_5 and S_6 Switches

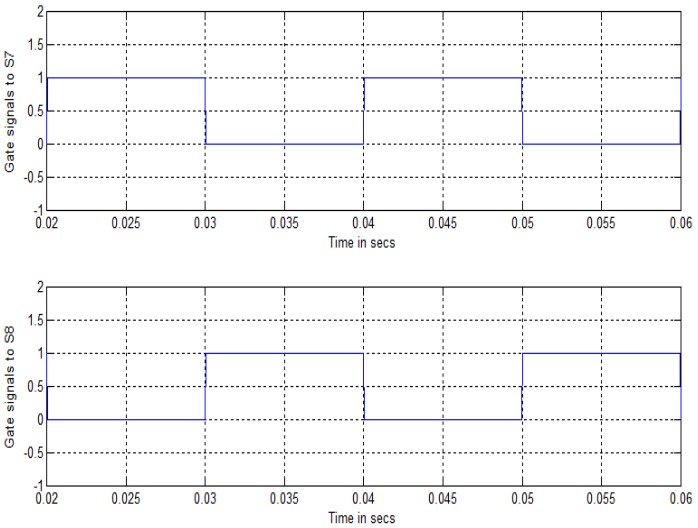

Figure 9 Switching pulses for S_7 and S_8 Switches.

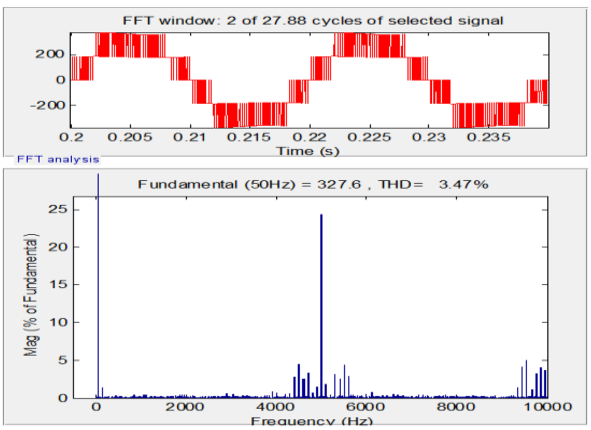

Figure 10 Output voltage THD

The THD performance of the inverter is 3.47% at full load operating condition and it is shown in Figure 10. The Modulation Index (MI) of the inverter is varied from 0 to 1 and the performance of the inverter has been analyzed through simulation. It is found that the number of levels reduces to three when the MI is reduced. The voltage waveform of the reduced MI is shown in Figure 11. Figure 12 shows the current waveform for MI of 0.5. It is found that the THD is less than 5%, which is the specified limit of IEEE standards.

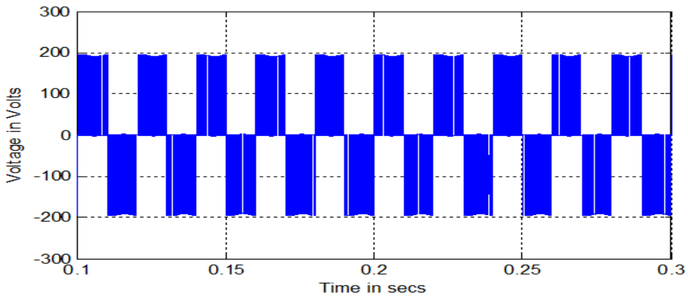

Figure 11 Load voltage with modulation index = 0.5

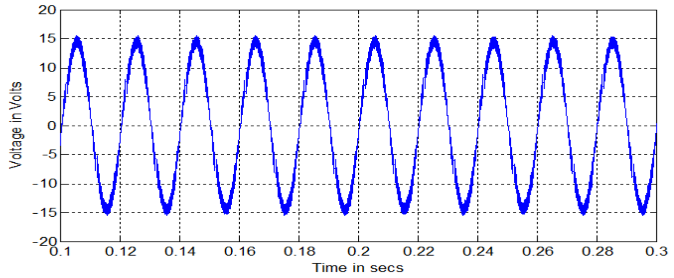

Figure 12 Load current with modulation index = 0.5

IV. CONCLUSION

Simulation of switched capacitor topology with boost capability has been simulated using MATLAB/Simulink. From this study it is observed that boost capability of inverter characteristics is highly suitable PV applications. Some of the switches of the proposed inverter operate in low frequency and it can reduce switching losses of the system is reduced significantly. This makes the inverter to operate at high efficiency. The proposed inverter uses a minimum number of switching devices when compared to the other inverters proposed in the literature. The system operates on acceptable THD values and also results are obtained for different modulation indexes.

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AUTHORS PROFILE

R. Saravanan, received his B.E., degree in Electrical and Electronics Engineering from Anna University, Chennai in 2007 and M.E., degree in Power Systems Engineering from Anna University, Chennai in 2009. He completed his Ph.D in Electrical Engineering from Anna University, Chennai, Tamil Nadu, India, in 2016. Currently, he has been an Associate Professor at Balaji Institute of Technology & Science, Laknepally, Warangal, Telangana 506330.

A Hanumaiah, Professor, Department of Electrical and Electronics Engineering, VLITS, Guntur, Andhra Pradesh. He completed his M.Tech, Acharya Nagarjuna University and PhD from Osmania University in 1996**.**

M Venkatesan received his B.E., in Electronics and Communication Engineering from Anna University, Chennai, Tamil Nadu, India, in 2008, and his M.E., in Power Electronics and Drives from Government College of Technology, Coimbatore, Tamil Nadu, India, in 2010. He completed his Ph.D in Power Electronics from Anna University, Chennai, Tamil Nadu, India, in 2017.

K. Balachander received the Diploma in Electrical and Electronics Engineering from PSG Polytechnic, Coimbatore in 1993 and Bachelor degree in Electrical and Electronics Engineering from Coimbatore Institute of Technology, Coimbatore in 2001. He acquired Master of Engineering in VLSI Design from Anna University Coimbatore in 2009 and doctorate in Electrical and Electronics Engineering from Karpagam Academy of Higher Education, Karpagam University, Coimbatore in 2017. He is working as an Associate Professor in Karpagam Academy of Higher Education, Karpagam University, India. He has totally around 14 years of teaching experience and 7 years of industry experience. He has published around 45 National and International Journal papers and 10 papers in Conference proceedings. He is a recognized reviewer in many reputed journals. He is also a member of ISTE, IE (I), IAENG, IRED, IACSIT. His areas of interests are Renewable Energy, Smartgrid, Distributed Generation and Power System Operation and Control.