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An Analytical Modeling for Dual Source Vertical Tunnel Field Effect Transistor

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Abstract*: *The given paper proposes the 2D analytical modeling of surface potential and electric field for a Dual Source Vertical Tunnel Field Effect Transistor (DSV-TFET). The 2-D Poisson equations are solved by parabolic approximation method, with the help of suitable boundary conditions and analytical expressions for surface potential and electric field distribution in DSV-TFET. The analytical results of proposed model are compared with simulation results drive using SILVACO TCAD tool, whereas in our proposed device DSV-TFET provides the high on current (ION=1.74×10^{-4} A/μm), low OFF current (IOFF= 6.92 ×10^{-13} A/μm), ION/IOFF current ratio in order of 10^{8} to 10^{9} with the minimum point of average subthreshold slope of 3.47 mV/decade which can be used for low power application.

Index Terms: Dual Source Vertical Tunnel FET (DSV-TFET), Subthreshold Slope (SS), Band-to-Band Tunneling (BTBT), Work Function (WF), Average Subthreshold Slope (AVSS), Low Power (LP).

I. INTRODUCTION

With the continuous scaling down of the conventional metal-oxide-semiconductor (MOS), its performance has also been degraded. Due to scaling degradation, MOS devices suffer from various short channel effects (SCEs) such as hot carrier effects, drain induce barrier lowering (DIBL) and very high OFF state current [1-3]. Also, subthreshold slope (SS) of MOSFET which cannot be suppressed below 60 mV/decade [4-5]. Owing to all these limitations, we are moving towards for an alternative device such of tunnel field effect transistors (TFET). Since TFET has a similar structure as that of MOSFET, it is a promising device to replace the MOSFET for low power application purpose. Devices such as TFET are being considered as a substitute in place of the conventional MOSFETs to overcome the limitations of short channel effects and improved input characteristics of the device like steeper sub-threshold slope (SS), low threshold voltage (VT) with high ION/IOFF current ratio [6]. The working principal of the TFET is based upon Band to band tunneling mechanism (BTBT) which responsible for the drain-source current which further controlled by the gate biasing voltage [7-8].

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In the BTBT mechanism, the electrons tunnel from valance band of source to the conduction band of drain and vice versa. Observing International Technology Roadmap for Semiconductors (ITRS) report in 2013 still there will be possibility to shrink the physical gate length of the transistor up to 4 nm till the year 2028 [9-10]. The revised report of the ITRS exhibited that the physical gate length will remain constant with 10nm after the year 2021.However, ITRS chair Paolo Gargini states that still some advance scaling may be possible if the transistors drive vertically. So, this paper includes the Vertical analysis of the U-shaped TFET device for low power (LP) applications. Also, the proposed U-shaped Vertical TFET overcome with the SCEs and found with steeper subthreshold slope with enhanced on current as per the results outcome. In comparison to the conventional TFET, the U-shaped Vertical TFET consist of U-shaped Vertical dual source with the effective thinner channel length up to 8 nm which meritoriously doubles the tunneling area and improves the drive current. It is also demonstrated and suggested that the drain doping concentration also improves the on current of the device. This device is made up of silicon material which can further scalable and simulated in accordance with the Moore's Law [11-12]. Additionally, there is narrow channel between drain and gate region, so the symmetric configuration can effectively avoid the short channel effects (SCEs). Therefore, in this paper 2-D Poisson equations are solved with the help of suitable boundary conditions and analytical expressions for surface potential and electric field distribution in DSV-TFET and are compared with simulation results using SILVACO TCAD tool.

In this paper, an analytical modeling of the DSV-TFET has been proposed with high ON state current which can be express by the band-to-band tunneling probability *T(E)* at source and channel junction as per the following equation 1 [13].

$$T(E)\ \alpha\ exp\left(-\frac{4\sqrt{2m^{*}}E_g^{3/2}}{3|e|\hbar\left(E_g+\Delta\Phi\right)}\sqrt{\frac{\varepsilon_S}{\varepsilon_{ox}}t_{ox}t_S}\right)\Delta\Phi \qquad (1)$$

Where E_g, t_{si}, ε_{ox}, ε_s, m^*, $\Delta\Phi$ and t_{ox} are energy band gap, silicon thickness, oxide dielectric constant, dielectric constant of material, effective carrier mass, energy range which provide tunneling and oxide thickness respectively. From equation 1 it is observed that the tunneling probability also depended on the energy bandgap of the material.

II. DEVICE STRUCTURE AND PROCESS PARAMETERS

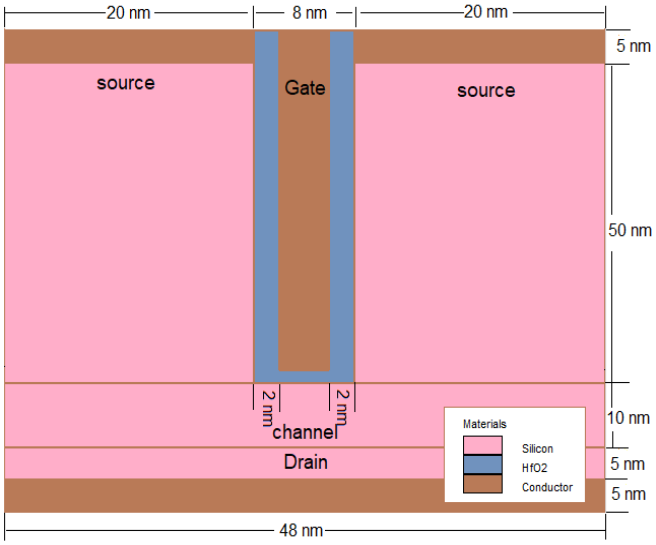

Fig. 1. Schematic structure of a DSV-TFET using SILVACO TCAD tool.

Figure 1 represent the schematic structure of proposed n-type DSV-TFET. In our proposed device, hafnium dioxide (HfO_2) is used as the gate oxide material which having a dielectric constant of (k= 22). The effective gate oxide thickness (t_{ox}) is 2 nm and the physical gate length (L_G) is 8 nm. The device consists of the symmetric dual source with effective length of 20 nm each side with the drain height and width of 5 nm and 50 nm respectively. The gate work function is set as 3.8 eV is optimized for the device. The doping concentration of channel (n+ type), highly doped source (p++ type) and drain (n++ type) is kept at 1×10^{18} cm^{-3}, 1×10^{20} cm^{-3} and 1×10^{19} cm^{-3} respectively.

Analytical modeling for the proposed device is done with the help of MATLAB tool whereas simulation results are obtained with the help of SILVACO tool by using 2-D Atlas device simulator with a non-local path band-to-band tunneling (BTBT) model, for determining the tunneling path. Lombardi's mobility model was activated for mobility effect and also enable the Band-gap narrowing model for high doping concentration in the drain and source regions and SRH (Shockley-Read-Hall) recombination model has been used.

TABLE I
LIST OF DEVICE PARAMETER USED FOR SIMULATION

PARAMETERS	SYMBOL	VALUES
Source Doping	N_A	1×10^{20} cm^{-3}
Drain Doping	N_D	1×10^{19} cm^{-3}
Channel Doping	N_i	1×10^{17} cm^{-3}
Gate Length	L_G	8 nm
Source Height	H_S	50 nm
Drain Height	H_D	5 nm
Channel Height or channel thickness	H_C	10 nm
Source Length 1	L_{S1}	20 nm
Source Length 2	L_{S2}	20 nm
Drain Length	L_D	48 nm
Gate Oxide thickness	t_{ox}	2 nm
Channel Length	L	48 nm
Gate work function	ϕ_{mg}	3.8 e V
Energy band gap of Si	E_g	1.12 eV
Dielectric constant gate oxide (HfO_2)	ε_{ox}	22 ε_O
Electron affinity	χ	4.05 eV

III. MODEL DERIVATION

The conduction phenomenon of V-TFET is completely different from the conventional MOSFET. The analysis of the DSV-TFET has been done by considering the source in two parts. The parameters of device are mentioned in table 1.

3.1. Surface Potential

The 2D Poisson's equation is used for the surface potential distribution in the gate oxide region as given below in equation (2) [14].

$$\frac{d}{dh}\left(\frac{d\Psi(h,l)}{dh}\right)+\frac{d}{dl}\left(\frac{d\Psi(h,l)}{dl}\right)=\frac{q\,N_{region}}{\varepsilon_{Si}} \quad (2)$$

where $\Psi(h,l)$ is surface potential as a function of device height (h) and lateral length (l), N_{region} is doping concentration of body or channel region, q is electronic charge and ε_{si} is dielectric constant of silicon. The profile of surface potential in the l direction is presumed to be a polynomial of second order [15] is shown in equation (3).

$$\Psi(h,l)=p(h)+q(h).l+r(h).l^2 \quad (3)$$

where p(h) is surface potential, r(h) and q(h) are arbitrary constants. p(h), r(h), q(h) are functions of h only.

3.1.1 Surface potential boundary condition

DSV-TFET has the surface potential at Si -HfO_2 interface (i.e. h=0) which is equal to the surface potential ($\Psi_s(h)$) shown by equation (4).

$$\Psi(h,0)=\Psi_s(h) \quad (4)$$

3.1.2 Electric field boundary condition

The electric field distribution at Si- HfO_2 interface is equal to zero, which is shown by equation (5).

$$\left.\frac{d\Psi(h,l)}{dl}\right|_{l=Tsi}=0 \quad (5)$$

The electric field displacement is continuous across the Si−HfO_2 interface, which given by equation (6).

$$\left.\frac{d\Psi(h,l)}{dl}\right|_{l=0}=\frac{-Cox\,(\Psi_G-\Psi_S(h))}{\varepsilon_{Si}} \quad (6)$$

$$\left.\frac{d\Psi(h,l)}{dl}\right|_{l=0}=\frac{\varepsilon_{ox}(\Psi_f(h)-V_{efb})}{\varepsilon_{Si}t_{ox}} \quad (7)$$

$$C_{ox}=\frac{\varepsilon_{ox}}{t_{ox}} \quad (8)$$

Where $\Psi_f(h)$ is gate surface potential, Cox is the gate oxide capacitance per unit area. V_{efb} , ε_{ox} , ε_{Si} and t_{ox} are effective gate flat band voltage, gate dielectric constant, silicon material dielectric constant and oxide thickness respectively. The effective gate flat band voltage is calculated using equation (9).

$$V_{efb} = V_g - V_{fb} \tag{9}$$

Where V_g and V_{fb} are gate voltage, flat band voltage at the gate respectively. V_{fb} is dependent on the work function of the gate. V_{fb} is calculated by given equation (10).

$$V_{fb} = \Phi_m - \left(\chi + \frac{E_g}{2q} + V_{th} * ln \left(\frac{N_i * exp\left(\frac{\Phi_{mg} - \Phi_m}{V_{th}}\right)}{N_i} \right) \right) \tag{10}$$

Where Φ_{mg}, Φ_m , V_{th} , , q, E_g, T, k, χ and N_i are work function of gate metal electrode, work function of metal, threshold voltage, electronic charge, energy band gap of silicon, room temperature, Boltzmann constant, electron affinity and doping concentration of intrinsic Silicon semiconductor respectively.

p(h), q(h) and r(h) are calculated by using the boundary conditions given in equation (4), equation (5) and equation (6) respectively.

$$p(h) = \Psi_f(h) \tag{11}$$

$$q(h) = \frac{C_{ox}\left(\Psi_f(h) - V_{efb}\right)}{\varepsilon_{Si}} \tag{12}$$

$$r(h) = \frac{1}{t_{si}}\left(- \frac{C_{ox}(\Psi_f(h) - V_{efb})}{\varepsilon_{Si}} \right) \tag{13}$$

Where, C_{ox} , and $\Psi_f(h)$ is gate oxide capacitance per unit area and surface potential at gate respectively. We are applying equation (11) and equation (12) in equation (13), arbitrary parameter r(h) is shown in the equation (14).

$$r(h) = \frac{\left(- \frac{C_{ox}(\Psi_f(h) - V_{efb})(1+\eta)}{\varepsilon_{Si}} \right)}{(2+\eta)t_{si}} \tag{14}$$

Where, $C_{si} = (\varepsilon_{si})/ t_{si}$, $\eta = C_{ox} / C_{si}$ and $C_{ox} = (\varepsilon_{ox})/ t_{ox}$.

After applying the value of *p(h)*, *q(h)* and *r(h)* in equation (3).

$$\Psi(h, l) = \Psi_f(h)(1 + Al + Bl^2) - Cl + Dl^2 \tag{15}$$

Where *A*, *B*, *C* and *D* is constant which are calculated by using the equation (16), (17), (18) and (19) respectively. A, B, C, D is depending on the V_g and device parameters.

$$A = \frac{C_{ox}}{\varepsilon_{Si}} \tag{16}$$

$$B = \frac{\left(\frac{C_{ox}}{\varepsilon_{Si}}(1+\eta) \right)}{(2+\eta)t_{Si}} \tag{17}$$

$$C = \frac{C_{ox} V_{efb}}{\varepsilon_{Si}} \tag{18}$$

$$D = \frac{\left(\frac{C_{ox} V_{efb}}{\varepsilon_{Si}}(1+\eta) \right)}{(2+\eta)t_{si}} \tag{19}$$

Substituting the Equation (15) in the Equation (2). Potential of the full channel change along the height of channel at some casually selected channel length as 1-D surface potential analytical model and 1-D Poisson equation are calculated as given in equation (20).

$$\Psi_l(h) = W_l exp\left(\frac{h}{\lambda_l}\right) + Z_l exp\left(\frac{-h}{\lambda_l}\right) - E_l \tag{20}$$

λ_l is a constant where the value of channel length is fixed. The value of *l* arbitrary parameter changes from *l* = 0 nm to *l* = t_{si} nm. this is computed the equation (21). arbitrary constant E_l is considered in equation (22). The value of W_l and Z_l parameters are calculated by some static value of channel length.

$$\lambda_l = \sqrt{\frac{1 + Al - Bl^2}{2B}} \tag{21}$$

$$E_l = \left(\frac{qN_i}{\varepsilon_{Si}} exp\left(\frac{\Phi_{mg} - \Phi_m}{V_{th}}\right) - 2D \right) \lambda_l^2 + (Cl - Dl^2) \tag{22}$$

For calculating arbitrary constant W_l and Z_l, the surface potential at the end of source h = 0 is calculated by the Equation (23) and the surface potential at the beginning of drain h= H is calculated by the Equation (24).

$$\Psi_h(h = 0) = V_S - V_{th} ln \left(\frac{N_i exp\left(\frac{\Phi_{ms} - \Phi_m}{MV_{th}}\right)}{N_i} \right) \tag{23}$$

$$\Psi_h(h = H) = V_D + V_{th} ln \left(\frac{N_i exp\left(\frac{\Phi_m - \Phi_{md}}{V_{th}}\right) P}{N_i} \right) \tag{24}$$

Where,Φ_{ms} is work functions of source electrode, Φ_{mg} is work function of gate metal electrode, Φ_{md} is work function of drain electrode, H is channel height, V_S is source voltage and V_D are drain voltage.

all arbitrary constants putting in equation (20), the surface potential of analytical model is shown in equation (25).

$$\Psi(h,l) = \left(\frac{F_l sinh\left(\frac{H-h}{\lambda_l}\right) - G_l sinh\left(\frac{h}{\lambda_l}\right)}{sinh\left(\frac{H}{\lambda_l}\right)} \right) - E_l \qquad (25)$$

Where F_l and G_l are given by equations (26) and equation (27) respectively.

$$F_l = \Psi_h(h=0) + E_l \qquad (26)$$

$$G_l = \Psi_h(h=H) + E_l \qquad (27)$$

3.2 Surface Potential

The vertical electric field can be defining as the negative gradient of the potential. Therefore, the electric field along the channel i.e. in h direction is given in equation (28).

$$E_h(h,l) = -\frac{\partial \Psi(h,l)}{\partial h} \qquad (28)$$

The vertical electric field is calculated by the equation (29).

$$E_h(h,l) = -\left(\frac{G_l cosh\left(\frac{h}{\lambda_l}\right) - F_l cosh\left(\frac{H-h}{\lambda_l}\right)}{\lambda_l sinh\left(\frac{H}{\lambda_l}\right)} \right) \qquad (29)$$

Similarly, electric field in the transverse direction can be differentiating the surface potential with respect to l-direction given by equation (30).

$$E_l(h,l) = -\frac{\partial \Psi(h,l)}{\partial l} \qquad (30)$$

And operative field is determined by equation (31).

$$E_{mod}(h,l) = \sqrt{E_h^2 + E_l^2} \qquad (31)$$

IV.RESULTS AND DISCUSSION

A. Surface Potential

The analytical model results verified by comparing with the 2 D simulation results which performed by using SILVACO TCAD tool. Fig 2 presented the comparison between simulated surface potential profile with the analytical surface potential profile at gate voltage varies from 0.2 V to 1.0 V at fixed drain voltage Vds=1 V. With the increasing in the gate voltage, the surface potential also increases because the tunneling distance between drain and source junction is proportional to the gate-source voltage. It is also observed from the figure 2 that with the increase in the gate-source voltage, the tunneling distance will be narrower which result in increasing the tunneling probability from valance band of source to conduction band of channel. The results of simulation and analytical of surface potential are almost same.

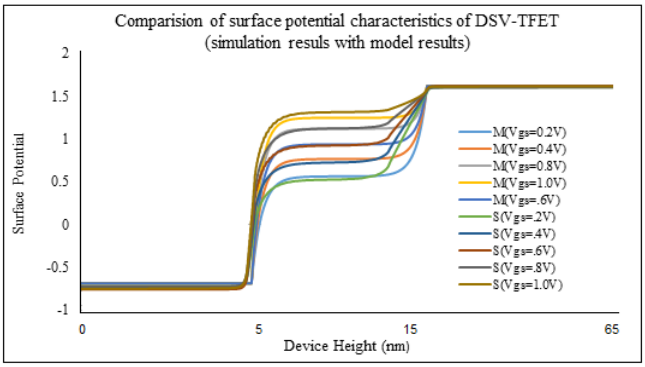

Fig. 2. The analytical and simulation results for the variation in surface potential of DSV-TFET along the channel for H=10 nm, Vgs =0.2 V to Vgs =1.0 V at Vds=1.0 V.

B. Electric Field Distribution

The simulated results of electric field distribution in the channel region shown in Fig. 3 which is is verified by the SILVACO TCAD tool.

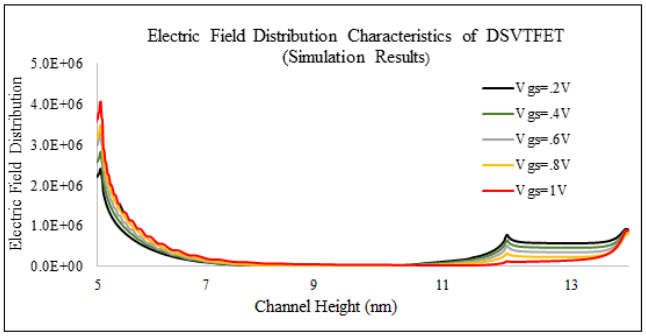

Fig.3 Electric field distribution of DSV-TFET at different values of Vgs by SILVACO TCAD simulation tool.

Figure 4 presented the comparison between simulated electric field and analytical electric field at gate-source voltage, with the variation from Vgs = 0.2 V to 1.0 V at Vds = 1.0 V. Under the OFF-state condition, the electric field is higher at drain
side and is gradually decreases with increases in gate voltage as shown in figure (3). Whereas at source-channel junction it increases with increase in gate voltage which result in increase in tunneling generation rate and increases tunneling current [16-17].

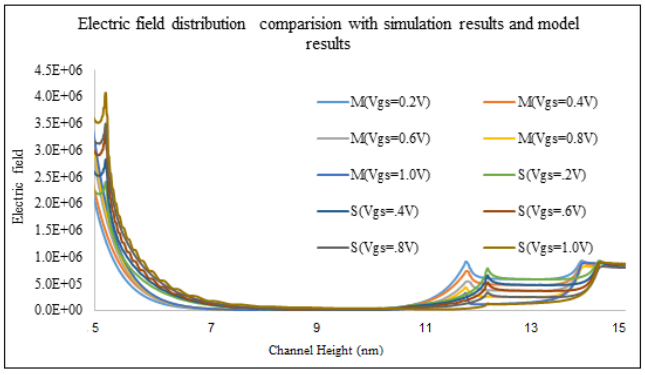

Fig. 4 The analytical and simulation results for the variation in Electric Field of DSV-TFET at Vds=1.0 V and Vgs =0.2V to Vgs =1.0V.

C. Drain current characteristics

Electric filed distribution is playing a major role in the channel for driving the drain current. It is observed from fig. 5that the ON current is recorded as 1.74×10^{-4} A/µm and OFF current recorded as 6.92×10^{-13} A/µm with I_{ON}/I_{OFF} current ratio in order of 10^8 to 10^9.

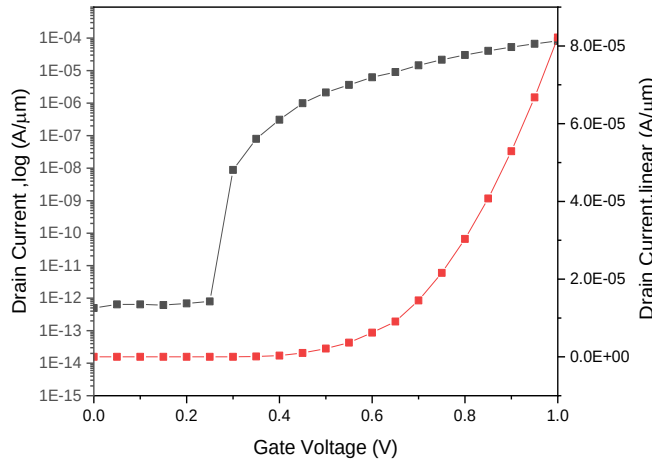

Fig. 5 Simulated Drain current characteristics of DSV-TFET at Vgs=1.0V and Vds=1.0 V

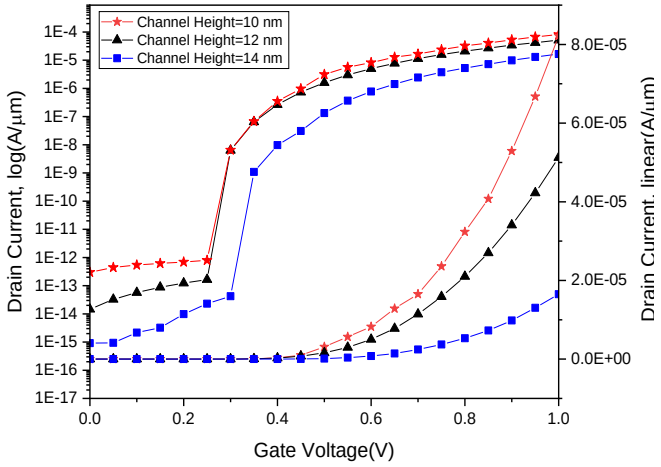

Fig. 6 Simulated Drain current characteristics of DSV-TFET for different channel height.

The impact of the variation with the channel thickness on the device characteristics at V_{ds} 1V is as shown in the figure 6. Here the channel thickness is analyzed with the variation of the 10 nm and 14 nm. It is depicted from the figure that with the increase in the value of the channel thickness there will be increase in the off-state current. This happens because of the channel thickness is thick enough, the drain field decrease the (BTBT) rate with static electric field. Thus, the off-state current will be recorded as 1.45×10^{-17} cm^{-3} for channel Height at 14 nm as shown in table 2.

TABLE 2,Performance comparison for different channel height DSV-TFET

Channel Height (nm)	V_T (V)	SS (mV/decade)	I_{OFF} (A/µm)	I_{ON} (A/µm)	I_{ON}/I_{OFF}	AVSS (mV/decade)
10	.35	12.78	2.96×10^{-13}	9.98×10^{-5}	3.33×10^{8}	39.42
12	.36	10.90	1.46×10^{-14}	5.123×10^{-5}	3.49×10^{9}	32.97
14	.44	11.33	1.45×10^{-17}	2.006×10^{-5}	1.37×10^{12}	30.52

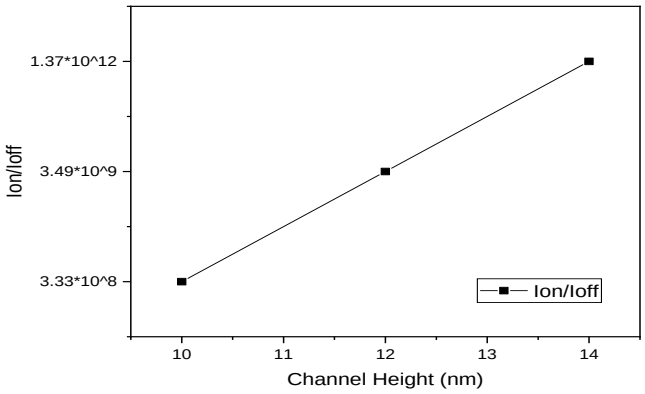

Fig.7: Transfer characteristics between channel height and I_{ON}/I_{OFF} for DSV-TFET

As the channel thickness start increasing form 10 nm to 14 nm then the I_{ON}/I_{OFF} current ratio increases proportionally as shown in figure 7.

V. CONCLUSION

The analytical model of surface potential and electric field for n type DSV-TFET has been proposed successfully. The model results are verified and validated with the 2-D simulation results obtain from SILVACO TCAD tool. The deviation in electric field distribution and surface potential with keeping drain voltage fixed at Vds=1.0 V and Vgs =0.0 V to Vgs =1.0 V.

VI. ACKNOWLEDGEMENT

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REFERENCES

1. Kahng, Dawon. "A historical perspective on the development of MOS transistors and related devices." IEEE Transactions on Electron Devices 23.7 ,655-657 (1976).
2. Moore, Gordon E. "Cramming more components onto integrated circuits." Proceedings of the IEEE 86.1 ,82-85 (1998).
3. Borkar, Shekhar. "Getting gigascale chips: Challenges and opportunities in continuing moore's law." Queue 1.7 ,26 (2003).
4. Choi, Woo Young, et al. "Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec." IEEE Electron Device Letters 28.8 ,743-745 (2007).
5. Gopalakrishnan, Kailash, Peter B. Griffin, and James D. Plummer. "I-MOS: A novel semiconductor device with a subthreshold slope lower than kT/q." Digest. International Electron Devices Meeting, IEEE (2002).
6. Khatami, Yasin, and Kaustav Banerjee. "Steep subthreshold slope n- and p-type tunnel-FET devices for low-power and energy-efficient digital circuits." IEEE Transactions on Electron Devices 56.11 ,2752-2761 (2009).
7. Kuo-Hsing, et al. "Direct and indirect band-to-band tunneling in germanium-based TFETs." IEEE Transactions on Electron Devices 59.2 ,292-301 (2012).
8. P.-Y. Wang and B.-Y. Tsui, “Band engineering to improve average subthreshold swing by suppressing low electric field band-to-band tunneling with epitaxial tunnel layer tunnel FET structure,” IEEE Trans. Nanotechnol., vol. 15, no. 1, pp. 74–79 (2016).

9. Hoefflinger, Bernd. "ITRS 2028—International roadmap of semiconductors." CHIPS 2020 VOL. 2. Springer, Cham, 143-148 (2016).
10. Neisser, Mark, and Stefan Wurm. "ITRS lithography roadmap 2015 challenges." Advanced Optical Technologies 4.4, 235-240 (2015).
11. Bhuwalka, Krishna K., Jörg Schulze, and Ignaz Eisele. "Scaling the vertical tunnel FET with tunnel bandgap modulation and gate workfunction engineering." IEEE transactions on electron devices 52.5,909-917 (2005).
12. Bhuwalka, Krishna Kumar, et al. "Vertical tunnel field-effect transistor." IEEE Transactions on Electron Devices 51.2 ,279-282 (2004).
13. Boucart, Kathy, and Adrian Mihai Ionescu. "Double-Gate Tunnel FET with High-$\kappa $ Gate Dielectric." IEEE Transactions on Electron Devices 54.7 ,1725-1733 (2007).
14. Sze, Simon M., and Kwok K. Ng. Physics of semiconductor devices. John wiley& sons, (2006).
15. Samuel, T. S., et al. "Analytical modeling and simulation of dual material gate tunnel field effect transistors." Journal of Electrical Engineering and Technology 8.6 ,1481-1486 (2013).
16. Zhao, Yijie, and Marvin H. White. "Modeling of direct tunneling current through interfacial oxide and high-k gate stacks." Solid-State Electronics 48.10 ,1801-1807 (2004).
17. Stuetzer, O. M. "Junction fieldistors." Proceedings of the IRE 40.11 ,1377-1381(1952).

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