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Impact of Resistive Open Faults on Inverter Chain and 7t Sram

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Abstract:An aggressive scaling of the technology and the increasing the number of the transistor counts are the major challenge of the design of the Integrated Circuit (IC). As well as interconnection lines and resistive opens have become a problem in modern nanometre technologies. The resistive open faults denote degradation in the connectivity within a circuit's interconnects because of unavoidable manufacturing failures in both current and developing technologies. The resistive open fault is an imperfect circuit connection that can be modelled as a defect resistor between two circuit nodes. The Resistive open faults will not cause function fault immediately. But, it will cause the delay fault and cannot employ the design of voltage to survey. In this research, find the impact of resistive open fault in the 7-Transistor (7T) SRAM cell design and inverter chain. The proposed 7T SRAM cell design and inverter chain is implemented in 45nm technology with cadence library. The main objective of this proposed research work is to efficiently detect impact of resistive open faults and reduces delay and static and dynamic power of 7T SRAM cell design and inverter chain.

Keywords: Resistive Open Fault [ROF], Delay Fault, Conductivity, Inverter Chain, 7T SRAM, Cadence tool, Area, Power, Delay.

I.INTRODUCTION

Integrated Circuit (IC) mean several number of transistors are interconnected with each other. Resistive open faults (ROFs) represents the degradation [1] [13] [14] in conductivity within a circuit's interconnects, due to inevitable manufacturing failures in both current and emerging technologies. Such type of faults mainly cause performance failures and reliability risks, whose magnitude is not only voltage-sensitive but also influenced by the electrical characteristics of the driving and driven CMOS networks.

In this work designed one inverter chain and 7T SRAM without resister and with resister by using cadence tool. First measured area, power, current and delay of inverter chain without resistor and with resistor and compared these two performances. Next measured area, power, current and delay of 7T SRAM without resistor and with resistor and compared these two performances. Finally found that resistive open fault how it effect the operation of inverter chain and 7T SRAM. And observed that delay fault caused by ROF.

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This brief is organized as follows: the inverter operation and 7T SRAM read & write operations presented in Section II and Section III. The existing method for designing of 7T SRAM discussed in Section IV. The circuit design process is also discussed. The impact of ROF on inverter chain and 7T SRAM circuits explained and discussed in Section V. Concluding remarks given in section VI.

II.INVERTER OPERATION

A. Without Resistor:

The inverter chain [2] without resistor is given fig.1. The inverter performs the transition operation such as logic 0 into logic 1 and logic 1 into logic 0. Designed a library for inverter chain with four 45nm CMOS inverters in Cadence tool. In CMOS inverter taken L: W of PMOS and NMOS transistors as 45:120 nm. The input given at first CMOS inverter and measured area, power, current, and delay.

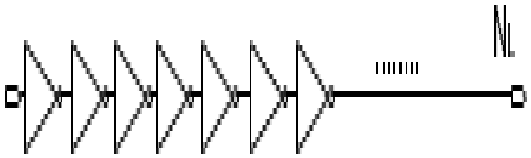

Fig. 1. Inverter chain without resistor

B. With Resistor:

The inverter chain with resistor is given fig.2. If resistive open fault induced in between cascading connection, how it effect circuit operation [3], [4] is described here. Due to this ROF causes delay fault. That means ROF changes the switching characteristics of inverter chain. Designed a library for inverter chain with resistor having four 45nm CMOS inverters in Cadence tool. In CMOS inverter taken L: W of PMOS and NMOS transistors as 45:120 nm. The input given at first CMOS inverter and measured area, power, current, and delay. And compared [5] these values with inverter chain without resistor.

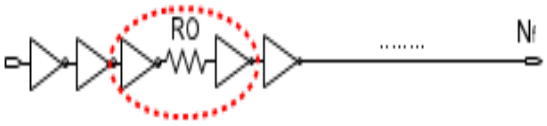

Fig. 2. Inverter chain with resistor

III.7T SRAM OPERATION

A. Without Resistor:

The 7T SRAM circuit also consists of two CMOS cross coupled to each other. In this circuit we additionally connect NMOS transistor to write line. And it also have two pass NMOS transistor connected to the bit and bit bar line. The access transistor N3 and N4 which are correspondingly connected to the write and read line to perform the write and read operation.

Before write operation the 7T SRAM [6] cell depends upon feedback connection. These feedback connection and disconnection can be performed by N5 transistor.

1. Write Operation:

The write operation can be start by turning off the N5 transistor to this cut off feedback [7] connection. When N3 is on and N4 is off the bit line bar carries complement of input data. The N5 is turned on and WL is turned off for reconnect the feedback connection to store new data. The bit line bar is discharged to "0" for storing "1" in the cell. And there is no need to discharge bit line for storing "0" in the cell.

2. Read Operation:

When performing the read operation both read and word lines are turned to on and also the transistor N5 is kept on.
The library of 7T SRAM without resistor designed in cadence tool. For this design required total 7 transistors and each transistor L: W is 45: 120 nm. By setting inputs performed read and write operations and measured area, power, current and delay. The 7T SRAM circuit is shown in fig.3.

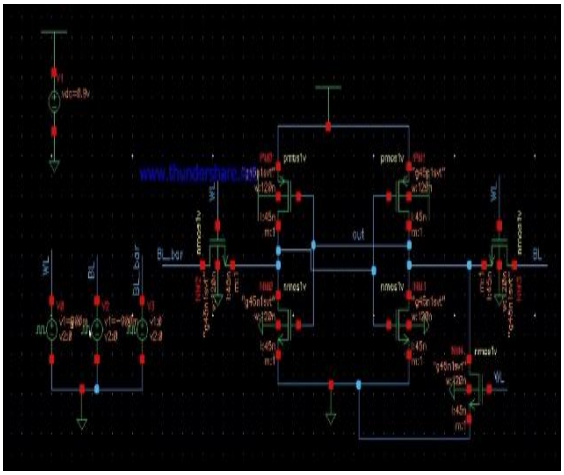

Fig. 3. 7T SRAM without resistor

B. With Resistor:

The library of 7T SRAM with resistor designed in cadence tool. For this design required total 7 transistors and each transistor L: W is 45: 120 nm. In this design added unwanted resistor in the circuit and assumed it as a Resistive Open Fault [ROF]. Due to this ROF causes delay fault and it effects the read and write operations of 7T SRAM. By setting inputs performed read and write operations and measured area, power, current and delay. And these all values compared with the 7T SRAM without resistor. The 7T SRAM circuit is shown in fig.4.

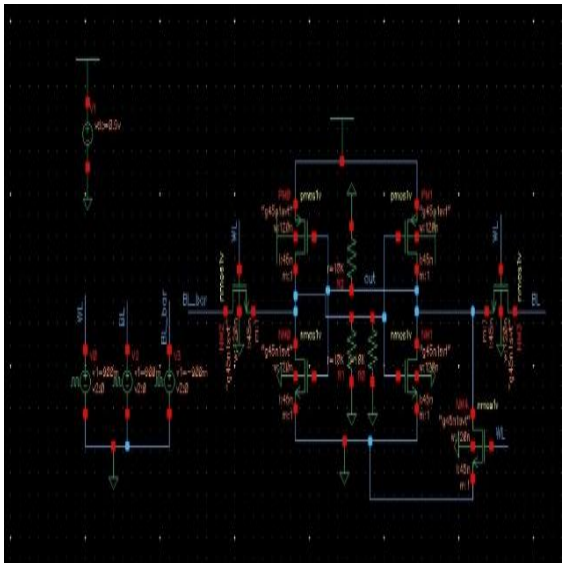

Fig. 4. 7T SRAM with resistor

IV.EXISTING METHOD

The SRAM memory cell with Resistive Open Faults is shown in Fig 5. The SRAM cell-1 [8] write concept depends on cutting off the feedback connection between the two inverters, before the write operation. In this SRAM Cell used 6 transistors are connected with 6 different resistors assumed as Resistive Open Faults [ROFs]. The electrical simulations of these all resistive open faults performed with the Infineon Internal SPICE Simulator. For reducing of simulation time, the simulations are performed on simplified version of the memory circuit that includes a reduced set of the core cells. The simulation [11] [12] performed by setting V_{DD} as 1.6V. That detect all six resistive open faults. This simulation results describes that, Due to these Resistive Open Faults mainly causes transition fault also referred as delay fault. If ROF values increases the delay also increases. If ROF having maximum value it referred as Stuck-Open-Fault and there is no conduction in between two nodes.

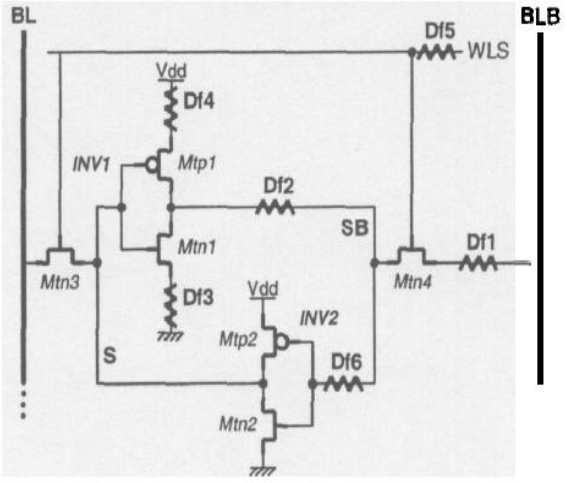

Fig. 5. SRAM Memory Cell with Resistive Open Faults.

V.RESULT

The simulation results of inverter chain without resistor, inverter chain with resistor, 7T SRAM without resistor and 7T SRAM with resistor is given here.

The comparison table of area, power, current, delay of these all circuits given in tables. These results describes that ROFs effects the circuit operation and it changes these all parameters.

A. Power Analysis:

The calculated power given in table.1. Table 1 shows the power values of inverter chain and 7T SRAM, it changes if ROFs induces in the circuit.

Table.1.

Circuits	Power (uW)
Inverter chain-ROF	0.111
Inverter chain	**0.0656**
7T-SRAM-ROF - Read	53.270
7T-SRAM - Read	**27.974**
7T-SRAM-ROF - write	60.004
7T-SRAM - write	**27.597**

B. Current Analysis:

The calculated current [15] given in table.2. The ROFs degrades the conductivity and causes and it is shown in below table.

Table.2.

Circuits	Current (uA)
Inverter chain-ROF	0.123
Inverter chain	**0.0729**
7T-SRAM-ROF - Read	59.189
7T-SRAM - Read	**31.082**
7T-SRAM-ROF - write	66.67
7T-SRAM - write	**30.663**

C. Delay Analysis:

The Resistive Open Faults degrades the conductivity. Due to this causes delay fault. The delay of the inverter chain, 7T SRAM [10] with and without resistor given in below table.3.

Table.3.

Circuits	Delay (nS)
Inverter chain-ROF	0.102
Inverter chain	**0.01**
7T-SRAM-ROF - Read	0.2
7T-SRAM - Read	**0.04**
7T-SRAM-ROF - write	0.3
7T-SRAM - write	**0.02**

The inverter chain circuit diagram without and with resistor shown in fig.6. , fig.7. The output waveforms of inverter chain without and with resistor is shown in below fig.8. , fig.9. The 7T SRAM circuit diagram with and without resistor is shown in fig.10. , fig.11. Designed by Cadence tool. The output waveform of 7T SRAM read operation with and without resistor shown in fig.12. , fig.13. The output waveform of 7T SRAM write operation with and without resistor shown in fig.14. , fig.15.

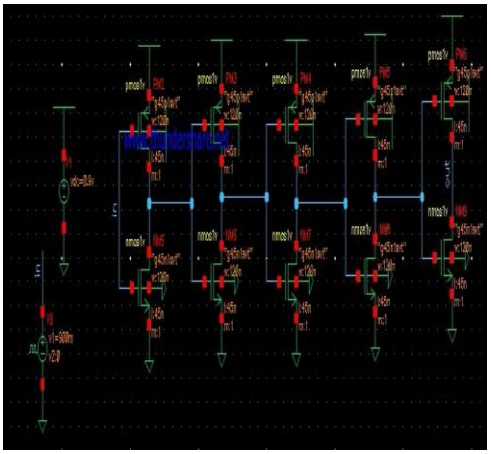

Fig.6. Inverter Chain without Resistor

The power and delay of 7T SRAM is given in one paper [16] as a 4.87 nW and 3.7 ns. Here by comparing of these values with proposed system, the proposed system decreases the power value to 27.974 and delay value to 0.04 ns. The dattaprasad madur [17] given 3D integrated 40nm CMOS Inverter circuit. This 3D integration process is cost effective and scaling process causes leakage power.

Manjeet Kumar [18] designed 65 nm CMOS Inverter and not explained clearly about rise & fall time. Kariyappa B S [19] measured delay of 45nm 7T SRAM as 139.3 ps and mainly concentrated on only Static Noise Margin [SNM]. Saurabh Khandelal [20] also designed 45nm 7T SRAM by using FinFET technology and measured delay as 0.2 ns for read operation.

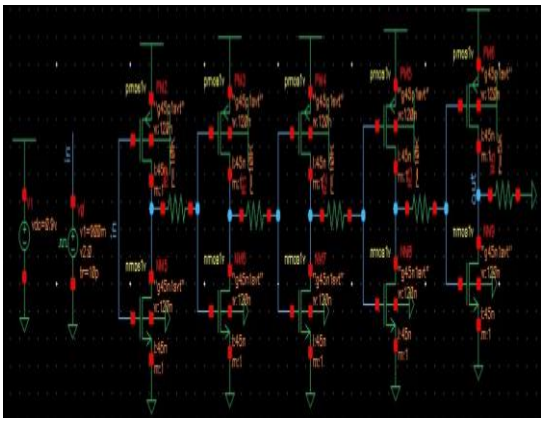

Fig.7. Inverter Chain with Resistor

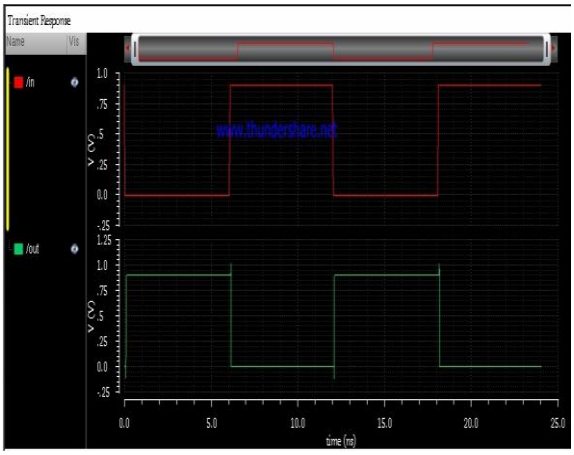

Fig.8. Output of Inverter Chain without resistor

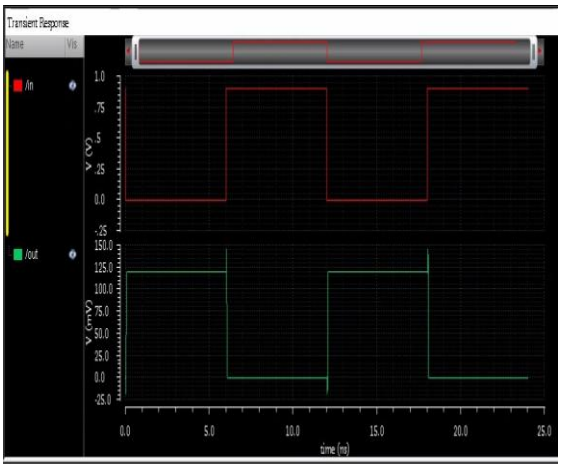

Fig.9. Output of Inverter Chain with resistor

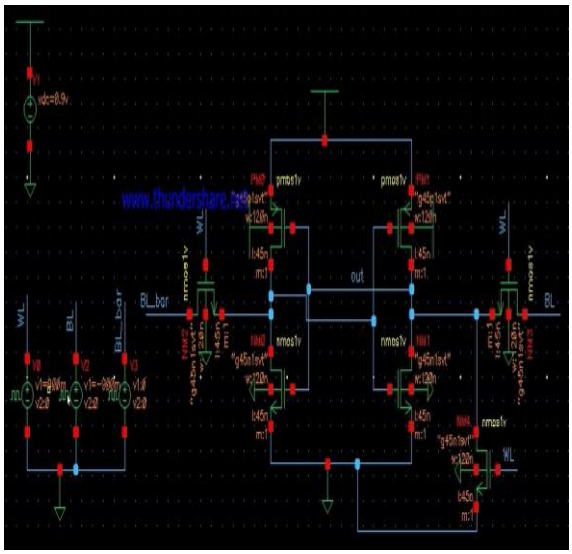

Fig.10. 7T SRAM without Resistor

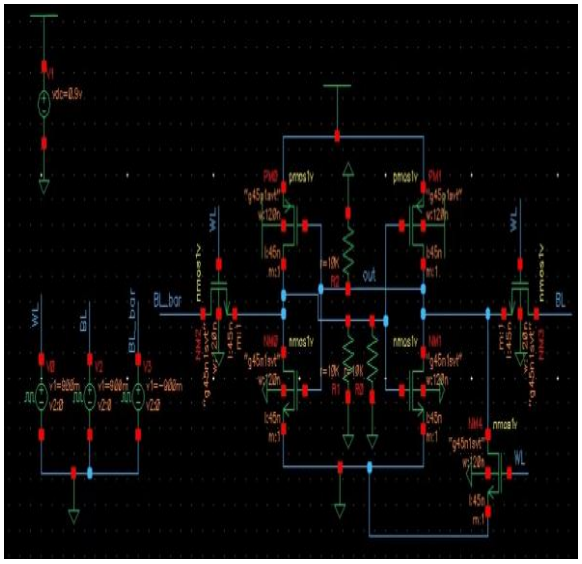

Fig.11. 7T SRAM with Resistor

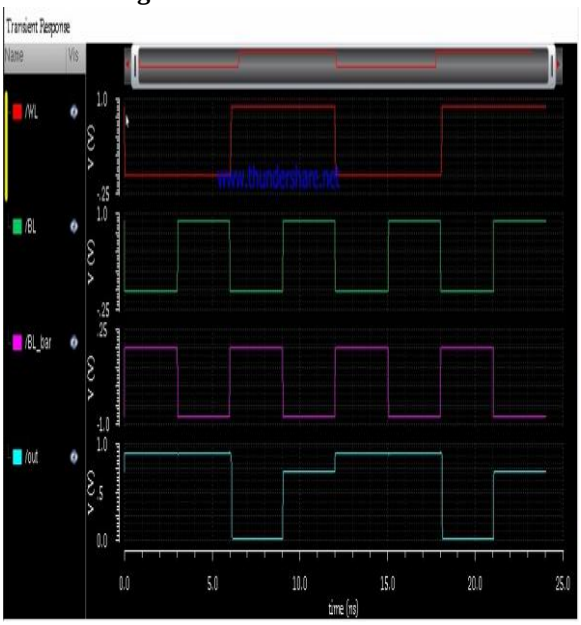

Fig.12. Output waveform of 7T SRAM read operation without Resistor

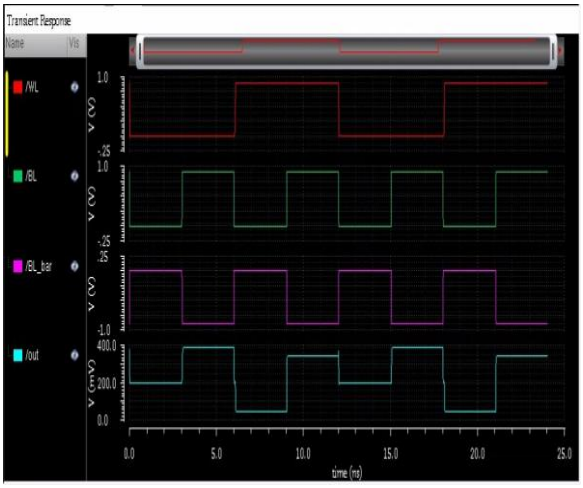

Fig.13. Output waveform of 7T SRAM read operation with Resistor

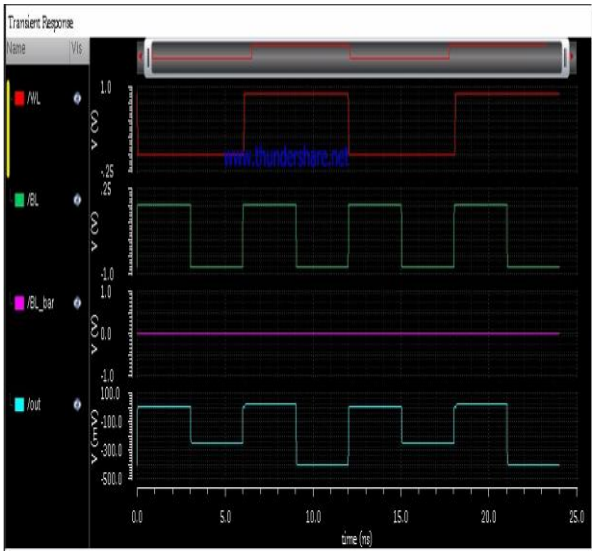

Fig.14. Output waveform of 7T SRAM write operation without Resistor

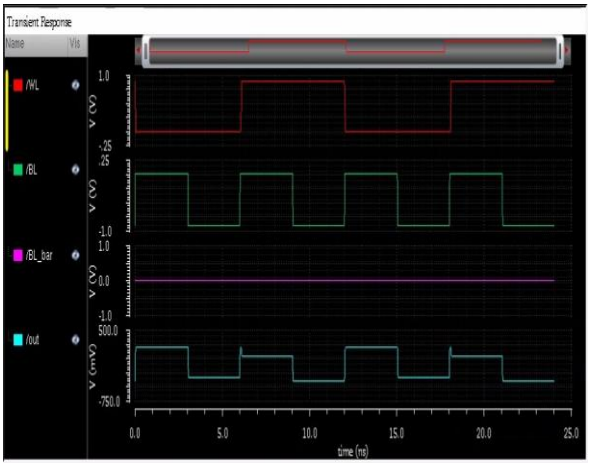

Fig.15. Output waveform of 7T SRAM write operation with Resistor.

VI.CONCLUSION

The ROF degrades the conductivity in the circuit and causes delay fault. This work shows the effect of ROF on the inverter chain and 7T SRAM. This proposed work gives comparison of 45nm inverter chain, 7T SRAM operations without resistor and with resistor. The ROF reduces the conductivity so the drives low current and increases delay in inverter chain and 7T SRAM.

REFERENCES

1. Arumí, Daniel, Rosa Rodríguez-Montañés, and Joan Figueras. "Test Escapes of Stuck-Open Faults Caused by Parasitic Capacitances and Leakage Currents." IEEE Transactions on Very Large Scale Integration (VLSI) Systems 24, no. 5 (2016): 1739-1748.
2. Zhong, Shida, Saqib Khursheed, Bashir M. Al-Hashimi, and Wei Zhao. "Efficient variation-aware delay fault simulation methodology for resistive open and bridge defects." IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 33, no. 5 (2014): 798-810.
3. Azevedo, Joao, Arnaud Virazel, Alberto Bosio, Luigi Dilillo, Patrick Girard, Aida Todri-Sanial, Jérémy Alvarez-Hérault, and Ken Mackay. "A complete resistive-open defect analysis for thermally assisted switching MRAMs." IEEE Transactions on Very Large Scale Integration (VLSI) Systems 22, no. 11 (2014): 2326-2335.
4. Mohammadat, Mohamed Tagelsir, Noohul Basheer Zain Ali, Fawnizu Azmadi Hussin, and Mark Zwolinski. "Multivoltage aware resistive open fault model." *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 22, no. 2 (2014): 220-231.
5. Yu, Changgeng, Guixiong Liu, and Liping Lai. "Diagnosis of Resistive-Open Defects using IDDT in Digital CMOS Circuits."WSEAS TRANSACTIONS on CIRCUITS and SYSTEMS Volume 13, 2014.
6. Mr. Kariyappa B S, Mr. Basavaraj Madiwalar, Mrs. Namitha Palecha. "A Comparative Study of 7T SRAM Cells". IJCTT Volume 4 Issue 7, 2013.
7. Mr.S.Mohamed Sulaiman, Dr.B.Jaison "Performance of 7t Sram Using Triple Threshold Voltage CMOS Technology" IJPAM Volume 119 Issue 15, 2018.
8. Luigi Dilillo, Patrick Girard "Resistive-Open Defects in Embedded SRAM core cells: Analysis and March Test Solution" IEEE, 1081-7735/04, 2004
9. Pankaj Agarwal, Nikhil Saxena "Low Power Design and Simulation of 7T SRAM Cell using various Circuit Techniques" Volume4Issue5-May 2013.
10. 10. Joel R, Gnana Sarvanan S "Power and Stability Analysis of 6T 7T Sram Cell Using Power Gating Techniques" IJIRT Volume 3 Issue 8, 2017.
11. L. Dilillo, P. Girard "New March Elements for Address Decoder Open and Resistive Open Fault Detection in SRAMs", Journal Integrated Circuits and Systems 2008; v.3 / n.1:7-2012.
12. Changgeng Yu, Guixiong Liu "Diagnosis of Resistive-Open Defects using IDDT in Digital CMOS Circuits", WSEAS TRANSACTIONS on CIRCUITS and SYSTEMS, E-ISSN: 2224-266X, Volume 13, 2014.
13. Mohamed Tag Eisir Mohammadat, Noohul Basheer Zain Ali "Detectability Analysis for Resistive Open Faults with Dynamic Supply Voltage Scaling Awareness", IEEE, 978-1-4577-0144-3/11.2011.
14. Mohamed Tagelsir Mohammadat, Noohul Basheer Zain Ali "Multi-Voltage Aware Resistive Open Fault Model", IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 22, NO. 2, FEBRUARY 2014.
15. James Chien-Mo Li, Edward J. McCluskey "Diagnosis of Resistive-Open and Stuck-Open Defects in Digital CMOS ICs", IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, VOL. 24, NO. 11, NOVEMBER 2005.
16. Shital Joshi and Umar Alabawi, "Comparative Analysis of 6T, 7T, 8T, 9T, and 10T Realistic CNTFET Based SRAM", Journal of Nanotechnology Volume 2017, Article ID 4575013.
17. Dattaprasad Madur and Dr.Deepak Bhoir "Three Dimensional Integration of CMOS Inverter", IJECET, Volume 5, Issue 11 November 2014.
18. Manjeet Kumar, "A Study of CMOS Inverter using 65nm Technology", IRJET Volume 04, Issue 10 October 2017.
19. Kariyappa B S and Basavaraj Madiwalar, "A Comparative Study of 7T SRAM Cells", IJCTT, Volume 4, Issue 7 July 2013.
20. Saurabh Khandelwal and Dr. Balwinder Raj, "Leakage Current and Dynamic Power Analysis of Finfet Based 7T SRAM at 45nm Technology", ACIT 2013.

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