High-Resolution DPWM for DC-DC Buck Converter using Sigma-Delta Modulation Techniques

Shubha Rao K, Veena S Chakravarthi

Abstract— in this paper, a 13-bit hybrid DPWM structure which consists of a second-order Σ-Δ modulator having 6-bit resolution and a counter-comparator block with the 7-bit resolution is designed. The Σ-Δ modulator is based on error feedback concept which increases the effective resolution of DPWM by 6-bit and at the same time reduces clock power requirements and noise disturbances. The timing simulation waveforms of the designed DPWM architecture are verified and PWM pulses of the desirable duty cycle are generated. The Σ-Δ modulator based DPWM is used to drive the power MOSFETs of switching buck converter and Inductor current output voltage waveforms are observed. Ripple quantities of 17.5% and 0.07% are obtained for Inductor current and output voltage which are within the upper limits of 20% and 1% respectively. The steady value of the output voltage obtained is 0.99955V. The result obtained validates the Hybrid DPWM design.

Keywords: Buck converter, digital control, sigma-delta modulator, high resolution.

I. INTRODUCTION

In a digitally controlled power supply system, the power converter is an analog /continuous signal system whereas the controller is a digital system. Therefore an interface system is required to transform the continuous signal to discrete signal or vice versa. Two such devices employed in power converter systems are the Analog-to-Digital Converter (ADC) and Digital Pulse Width Modulator (DPWM) equivalent to the Digital-to-Analog Converter (DAC). Fig.1 shows the digitally controlled buck converter system. The output voltage V_{out} is converted into digital by ADC and is compared with a digital reference signal and the error signal which is digital in nature is generated. The compensator block generates a discrete signal which is proportional to the duty ratio. This discrete is given to DPWM block wherein the discrete signal is converted back into an analog signal to drive the switches of the buck converter, to maintain the output voltage constant such that V_{out} conforms to the reference value V_{ref}.

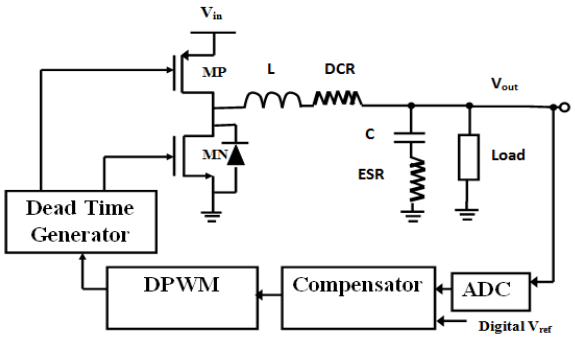

Fig.1 Digital control of buck converter

One of the most important blocks in digitally controlled SMPS is DPWM and its main function is to generate PWM pulses to control on-off of the power MOSFET to obtain the desired output voltage. A high-resolution DPWM is necessary to achieve precise voltage and avoid undesirable quantization effects such as limit-cycle oscillations. The chosen DPWM architecture should ideally minimize both area and power consumption. Hence a lot of research work in the field of DPWM focuses on realizing high-resolution architecture with the minimum area and power requirement

The paper [1] discusses the presence of steady-state limit cycles in digitally controlled PWM converters and it employed Single-phase and multi-phase controlled digital dither for increasing the effective resolution of the DPWM block. In [2] DPWM duty-cycle command was pre-processed by a multi-bit digital sigma-delta modulator and resulted in the reduction of total quantization noise at the output of the dc-dc converter while increasing the effective resolution of the DPWM in the control loop. A fully synthesizable hybrid DPWM with digital Delay Locked Loop (DLL) suitable for FPGA or custom chip implementation is introduced [3] and implemented the DPWM based on trailing, leading or triangular modulation. A high-resolution DPWM utilizing the carry flag delay time to achieve resolution as high as 70ps is presented in [4]. The paper [5] proposed two novel fully-Synchronous High-Resolution PWM implementations using different FPGA resources: the Digital Clock Management (DCM) and the I/O delay element (IODELAYE1). Very simple, high-resolution high-frequency DPWM architecture suitable for implementation in standard low-cost FPGAs is proposed in

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[6] which does not require manual placement or routing efforts and was demonstrated through a 50-MHz switching frequency, 8-bit, 60ps resolution DPWM, as well as through a 1MHz, 14-bit hybrid DPWM with 90-ps resolution with excellent monotonicity and linearity. Summarizing Digital Dither, Σ-Δ modulation, FPGA resources such as DLL, DCM and propagation delays through carrying chains are the techniques used in the design and implementation of DPWM. High resolution, small area, and low power are the parameters to analyze the performance of the DPWM architecture.

In this paper, a 13-bit DPWM structure which consists of a second-order Σ-Δ modulator having 6-bit resolution and a counter-comparator block with the 7-bit resolution is designed for a buck converter. The Σ-Δ modulator is based on error feedback concept which increases the effective resolution of DPWM by 6-bit and at the same time reduces clock power requirements and noise disturbances. The hardware-software co-simulation is performed to validate the design.

This paper is organized as follows. Section II describes the design of 13-bit Σ-Δ Modulator DPWM for a buck converter. The design of the buck converter is given in section III. The modeling and results are discussed in section IV. Finally, conclusions are drawn in section V.

II. DESIGN OF 13-BIT Σ-Δ MODULATOR DPWM

One of the most important blocks in digitally controlled SMPS is Digital Pulse Width Modulation (DPWM). The main function of DPWM is to generate PWM pulses to control the on-off of power MOSFET to obtain the desired output voltage [9]. A high-resolution DPWM is necessary to achieve precise output voltage and avoid limit-cycle oscillations. In order to increase resolution and reduce power consumption simultaneously, hybrid DPWM structures are utilized. In this paper, a 13-bit DPWM structure which consists of a second-order Σ-Δ modulator having 6-bit resolution and a counter-comparator block with the 7-bit resolution is designed to ease or lessen the requirement of high clock frequency and hence reduce power consumption. Fig.2 shows the proposed architecture.

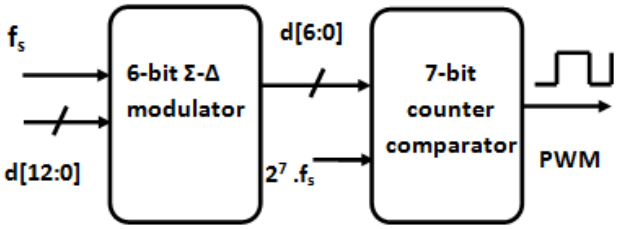


Fig.2 Structure of proposed Σ-Δ DPWM structure

Counter comparator DPWM Architecture

The counter-comparator DPWM is one simple hardware method to achieve digital-to-time conversion in core DPWM [10]. It uses a cyclic counter and two comparators, setting a set-reset (SR) latch high when the counter value is zero and low when the counter reaches the control duty value D. This scheme has the advantage of a simple structure and excellent linearity in digital to time-domain conversion. It needs $2^N \cdot f_s$ clock to achieve an N-bit DPWM at switching frequency f_s. However, when operating at the high-frequency f_s, it has the drawback of very high power consumption. Fig.3 shows the structure of counter-comparator DPWM.

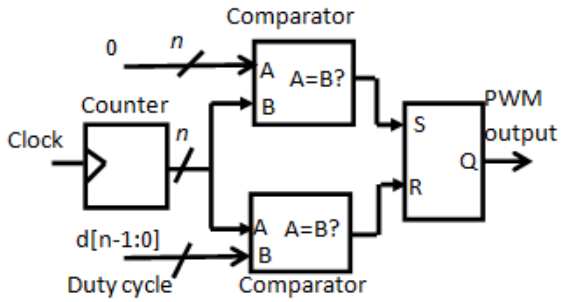


Fig.3 counter-comparator DPWM

A second order error feedback type Σ–Δ modulator

For DPWM application, the function of loop architecture of Σ–Δ modulator is to reduce the resolution of the large bit input signal to a few bit values without significant quantization error in the process. Fig.4 shows the architecture configuration of an error feedback filter Σ–Δ modulator for DPWM [8]. The discarded LSBs (error e) are filtered and fed back to the input port. The filter *He* generally is a delay or integrator block. From Fig.4, output signal R (z) can be written as:

$$R(z) = U(z) + [1 - He(z)].E(z)] \quad (1)$$

Where E(z) is the quantization error of truncation. Assuming *He* is a delay block, From equation (1) it can be seen that STF=1, and NTF=1-He(z) in the digital signal process. This equation shows how the transfer function NTF influences the truncated signal.$||He|| \approx 1$ under zero frequency condition, i.e. loop filter has infinite gain. Hence $||NTF(z)|| << 1$ and noise can be eliminated drastically. The output PWM signal becomes approximately equal to the input PWM signal as $R(z) \approx U(z)$. Therefore the high-resolution PWM input signal is almost unchanged, the quantization error is suppressed[10][11].

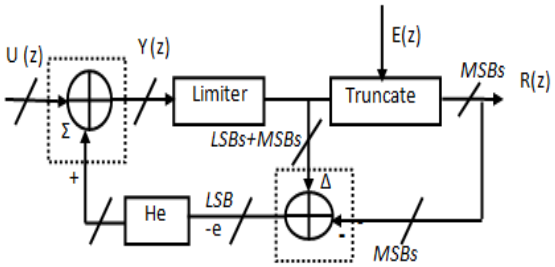


Fig.4 Error feedback type single stage Σ–Δ modulator for DPWM

The Signal Noise Ratio (SNR) and Effective Number of Bits (ENOB) of a second order Σ–Δ modulator is given by

$$SNR = 6.02\, N_{DPWM} - 11.14 + 50 \log(OSR) \quad (2)$$

$$ENOB = N_{DPWM} - 2.14 + 8.31 \log(OSR) \quad (3)$$

Where OSR is the oversampling ratio and is given $f_s/(2f_b)$, f_s is the switching frequency of the power converter circuit and f_b is the bandwidth of the compensator and N_{DPWM} is the number of bits in the low-resolution core counter-comparator DPWM. In this paper N_{DPWM} is 7 bit, switching frequency is 10MHz and bandwidth of the compensator is fs/20.With

these values, from equation (2) and (3), the SNR and ENOB obtained are 81 dB and 13.14 respectively. Hence a 6-bit Σ-Δ modulator is implemented in the proposed DPWM architecture. In fig.4, the signal U (z) is a high-resolution 13-bit digital signal from the compensator whereas R(z) is a low-resolution 7-bit signal which will be the input to the core DPWM. The truncate block will shorten its input signal to few MSB bits i.e 7-bit which will be the input to the core DPWM. The error signal is 6-bit LSBs which will be feedback through the integrator or delay block which forces its average value to zero. The function of the limiter is to limit the error to an acceptable level to the PWM process. The architectural configuration of second-order error feedback type Σ–Δ modulator is as shown in fig.5.The architecture consists of few adders and delay blocks, a multiplier, a truncation block.

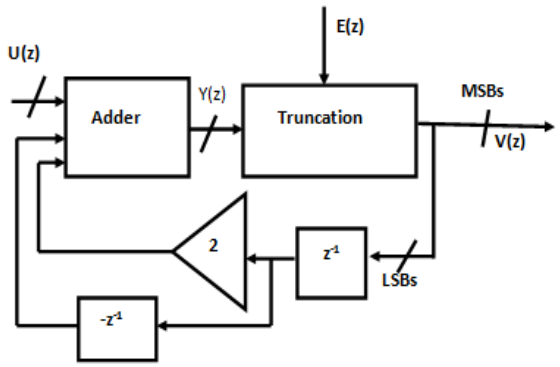


Fig.5 A second order error feedback implementation of Σ–Δ modulator.

III. DESIGN OF BUCK CONVERTER

The Σ–Δ modulator DPWM is designed to drive the switches of a synchronous buck converter. A DC-DC buck converter topology which converts a voltage of 3.2V to 1V operating in the continuous current mode (CCM) at 10MHz switching frequency is designed and a constant switching frequency pulse width modulation (PWM) technique is applied in voltage control mode to provide a stable supply voltage to a load. Fig.6 illustrates the circuit and basic components for a buck converter.

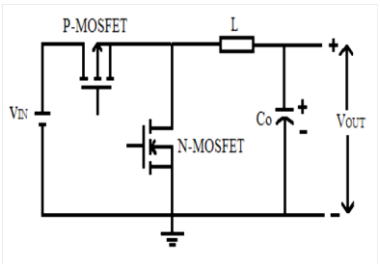


Fig.6 The synchronous buck converter circuit

Considering 20% current ripple, 1% voltage ripple and 5% maximum output voltage overshoot, the synchronous buck converter is designed. A MATLAB program is written to find the values of the LC filter. Table I shows the main specifications of the synchronous buck converter.

TABLE I. BUCK CONVERTER SPECIFICATIONS

Parameter	Minimum	Nominal	Maximum
Input Voltage (V_{in})	1.8 V	3.2 V	3.6V
Output Voltage (V_{out})	0.9V	1 V	1.2V
Output current(I_{out})	2mA	-	800mA
Switching frequency (f_s)	-	10MHz	-
Output inductor (L)	-	1uH with DCR=1mΩ	-
The output capacitor (C)	-	2uf with ESR=9mΩ	-

IV. RESULTS

Fig.7 shows the structural view of the proposed Σ–Δ modulator based DPWM. The effective resolution of the 7-bit core DPWM is increased to 13-bit by 6-bit Σ–Δ modulator by using noise shaping concept. The proposed hybrid Σ–Δ modulator based DPWM is modeled in the digital domain using Xilinx system generator tool and timing simulation is performed to verify the design. Fig.8 shows the modeling of Σ–Δ modulator based DPWM driving a buck converter in Simulink tool. The Σ–Δ modulator based DPWM is designed using Xilinx system generator tool and co-simulation is performed to validate the design. Fig 9 shows the simulation timing waveforms of PWM output for a 13-bit duty cycle with a value of 0.3125.

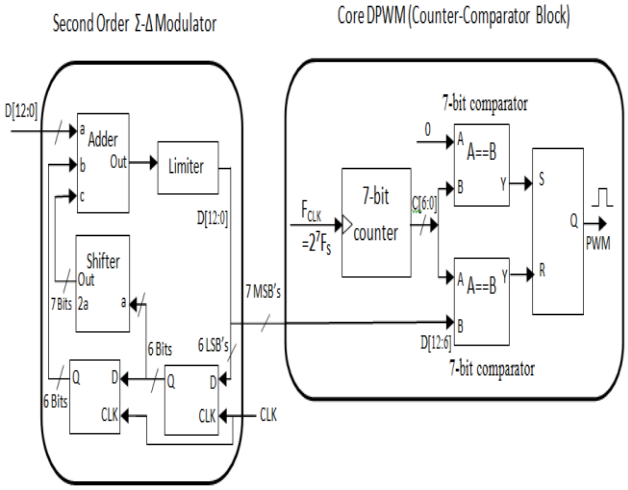


Fig.7 Structural view of Σ–Δ modulator based DPWM

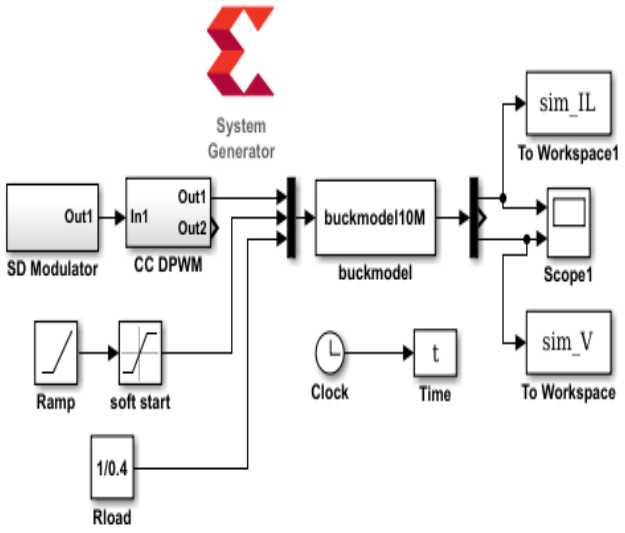


Fig.8 modeling of Σ–Δ modulator based DPWM driving a buck converter

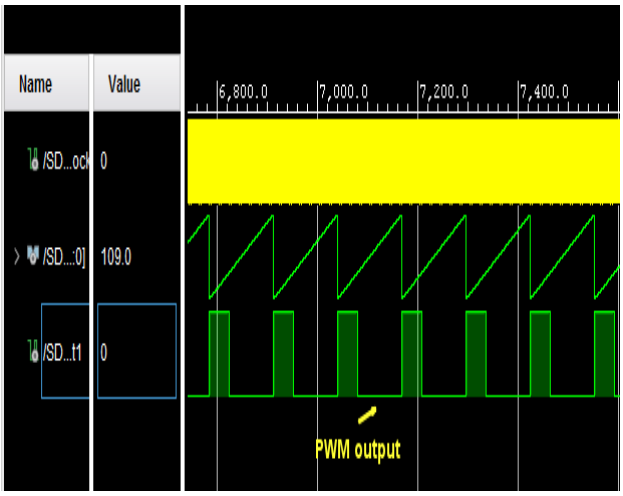
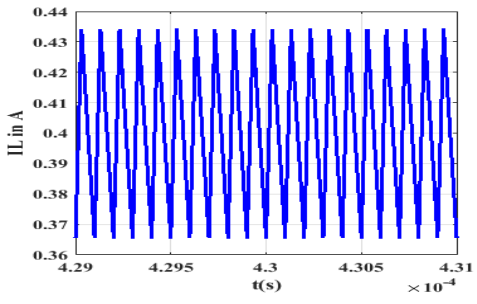
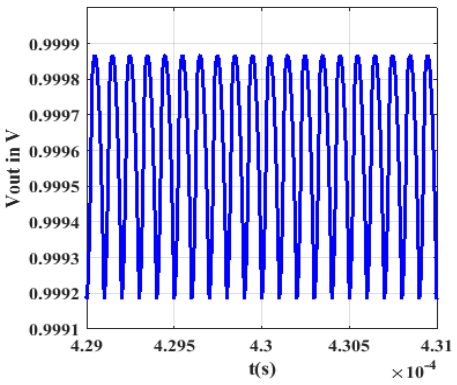


Fig.9 Timing simulation PWM output of Σ–Δ modulator DPWM

The hybrid Σ-Δ modulator based DPWM designed is connected to drive the buck converter with a duty cycle value of 0.3125 and output voltage and Inductor current waveforms are observed. The power supply is operated in open loop configuration. The ripple observed in Inductor current and output voltage is 15.5% and 0.07% which are within the limits of 20% and 1% respectively. The steady value of output voltage and current are 0.99955 V and 0.4A respectively. Fig.10(a)-(d) shows ripples and steady values of Inductor current and output voltage.



(a)



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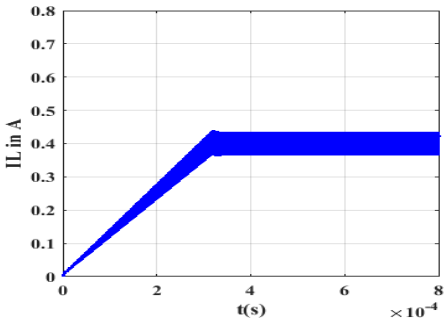
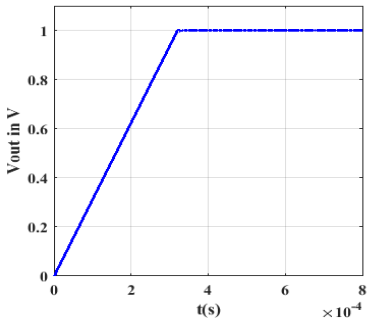


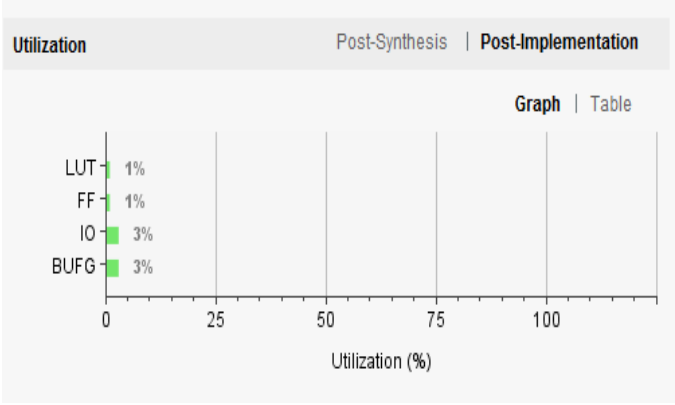
(c)



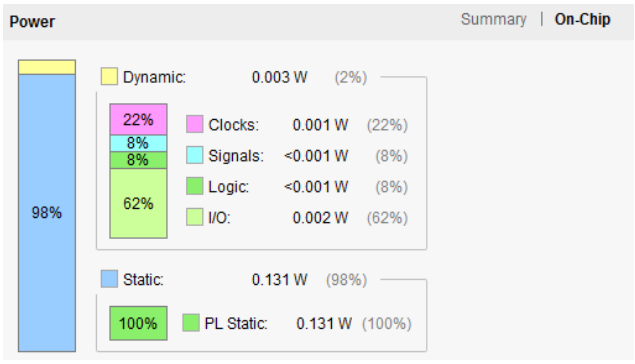
(d)

Fig.10 (a) current Ripple (b) voltage Ripple (c) Inductor current (d) output voltage waveforms.

The designed Σ–Δ modulator based DPWM is synthesized and implemented in FPGA using Xilinx vivado tool. Fig.11 (a),(b) and (c) shows the utilization, timing and power report generated during synthesis of the design.



(a)



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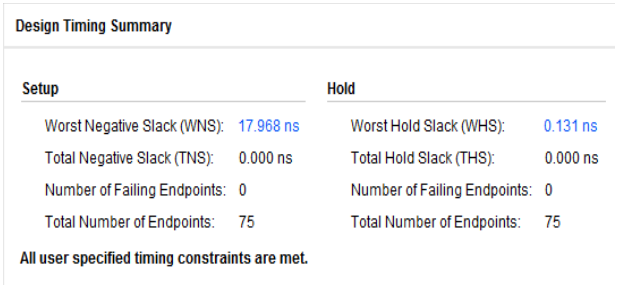

(c)

Fig.11(a) utilization report (b) power report (c) timing report

V. CONCLUSIONS

In this paper, a 13-bit hybrid DPWM structure which consists of a second-order Σ-Δ modulator having 6-bit resolution and a counter-comparator block with the 7-bit resolution is designed. The Σ-Δ modulator is based on error feedback concept which increases the effective resolution of DPWM by 6-bit and at the same time reduces clock power requirements and noise disturbances. The timing simulation waveforms of the designed DPWM architecture is verified and PWM pulses of the desirable duty cycle are generated, The Σ-Δ modulator based DPWM is used to drive the power MOSFETs of switching buck converter and Inductor current and output voltage waveforms are observed. Ripple quantities of 17.5% and 0.07% are obtained for Inductor current and output voltage which are within the limits of 20% and 1% respectively. The steady value of the output voltage obtained is 0.99955V. The results obtained validate the Hybrid DPWM design..

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