Harmonic Reduction of Shunt Active Power Filter using SVPWM

Sh Suresh Kumar Budi, R.Kiranmayi

Abstract:- waveforms of voltage and current are distorted and requirement of reactive power increase due to developing use of non-linear and time-varying loads. Harmonic distortion is recognized to be sources of a number of problems, such as increase in power losses, unnecessary heating, harmonic resonances in the utility, communication obstruction, flash and clear noise, inaccurate operation of susceptible loads [1, 2].

Conventionally, LC tuned passive filters absorb generated vocal currents due to nonlinear loads. Their primary benefit is more reliability with reduced cost. However, passive filters have a number of demerits like which may be the source of harmonic interface with the utility system, in the existence of inflexible value of fine-tuning LC filter is necessary and could not meet the predetermined harmonic current restrictions [3, 4]. This gives the inspiration to the exploration of an active power filter methodology, which is sensibly viable, cost valuable and can gather the suggested standard for large power nonlinear loads. Due to the high rating and large switching-frequency constraint of the Pulse Width Modulation (PWM) inverters are used for high-power applications.

Keywords— Shunt Active Filter(SAF), Voltage Source Inverter(VSI), Space Vector Pulse Width Modulation (SVPWM)

1. INTRODUCTION

This paper studies power translation systems with transformer less active filter. Among a variety of methodologies the shunt active filter in associate with Voltage Source Inverter (VSI) is the mainly familiar because of its high efficiency [5]. The adoptive control approaches decide performance of the active filter. An active power filter controller is of mainly of two parts. The first is used to stable DC bus voltage to constant by determining the reference current of APF. These reference currents obtained by different methods, like instantaneous reactive power method, synchronous reference frame theory, supplying current regulation and etc., with the help of load current or the mains current. The second is used to inject the compensating current into AC mains with control of VSI. The commonness of these techniques is to control VSI with the difference between fundamental and reference currents.

A substitute control technique for shunt APF's is presented in this paper [6]. The presented technique differs from formerly proposed methodologies in the following ways: a) for an APF a reference voltage vector is generated instead of reference current; b) Space Vector Pulse Width Modulation (SVPWM) [7, 8] is used to generate reference voltage for generating preferred output voltage of APF. Therefore, the proposed technique is easy and simple. The ideal standard of this technique is discussed in aspect in this paper and proved its authority by results in simulation.

II. SVPWM

A. Principle of svpwm

Initially on the basis of space vector representation a three-phase inverter is presented. The three-phase VSI is recreated in Fig. 1. by controlling the switching variables a, a', b, b', c and c' six power switches S1to S6 that form the output. a', b', or c' is 0 when an superior transistor is switched on. Consequently, the output voltage can be found by the on and off states of the superior switches S1, S3, S5.

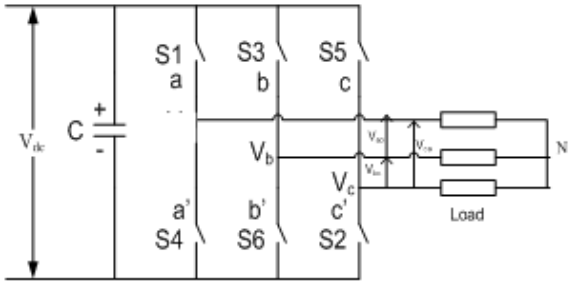

Fig 1 3Ø VSI

The vector of line voltage being given by

$$\begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} = V_{dc} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \quad (1)$$

Where [a, b, c]t is switching variable vector

[Va Vb Vc]t is phase voltage vector is expressed as.

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = \frac{V_{dc}}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \quad (2)$$

As represented in Fig 1, for three upper power switches there are eight possible combinations of on and off. The 8 switching vectors, output phase voltage, and output line voltages represented in provisions of DC-link voltage Vdc are indicated in (1) and (2).

The voltage equations in the abc reference theory can be malformed into the fixed d-q reference theory for actualize SVPWM that consists of the parallel (d) and perpendicular (q) axes as depict in Fig.2.

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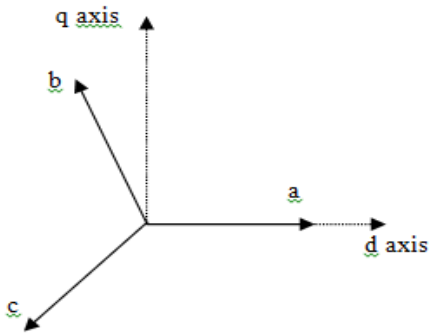


Fig.2 abc reference frame and stationary d-q reference frame

The relation from the figure is given as

$f_{dq0} = K_s f_{abc}$

where, $k_s = \frac{2}{3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/2 & 1/2 & 1/2 \end{bmatrix}$, (3)

$f_{dq0} = [\, f_d \; f_q \; f_0 \,]^T$, $f_{abc} = [\, f_a \; f_b \; f_c \,]^T$, and represents any voltage variable or current variable

As portrayed in Fig.2, this conversion is identical to a symmetrical protrusion of [a, b, c]t onto the 2-dimensional vertical to the vector [1, 1, 1]t in a 3-dimensional organize system. 6 active and 2 zero vectors are produced from the above results. Six active vectors (V1 - V6) contour the axes of a hexagonal as portray in Fig.3, and provide electric power to the system. The phase angle is 60 degrees among any 2 adjacent active vectors. In the interim, at the origin there are 2 zero vectors (V0 and V7) and 6 other vectors are denoted by Vi(where i varies from 0 to 7

0(000), 1(100), 2(110), 3(010), 4(011), 5(001), 6(101), 7(111). The binary numbers 1 suggests superior switch being on and 0 alludes to the bottom switches being on. It tends to applied to preferred output voltage to obtain the preferred reference voltage Vref in vector form in the d-q plane

The intention of SVPWM procedure is to estimate the reference voltage Vref in vector form is utilizing the 8 switching patterns. One basic strategy for estimate is to create the inverter in a small period, T to be the identical as that of Vref in the same period.

SVPWM can be actualized by the accompanying advances:

- Rule 1. Resolve Vd. Vq, Vref and α
- Rule 2. Resolve time duration T1, T2, T0
- Rule 3. Resolve switching time for switches (S1 to S6)

S 1 to S 6 represents segments from 1 to 6

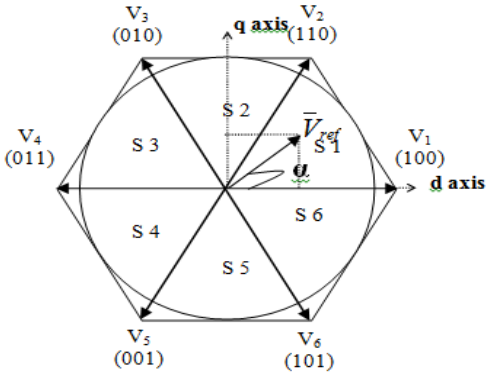


Fig.3 switching vectors and segments

B. SVPWM based DC bus:

The foremost merit of the SVPWM over Sinusoidal Pulse Width Modulation is that it improves utilization of DC bus near 15%. It is illuminating to found the pole voltage of a phase, for instance, to appreciate this reality.

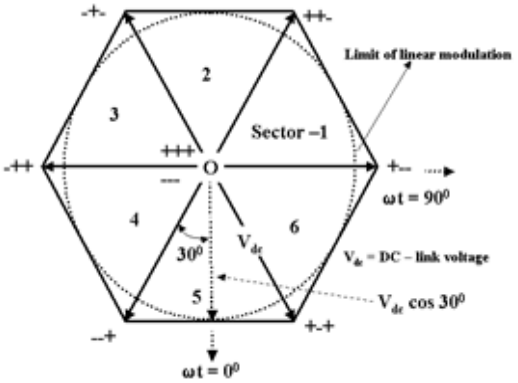


Fig.4 Resolve the sample-averaged pole voltage

$$T_1 = \frac{|\mathbf{v_{sr}}|\, T_s \sin(\pi/3 - \alpha)}{V_{dc} \sin(\pi/3)} \quad (4a)$$

$$T_2 = \frac{|\mathbf{v_{sr}}|\, T_s \sin\alpha}{V_{dc} \sin(\pi/3)} \quad (4b)$$

In equation.4, represents the of the reference vector amplitude and ‘ ’ denotes position with respect to the starting of the segment in which reference vector tip is situated. As varies from and the equations being.

Fig.5 exhibits average voltage VA0, phase voltage VAN and line voltage VAB. VA0 consists of a fundamental component as well as triple order components of fundamental.

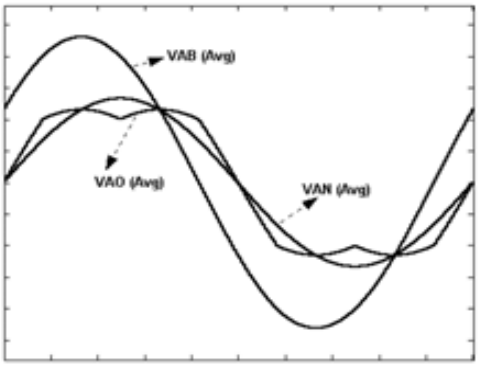


Fig 5 voltage waveforms of VA0, VAN and VAB

The triple component of voltages cancel out each other and the resultant a sinusoidal averaged line voltage is being produced. The radius of the biggest circle corresponds to the peak value of the reference space vector voltage that can be extolled in the hexagon as exhibited in phase-A voltage is given by:

$$V_{ph,peak} = (2/3) * |V_{sr}| \quad (6)$$

$$V_{ph,peak,\max} = \frac{2}{3} * \frac{\sqrt{3}}{2} * V_{dc} = \frac{V_{dc}}{\sqrt{3}} = 0.577 * V_{dc} \quad (7)$$

From a three Phase inverter phase maximum voltage can be obtained with SPWM method is equal to Where as with SVPWM is which is about 15.4% more than SPWM. Hence SVPWM achieves good usage of DC bus.

III CONTROL METHODOLOGY

A. Block Diagram Of Control System

A forced-commutated VSI with DC capacitor is an active power filter as exhibits in Fig.6. The voltage distortion in supply system is normally very low. The supply voltage is assumed to be ideal. Which is sinusoidal and from Clark's transformation 3Ø balanced voltages [vsa vsb vsc] in a-b-c can be represented in 2-phase illustration i.e., d-q theory, these voltage vectors have constant amplitude with angular speed of

$$\overline{V}_s = \frac{2}{3}\left(v_{sa}a^0 + v_{sb}a^1 + v_{sc}a^2\right) = V_{sd} + jV_{sq} = V_s\angle\theta^s \quad (8)$$

where $a = e^{j\frac{2}{3}\pi}$

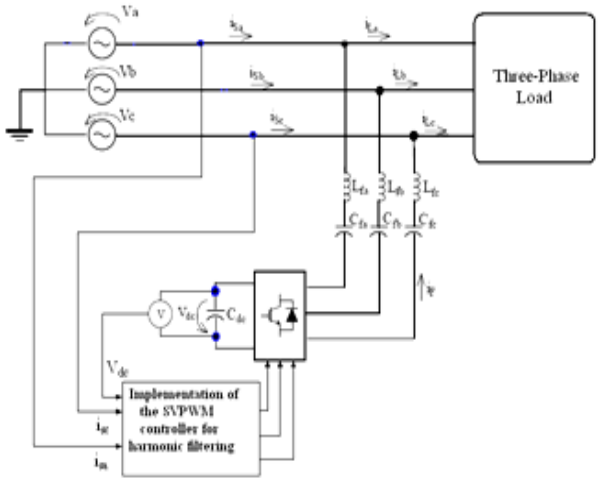


Fig.6 APF using SVPWM

From Fig.6, to maintain the constant DC bus voltage Vdc capacitor is used and it stores energy on the DC side, three-phase VSI as a main circuit for shunt APF. Phase A equivalent circuit is as exhibited in Fig.7 for the above described Fig.6.

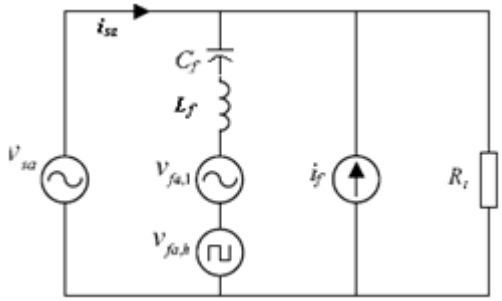


Fig.7 per phase Equivalent circuit of phase A

B. Compensation Principle

In the Fig.6, vfa,1 represents output voltage where as vfa,h represents harmonic voltages of the inverter. in parallel from a inductor Lf and capacitor Cf these voltages are associated to source supply (vsa). The harmonic currents emitted from the load automatically by the injection of suitable voltages from the APF in which the supply current isa is forced and harmonics are compensated.

From Fig.6, the steady state relationship between the AC supply voltage and the APF.

Supply voltage is given by $\overline{V}_s$

Fundamental current of APF is given by $\overline{I}_{f1}$

Fundamental voltage of APF is given by $\overline{V}_{f1}$ and these variables are represented in the form of space vector.

$$\overline{V}_s = L_f \cdot \frac{d\overline{I}_{f1}}{dt} + \frac{1}{C_f}\int \overline{I}_{f1}dt + \overline{V}_{f1} \quad (9)$$

The inductor Lf and capacitor Cf are joined to APF. The purpose of these inductor and capacitor is to filter higher harmonics in the current and connects the AC supply to the network. As the reactance is small the voltage across the inductor voltage and capacitor voltage is very small as for the 50Hz frequency as compared with the main voltage. So the voltage across these elements will be neglected. Then the balanced voltage can be written as

$$\overline{V}_s = \overline{V}_{f1} \quad (10)$$

When the supply current and voltages are in phase and in sinusoidal in the presence of nonlinear load, the APF generates to a pure resistance load as Rs, and corresponding equation being

$$\overline{V}_s = R_s \cdot I_s \quad (11)$$

where .

$$\overline{I}_s = \frac{2}{3}\left(i_{sa}a^0 + i_{sb}a^1 + i_{sc}a^2\right) = I_{sd} + jI_{sq} = I_s\angle\theta_i$$

Then the relationship between supply current Is and the supply voltage amplitude Vs is

$$V_s = R_s I_s \quad (12)$$

From equations (10),(11) and (12) and equation (10) becomes

$$\overline{V}_{f1} = \frac{V_s}{I_s} \cdot \overline{I}_s \quad (13)$$

Equation (13) portrays the connection between the supply voltage, APF output voltage and the supply current, when the APF work typically. Be that as it may, for assembly the APF consistently accomplishing the necessary impact, the voltage at DC bus Vdc must be adequately large and stable. In the event that power imbalance, for instance, transient produced by load change, the difference between the supply power and the load power can be from the DC capacitor, the DC capacitor normal voltage is reduced. Right now, to raise the delivered real power by the supply the magnitude of the supply current must be enlarged. Despite that when the capacitor voltage increases supply current has to be reduced. Therefore, the active power flow can be reflecting by the DC capacitor voltage. So as to keep the stable DC bus voltage, the setting voltage is compare with detected DC bus voltage. The stood out results is continued from a PI controller and from the PI controller supply current Is can be acquired.

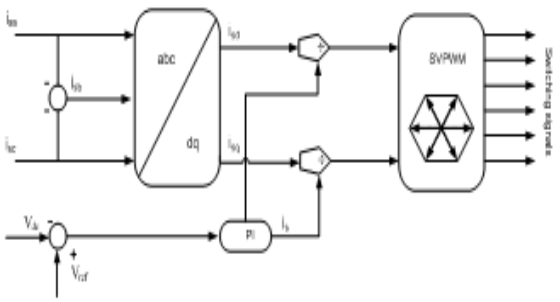


Fig.7 proposed algorithm

The Fig.7 exhibits the proposed algorithm of active filter controller with hybrid active filter system which executed for reducing the harmonics. The supply currents isa ,isc are sampled by the controller in each cycle, and the supply current isc is resolved with the equation of -(isa+isc), as the addition of these currents is zero. The transformed DC quantities (d-q) axis from the above 3Ø supply currents generated from synchronous reference frame, the PI controller generated supply current, Vdc and Vref generates voltage signal. By utilizing Fourier analysis used in the block, magnitude of voltage and phase angle is determined and these are fed to the proposed code to resolve the time duration T0,T1 and T2 which are on-time of V0, V1, and V2.

IV SIMULATION RESULTS

Firstly, the three-phase supply currents are detected and changed into d-q axis. The principal component of the supply current is changed into d-q axis and the supply current magnitude Is created by the PI controller. The obtained d-q axis components produce voltage signal command. With the utilization of Fourier magnitude block, voltage magnitude and phase angle is determined from the obtained signal. These qualities are fed to the created code and produced switching actions are connected to the APF. In this way, power balancing of the filter takes place. Further, presentation with various loads is presented.

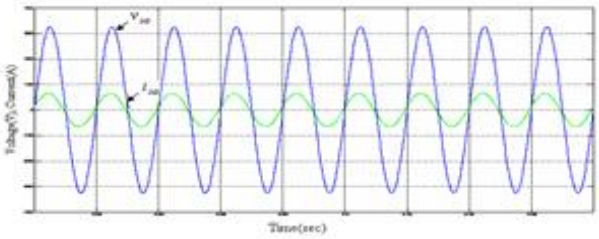
The total simulation representation of APF with various loads is exhibits in Fig. 8, 9 and 10. For an input rating is of 230V with 5kHz frequency, the simulation outcome previous and later power balancing are exhibited.

System parameters	Values of parameters
Supply system	230 V (rms), 50 Hz, three-phase supply
Linear balanced load	$Z_l = 75 + j\,62.83\ \Omega$
Linear unbalanced load	$Z_{la} = 75 + j\,31.42\ \Omega$, $Z_{lb} = 100 + j\,23.56\ \Omega$, $Z_{lc} = 85 + j\,31.42\ \Omega$
Non-linear load with resistance	R=1000 Ω
APF	C_{dc}=1000µf, Vref = 750V, C_f = 24µf, L_f = 30 mH

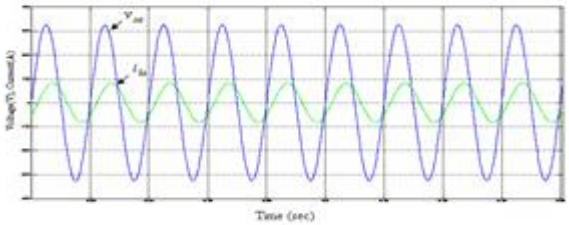
Table 1 parameter values

A. Linear balanced load

load current and Source current are reduced by factor 25 for evaluation reason



(a)

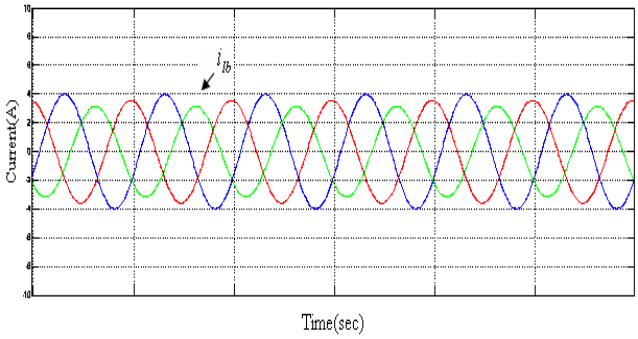


(b)

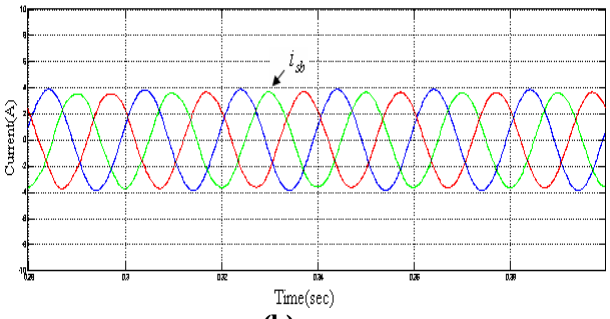
Fig.8 Linear balanced load
(a) phase-A supply voltage and load current
(b) phase-A supply voltage and supply current

The Fig.8 exhibits the APF when load is 3Ø balanced RL load. Fig.8 (a) and Fig.8 (b) is the waveforms of the phase-A supply voltage and the load current before and compensation respectively

B. Linear unbalanced load



(a)

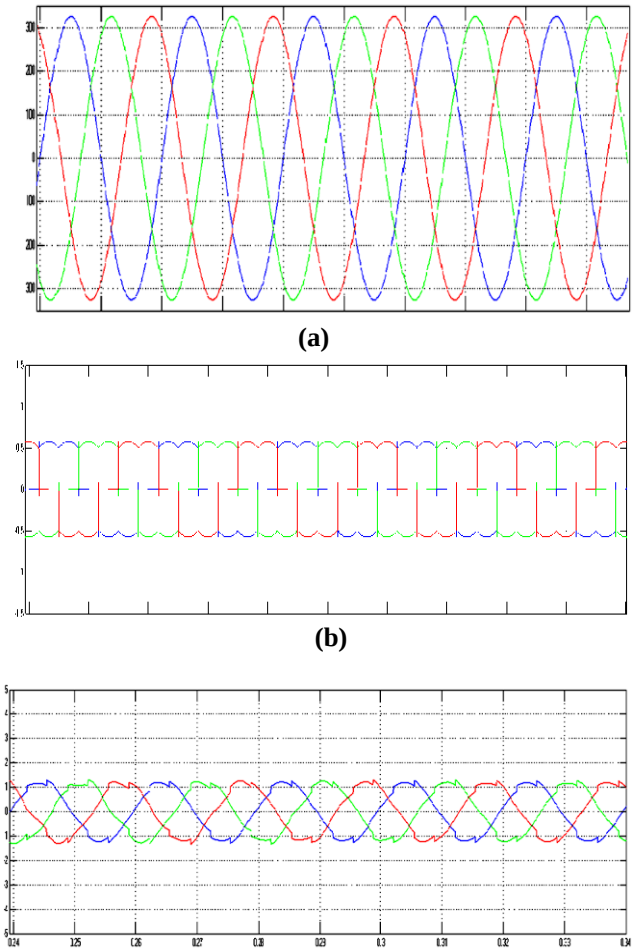


(b)

Fig.9 linear unbalanced load
(a) 3Ø load current (b) 3Ø supply current

The Fig.9 exhibits the APF with 3Ø unbalanced RL load. Fig.9 (a) and Fig.9 (b) is the waveforms of the 3Ø load current before compensation and after compensation respectively. From the figures, it very well may be seen that APF controller can cure the system unbalance.

C. Non-linear load with resistance



(a)

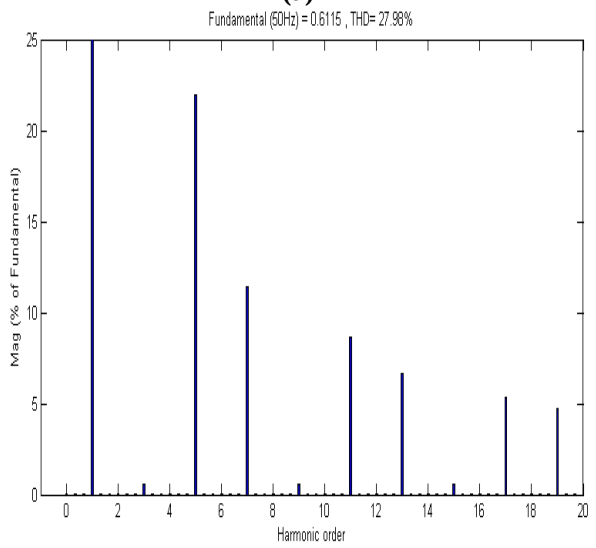
(b)

(c)

Fig.10 Simulation results of non-linear load 3Ø source voltage (b) 3Ø load current (c) 3Ø source current

The Fig.10 exhibits the APF with non-linear load i.e., A 3Ø diode bridge rectifier with R load. Fig.10 (a) source phase voltage where as Fig.10 (b) and Fig.10 (c) load current before and after compensation respectively.

(a)



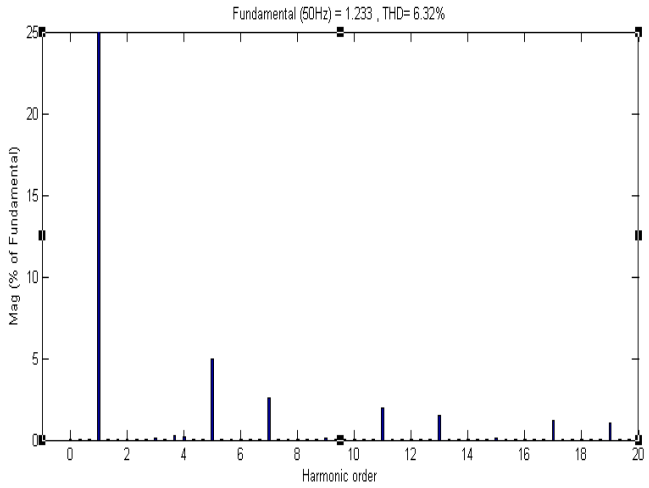


Fig 11 Harmonic spectrum of non-linear load
(a)The phase-A load current harmonic spectrum
(b)The phase-A source current harmonic spectrum

The Fig.11 demonstrates the reproduction of harmonic range of APF as soon as the non--linear 3Ø diode bridge rectifier with R load is connected. Fig.11 (a) and Fig.11 (b) is the load side harmonic range of the current before and later stages of compensation respectively. There is difference in waveforms in source current previous and later stages of compensation. The dominant harmonics in load current are fifth, seventh, eleventh and thirteenth order where as these harmonics reduced in after compensation. The THD of current at load is 27.98% where as supply current 6.32%. It should be noticed that by using passive filter higher order harmonics are reduced where change in current with respect to time is high because of fixed frequency.

V. CONCLUSION

From the above results the performance APF with SVPWM for different loads is viewed. The load voltage and current are in phase if there should be linear balanced or unbalanced load, the amplitude of 3Ø source currents are made equal. In both the cases simulation results is obtained. The THD in source current is reduced when associated to non-linear load when simulated. These currents from the nonlinear load are drawn by the hybrid filter and maintain grid voltage sinusoidal. Even though load is unbalanced, linear or nonlinear i.e., load current is non-sinusoidal but supply current remains sinusoidal.

In this paper, SVPWM based control method for the APF is presented. This strategy requires couple of sensors, easy in algorithm and ready to compensate unbalanced load disturbances. The algorithm will most likely diminish the difficulty of the control circuitry. The harmonic spectrum under non-linear load conditions exhibits better result. The SVPWM uses two level inverter for more efficiency, usage of DC bus voltage and to generate minimum harmonic distortion in 3Ø VSI. For power quality improvement SVPWM control technique is connected in series with APF. The performance of Active Power Filter with SVPWM is done in MATLAB/Simulink

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