Hardware Implementation of an Enhanced Seven Level H Bridge Inverter with Reduced Switch Configuration

M.Suneel Kumar, V.Ramudu

Abstract*:- *There are various boundaries in extracting power through Renewable energy sources. To reduce the insufficiency and high power demand we need to look up power extracting Techniques. To take out power through divergent sustainable power source assets for example solar energy, Photo Voltaic cell, Wind energy, Multilevel inverter is used .It orchestrates the preferred ac production from a number of dc input sources. The primary focal point of the paper is develop the productivity of level inverter and get better the nature of yield voltage by way of diminish number of power electronic switches. Here MOSFETs are used as switches. In this Paper, Simulation along with hardware design of 7-level cascaded Multi-level inverter and reduced switch multilevel inverter are presented.

I. INTRODUCTION

To converts the low level dc voltages into required AC voltage multilevel inverters are used . So as to deliver the AC output from DC output mainly a two-level inverter is preferred. To integrate a required single phase or three-phase voltage Multilevel converters are mainly utilized. The needed multi-staircase yield voltage is acquired by joining a number of dc voltage sources for case in point Solar panels, fuel cell , ultra-capacitors and batteries are majority familiar self-governing sources utilized . The utilization of power devises at elevated power typically insist switching frequency decline , so as to guarantee that misfortunes brought about by the deficient scenery of realistic switching strategy does not altogether diminish inverter effectiveness. at present, numerous application for multilevel inverters, such as electrical drives ,FACTS equipment and HVDC lines. Mainly three customary structures for multilevel inverters are there, they are : diode-clamped, flying capacitor, and cascaded multilevel inverter with split dc sources.

II. CASCADE HB MULTILEVEL INVERTER

The normal 2 level or 3 levels inverter does not considerably get rid of the avoidable harmonics within the inverter output . hence, as a replacement for of traditional Pulse width modulation inverters multilevel inverter are used . In this procedure, at the converter terminals, the phase voltage levels are 2L+1, Hear L is the voltages across the DC source . at these, a detach dc link capacitor are used across for the voltage source and among the capacitor potential may vary. So, single dc voltage source needs for every power circuit depends upon the amount of phase voltage. The quantity of dc link capacitors will vary. Each cell of H-Bridge for multilevel inverter can have positive, negative or zero voltage. The total of all voltages of H-connect cell and as for neutral point is the output voltage it is symmetric, so the voltage levels are odd in numeral. Cascaded HB multilevel inverters have IGBT is act as switch. Those switches consists lower block voltage and switching frequency is high . each single H-bridge converter is connected with a single DC source & AC voltages of various levels at converter ends are joined in series and produce dissimilar output voltages they are Positive Vdc, Negative Vdc and zero Vdc. The summing up of converter outputs is the output ac voltage wave form. Cascaded HB multilevel inverter is a curious and attractive topology, for example, configuration , required less segments and so on. The principle benefit is it make output voltages with little bending and little voltage stresses (dv/dt). This will work with a lower switching frequency. Many H-bridge Inverter units are integrated in Cascaded Multilevel Inverter . each H bridge be nourished from an alternating DC supply this will be given from batteries, power modules, or solar panels .The working of the inverter is accomplish a favored voltage through diverse Dc Sources .The terminals of multilevel inverters be associated into series arrangement. like the flying-capacitors inverter or diode-clamp. This type inverter no need of capacitors for voltage-balancing or voltage-clamping diodes; hence this inverter has more benefits. by four unique mixes of switches, Switch1, 2, 3, and 4 of inverter will deliver output voltage in the dimensions of +Vdc, 0, and – Vdc .In request to get +Vdc, switches 1 and 4 shoul be ON while to acquiring – Vdc, we have to switch on ON switches 2 and 3. by turning ON, of Switch 1 and 2 or 3 and 4, the voltage output is zero. Output of every one of each full Hbridge Multi level inverter is associated with sequence arrangement with the goal that the voltage output wave produced will be the summing up of the inverter voltage outputs .

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III. CASCADE H-BRIDGE SEVEN LEVEL INVERTER DESIGN

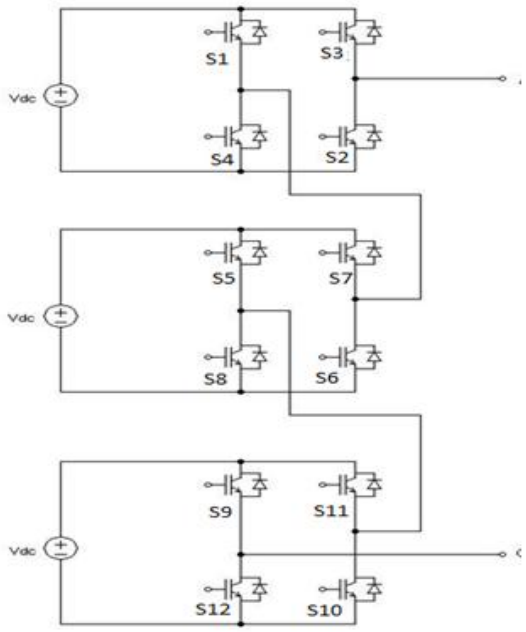

Figure.1. H-bridge Cascaded 7-level Inverter

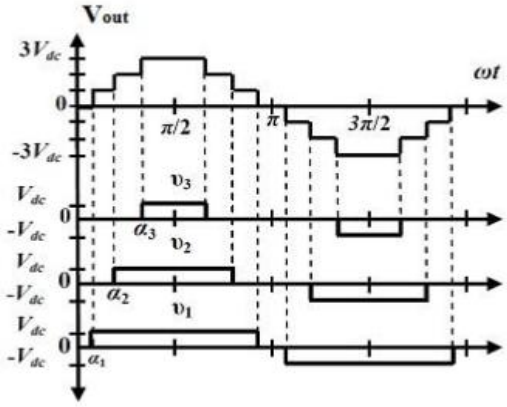

Figure.2. Voltage output Waveform of Cascaded HB 7-level Inverter

Single stage 7-level Cascade HB ML Inverter has created 7 stage of output as augmentation with its input supply (Vdc), those are , positive three Vdc, positive two Vdc, positive Vdc, zero, nagativeVdc, negative two Vdc and negative three Vdc. The subsequent AC ouput voltage swing from positive three Vdc to negative three Vdc through zero level. Task of ML inverter is resolved dependent upon the state of the switch-close and switch-open condition for every power electronic switch. output estimation for the inverter will relies upon pattern that of switching pose . In the seven - level CHB-MLI there are seven potential outcomes design of switching arrangement. The output voltage for every arrangement which can to be clarified as pursue:

Stage-1: In this stage the SW-one, SW-two, SW-five, SW-six, SW-nine and SW-ten are switched on, consequently the voltage at the output terminals is three times of Vdc.

Stage-2: In this stage the SW-one, SW-two, SW-five, SW-six, SW-ten and SW-twelve are switched on, consequently the voltage at the output is two times of Vdc.

Stage-3: In this stage the SW-one, SW-two ,SW-six, SW-eight, SW-ten and SW-twelve are switched on, consequently the voltage at the output terminal is Vdc.

Stage-4: In this stage the SW-two SW-four, SW-six, SW-eight, SW-ten and SW-twelve are switched on , consequently the voltage at the output terminal is 0 volt.

Stage-5: In this stage the SW-two ,SW-four, SW-six, SW-eight, SW-nine and SW-ten are switched on, consequently the voltage at the output terminal is nagativeVdc.

Stage-6: In these task when SW-two, SW-four, SW-seven, SW-eight, SW-eleven and SW-twelve are on, consequently the voltage at the output terminal is two time of negative Vdc

Stage-7: In these task when SW-three, SW-four, SW-seven, SW-eight, SW-eleven and SW-twelve are on, consequently the voltage at the output terminal is three time of negative Vdc .

The multilevel cascade HB inverter output voltage of is whole output of all extensions associated in sequence arrangement. 7-level cascaded HB inverter comprises with three bridges which are associated at sequence arrangement. The output level in Cascaded HB-MLI is given as N=2L+1 where L is isolated DC supply and N is inverter output level. The primary task of the inverter is to integrate preferred voltage commencing forn independent DC supply. Cascade HB-ML Inverter is series with parallel association of power electronic switches. An isolated figure of supplies are necessary by Cascaded HB-ML Inverter, every one of these connected to a H-bridge source cell. Three full H-bridge are there in the inverter, at that point it essential three DC power sources for every cascade H-bridge. Aurdino uno is utilized as controller to organize gate pulses of cascaded HB multilevel inverter.

IV. 7 LEVEL REDUCED SWITCH MULTILEVEL INVERTER

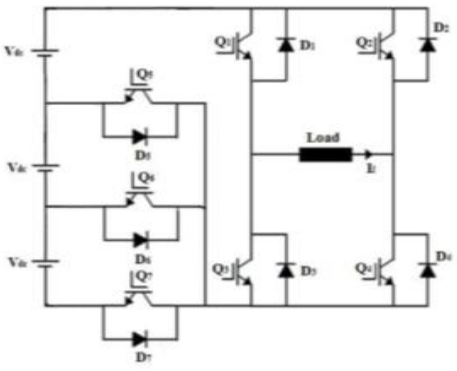

Figure 3. Seven Level reduce switched Multilevel Inverter

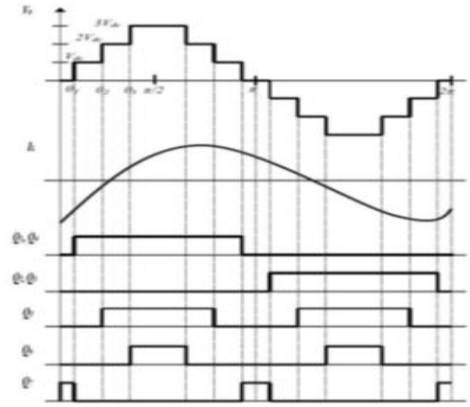

Figure.4. voltage Waveform across the output terminals of Seven Level reduced switch Multilevel Inverter

So as to expel the disadvantages, we propose another representation:

- Many power switches are utilized for the above representation so that power misfortune on the switches should be exceptionally more because of this the utilize and magnitude for the harmonics filter increments.
- there is high stress on power electronic equipment if the voltage level is high,.
- due to the power misfortunes in different converters there would be low productivity.

To dispose of the above issues, a measured power electronic innovation called multilevel inverter, this is suggestible to coordinating sustainable power sources. Primary aim is show signs of improvement the nature of multilevel inverter output voltage with diminished numeral of switches. Mainly noteworthy matter in multilevel inverter configuration is , it creates almost productivity voltage waveform in sinusoidal and to evacuate harmonics in lesser order. A key subject for the lower order harmonics to discover switching angles in order to create the output voltage among fundamental frequency.

Table1. Seven Level reduced switechedmulti level Inverter Switching Sequence

S1	S2	S3	S4	S5	S6	S7	O/P voltage level
1	0	1	0	0	0	1	+Vdc
1	0	0	1	0	0	1	+2Vdc
1	0	0	0	1	0	1	+3Vdc
0	0	0	0	0	0	0	0
0	1	1	0	0	1	0	-Vdc
0	1	0	1	0	1	0	-2Vdc
0	1	0	0	1	1	0	-3Vdc

Mode Of Operation

Seven Level reduced switched Multilevel Inverter has seven mode of operation and

they are as follows

1. Mode 0(0Vdc)
2. Mode 1(1Vdc)
3. Mode 2(2Vdc)
4. Mode 3(3Vdc)
5. Mode 4(-1Vdc)
6. Mode 5(-2Vdc)
7. Mode 6(-3Vdc)

Each mode is explained with the help of circuit diagram and are follows

Mode 0

In this mode the entire switch is turned off as shown in figure given below. The output voltage is zero hence the name 0Vdc

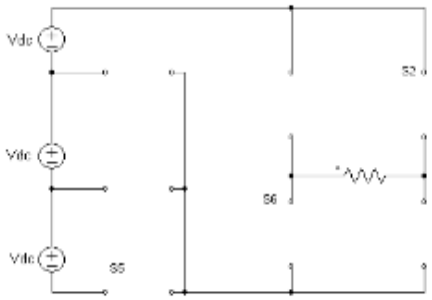

Fig 5. mode 0(0Vdc)

Mode 1

In this mode we get an output voltage +Vdc .The switches which are conducting in mode 1 process are as follows: S1-S3- S7. The switches which non-conducting are: S2-S4-S5-S6. Now only three switches operate at a time to give the desired output waveform. The current flow path is as follows S1-R load-S7-S3-+Vdc.

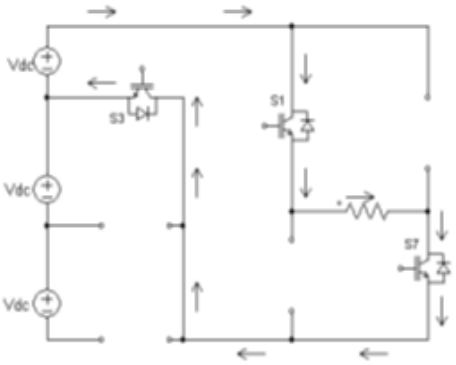

Fig 6. Mode 1(+Vdc)

Mode 2

In this mode we get an output voltage +2Vdc, i.e the second step in the output waveform. The switches which are conducting in the mode 2 of process are S1-S4-S7. The switches which are non-conducting are: S2-S3-S5-S6. The current flow path is as follows S1-R load-S7-S4-+Vdc-+Vdc.

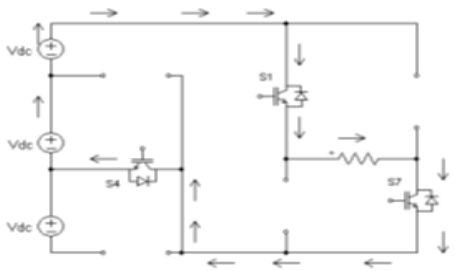

Fig 7. Mode 2(+2Vdc)

Mode 3

In this mode we get the output voltage as +3Vdc, i.e third step of the output voltage. The switches which conducting in this mode of operation are S1- S7-S5. The current flow path is as follows S1-R load-S7-S5-+Vdc-+Vdc-+Vdc.

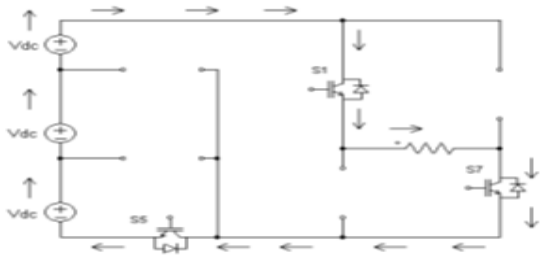

Fig 8Mode 3(+3Vdc)

Mode 4

In this mode we get an output voltage . The switches which are conducting in the mode 4 of process are as follows: S2 -S3 -S6. The switches which are non-conducting are: S1-S4 S5-S7. The current flow path is as follows S2-R load-S6-S3--Vdc.

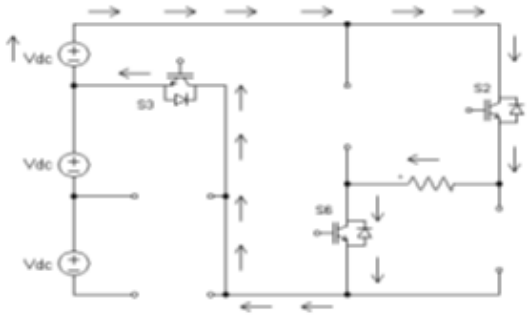

Fig 9 Mode 4(-Vdc)

Mode 5

The switches which are conducting in the mode5 process are as follows: S2-S3- S6. The switches which are non-conducting are: S1-S4-S5-S7. The current flow path is as follows S2-R load-S6-S4—Vdc--Vdc.

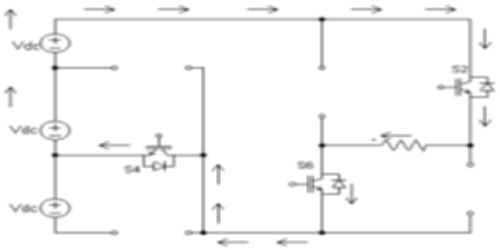

Fig 10mode 5(-2Vdc)

Mode 6

In this mode we get an output voltage -Vdc. The switches which conducting in the mode 6 process are as follows: S2-S3-S6. The switches which are non-conducting are: S1-S3-S4-S7. The current flow path is as follows S2-R load-S6-S5—Vdc—Vdc--Vdc.

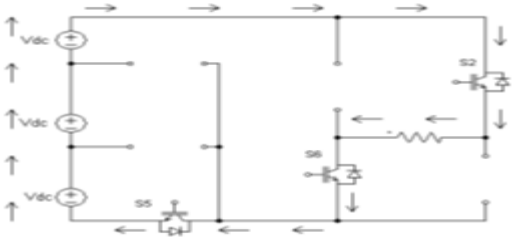

Fig 11. mode 6(-3Vdc)

Output Waveform

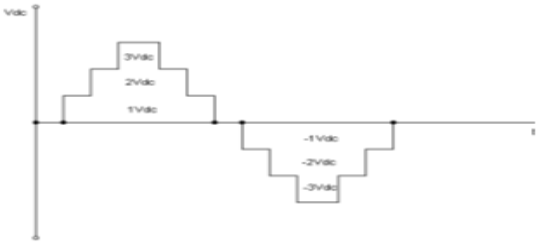

Fig 12 Output voltage Waveform fo the reduced switched topology

Figure 12 represents the expected output terminal voltage waveform which can be obtained by conducting this project.

Advantages

1. Soft switching procedures can be utilized to lessen exchanging misfortunes and stresses.
2. compared to diode clipped and flying capacitors , it necessitate the less numeral of parts to accomplish a similar numeral of voltage stage.
3. Capability of electrical shock is decreased because of independent DC sources.
4. switching redundancy for inward voltage level is conceivable in light of the fact that the voltage at output terminal is total of every bridge across output.
5. The arrangement structure permits a versatile circuit design and bundling because every bridge have a similar arrangement.

V.HARDWARE USED

The single phase seven level cascade multilevel inverter comprises of 12 mosfets , 12 mosfet driver IC and 3 DC sources. The gating signals of mosfets are provided by a Ardinouno controller. The 1-phase 7-level reduced switches inverter comprises of 7 mosfets , 7 mosfet driver IC and 3 DC source. The gating signals of mosfets are provided by a Ardinouno controller.

Mosfet

MOSFETS has four terminals i.e. source (S), gate (G), drain (D), and body (B). Regularly the body terminal of the mosfets is associated with source terminus assembly it a 3 terminal device. It is a type of field effect transistor that entirety by changing the width of conduit along which holes or electrons stream. The charge carriers start at source and end by drain. It is a voltage controlled device as width of the conduit is constrained by voltage at gate. There are two modes in which a mosfets can work, depletion mode and enhancement mode. Power mosfets has high switching speed making it well suited for

power electronics applications. The mosfets used in this project is IRF510 that is of N –Channel type

Optocoupler :

An Optocoupler, is an electronic segments that interlink 2 distinct electrical circuits by methods for a light delicate optical interface.it is utilized To give electrical segregation among an info source and a output load.

Isolation is the electrical or magnetic division between two circuits and frequently used to isolate two unmistakable areas of a power supply.Isolation gives a hindrance crosswise over which risky voltages can't go in case of a flaw or part failure.it avert the exchange of large or unsafe voltages among circuits for security cause and assurance against electric shock. It impede large common mode voltage exhibit in our signals that can forestall its estimation and harm hardware.. Optocoupler, otherwise called an Opto-isolator, embrace of a LED that generates infra-red light and a semiconductor photograph touchy gizmo that is used to recognize the transmitted infra-red shaft. Flow from the yield signal passes around the input LED and that discharges an infra-red light whose power is comparative toward the electrical signal. This transmitted light dip over the base of the photo-transistor, it makes switch-ON and direct likewise to a typical bipolar transistor. At the point when the existing coursing around the LED is encroach on; affecting infra-red transmitted light is cut-off, causing the photo-transistor to quit leading. The photo-transistor can be used to exchange current in the given circuit. As long as there is refusal adjacent electrical alliance among the advice and given optocoupler, electrical disconnection up to 10kV is achieved.theoptocoupler utilized in this task is MCT2E901Q ,6pin

Microcontroller- Arduino Uno

The Arduino Uno contains 14 digital in/out pins, it has 6 input analog pins, USB connection, it requires dc supply for that adapter or battery can be used ,. in the In this project, Arduino Uno has been used to provide the switching pulses to mosfets

SOFTWARE Matlab - R2013 , the Simulink tool in Matlab to obtain simulation of the inverter. the desired output, which could be observed in the scope on Matlab , and those output are provided below.

VI. SIMULATION AND HARDWARE CIRCUITS & RESULTS

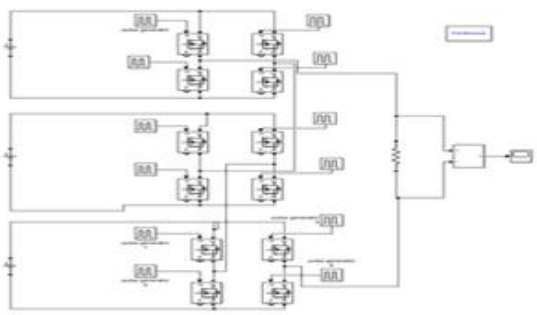

Fig 13.Simulation circuit of Conventional seven level Cascaded HB Multilevel Inverter

The above fig shows simulation circuit of the Conventional seven level Cascaded HB Multilevel Inverter. pulse generator block is used to provide giving gate pulses for MOSFETs.

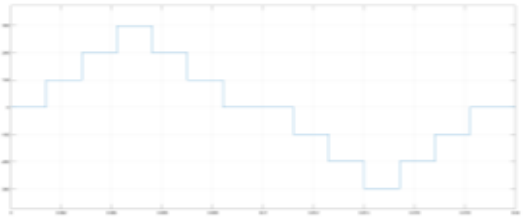

Fig 14.simulation output voltage waveform of Conventional 7 level Cascaded HB Multilevel Inverter

Above fig shows simulation output voltage waveform of Conventional seven level Cascaded HB Multilevel Inverter.

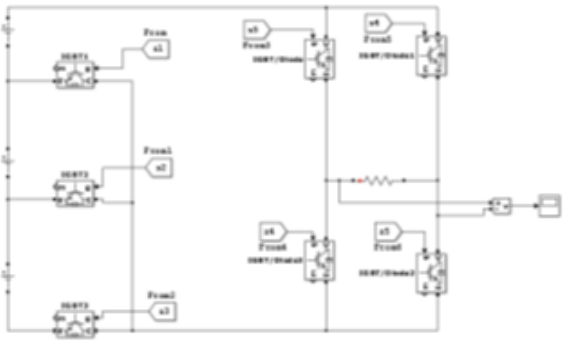

Fig15.Simulation circuit of 7 level reduced switched Multilevel Inverter.

The above fig shows the Simulation circuit of 7 level reduced switched Multilevel Inverter. For this only 7 switches used for 7 level output. Output is taken across the resistive load

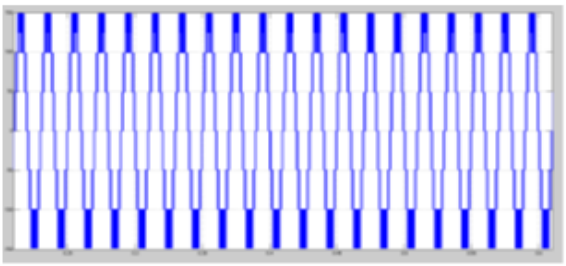

Fig16.Inverter Output voltage of 7 level reduced switched Multilevel Inverter.

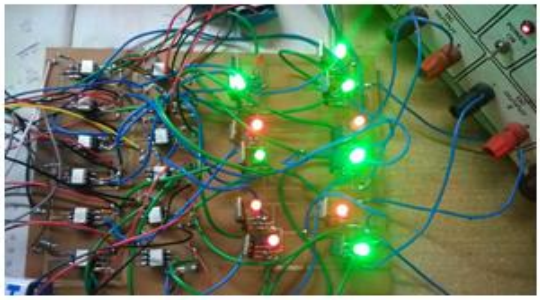

Fig 17.PCB Board of Conventional 7 level Cascaded HB Multilevel Inverter

Fig 18.Hardware setup of Conventional 7 level Cascaded HB Multilevel Inverter

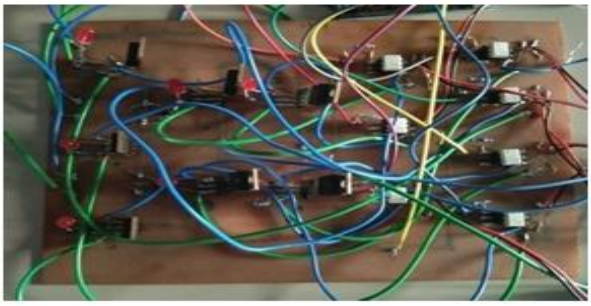

Fig 19.PCB Board for 7 level reduced switched Multilevel Inverter

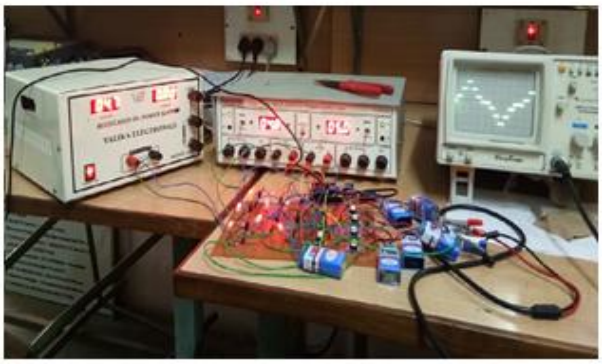

Fig 20.Hardware setup for 7 level reduced switched Multilevel Inverter

VII. CONCLUSION

The conventional cascade HB multilevel inverter utilizing equivalent DC sources and proposed 7 level diminished switches multilevel inverter was validated and created with the hardware . The aurdiniuno is utilized as a controller for giving gate signals to mosfets The firing angels are determined and sustained to the inverter for its activity by utilizing ardino.. In the traditional HB Multilevel inverter for 7 level output 12 switches are required though in altered methodology just 7 changes are essential to accomplish 7 level output. The level of decreased count of switches is clarified along the assistance of the table2 demonstrated as follows.

Table 2: Percentage of switch Reduction

Type of the inverter	No of Switches used
7-level cascade HB Multilevel inverter	12
7-level reduced switched Multilevel inverter	7
% of reduction in switch	41.667

REFERENCES

1. IEEE Recommended Practices and Requirements for Harmonics Control in Electric Power Systems, IEEE Std. 519, 1992.
2. A. Moreno-Munoz, Power Quality: Mitigation Technologies in a Distributed Environment. London, U.K.: Springer-Verlag, 2007.
3. N. G. Hingorani, “Introducing Custom Power,” IEEE Spectrum, Vol.32, n. 6, pp. 41-48, June 1995
4. Ghosh and G. Ledwich, Power quality enhancement using custom power devices, London, Kluwer Academic Publishers, 2002.
5. Naderi and A. Rahmati, "Phase-Shifted Carrier PWM Technique for General Cascaded Inverters," IEEE Trans. Power Electron. vol. 23, pp. 1257-1269, 2008.
6. A Pandey, B Singh, B N Singh, A Chandra, K Al-Haddad, D P Kothari, “A Review of Multilevel Power Converters”, IE (I) Journal.EL, vol. 86, pp.220231, March, 2006.
7. K.A Corzine, and Y.L Familiant, “A New Cascaded Multi-level H-Bridge Drive,” IEEE Trans. Power. Electron., vol.17, no.1, pp.125-131. Jan 2002.
8. J.S.Lai, and F.Z.Peng “Multilevel converters – A new breed of converters”, IEEE Trans. Ind.Appli., vol.32, no.3, pp.509-517. May/ Jun. 1996.
9. N. A. Rahim, and J. Selvaraj, ―Multistring five-level inverter with novel PWM control scheme for PV application,‖ IEEE Trans. Ind. Electron., vol. 57, no. 6, pp. 2111-2123, June 2010.
10. P.Bhagwat, and V.R.Stefanovic, “Generalized structure of a multilevel PWM Inverter,” IEEE Trans. Ind. Appln, Vol.1A-19, no.6, pp.1057-1069, Nov. /Dec...1983.
11. J.Rodriguez, Jih-sheng Lai, and F Zhengpeng, “Multilevel Inverters; A Survey of Topologies Controls, and Applications,” IEEE Trans. Ind. Electron., vol.49,no4. pp.724- 738. Aug.2002.
12. RoozbehNaderi, and Abdolrezarahmati, “Phase-shifted carrier PWM technique for general cascaded inverters,” IEEE Trans. Power. Electron. vol.23, no.3, pp.1257-1269. May. 2008.
13. Bhim Singh, Kamal AlHaddad&Ambrish Chandra, 1999, A Review of Active Filter for Power Quality Improvements, IEEE Trans on Industrial Electronics, 46(5), pp.960970