

Bat Algorithm Based Selective Harmonic Elimination PWM for an Eleven Level Inverter

S.Srinivasan, S.Muthubalaji, G.Devadasu, R.Anand

Abstract -Multilevel inverters are the vital drives in industry and new energy power schemes. Selective Harmonic Elimination (SHE) based inverters are the best choice for attaining the preferred fundamental component as well as for harmonic free electrical applications. Since the SHE-PWM methodology has non-linear and transcendental equations, finding the appropriate switching angles for this are so difficult. In this paper, Bat Algorithm (BA) is proposed to solve the switching angles for an eleven level inverter with dissimilar dc sources. This proposed algorithm is validated with thorough simulation for finding its viability and efficiency. The attained results prove that Bat algorithm is very effective than Genetic algorithm (GA) and Flower Pollination Algorithm (FPA) in removing the selective harmonics and in turn that leads to the minimization of Total Harmonic Distortion (THD) in the voltage output.

Keywords: Cascaded H Bridge Inverter (CHBI), Selective Harmonic Elimination (SHE), Bat Algorithm (BA), Total Harmonic Distortion (THD).

I. INTRODUCTION

Day by day, the Conventional fuels are depleting on one side and the electrical power demand is increasing on the other side. To balance this situation, development of newer power generation units like solar photo voltaic, wind energy generation sources are considered as the alternative for conventional fuels. Multilevel inverters are considered as the best suitable drives for newer energy applications. Conventional three-level inverters can't able to produce harmonic free sinusoidal waveforms and hence it is so difficult for them to fulfill the high quality power needs of a variety of engineering applications. The main advantages of multi-level inverters are near sinusoidal staircase output voltage, high electromagnetic compatibility, lower dv/dt stress, low harmonic distortion, lower switching losses, lower switching frequency stress, higher voltage capability, higher efficiency, etc. Multilevel inverter topologies are basically categorized as flying capacitors, diode-clamped inverters and cascaded H-bridge Inverter (CHBI) [1-4]. Each and every topology has their own merits and demerits and is appropriate for a variety of applications. Out of these aforementioned topologies, cascaded H-bridge inverter grasps its own attention because of its modularity and simplicity of its control strategy. In cascaded H-bridge inverters, $(2s+1)$

number of output voltage levels can be generated by means of connecting 's' number of single phase H-bridge inverters in cascade.

Eliminating the harmonic component and meeting the minimal THD in the voltage output of multilevel inverters are the foremost issues to be considered [4-5]. The performance of the multilevel inverter is decided by the proper selection of the particular Pulse Width Modulation (PWM) technique. These PWM methods can be generally classified as sinusoidal PWM, Space Vector PWM and Selective Harmonic Elimination PWM (SHE-PWM) [6-7]. To eradicate lower order harmonics by utilizing the method of adding various switching angles in a non-sinusoidal voltage wave was initiated around 1960s. Selective harmonic elimination methodology is considered as the most excellent methodology, which chooses appropriate switching angles to eradicate the harmonics in the lower order as well as lowering the THD of voltage output of multilevel inverter. The objective of some of the THD minimization approaches are to denote the switching angles for attaining preferred fundamental component with achievable minimum THD. But in the case of SHE-PWM technique, the multi-levels in the voltage or current waveform of the multi-level inverter is decomposed using Fourier theory to find out the optimum switching angles in order that exact lower order harmonics like 5th, 7th, 11th and 13th can be lowered in the voltage output of the multilevel inverter. SHE technique uses a set of non-linear transcendental equations as the fitness or objective function. There are three methods for solving the SHE problem, resultant theory method, iterative methods like Newton Raphson method and evolutionary algorithms like Genetic Algorithm (GA), Flower Pollination Algorithm (FPA), BFOA, PSO and so on [4], [8-20]. In this paper, to deal with SHE problem and to find out the finest switching angles for minimizing the THD level, Bat Algorithm (BA) technique is proposed [21]. Simulation and experimental results are presented for an eleven level cascaded H-bridge inverter to validate the proposed BA method.

II. MULTILEVEL INVERTERS

2.1 Cascaded eleven-level Inverter Configuration

The simulation diagram of cascaded eleven-level inverter along with dissimilar dc sources is provided in figure 1. A cascaded eleven-level inverter is having five cascaded H-bridges. Every H-bridge is having four numbers of MOSFET switches as shown in the figure 2. Synthesizing

Revised Version Manuscript Received on August 19, 2019.

S.Srinivasan, Associate Professor, EEE Dept., CMR College of Engineering & Technology, Kandlakoya, Hyderabad, Telangana, India. (email id: s.srinivasan2906@gmail.com)

S.Muthubalaji, Professor, EEE Dept., CMR College of Engineering & Technology, Kandlakoya, Hyderabad, Telangana, India.

G.Devadasu, Professor, EEE Dept., CMR College of Engineering & Technology, Kandlakoya, Hyderabad, Telangana, India.

R.Anand, Associate Professor, EEE Dept., CMR College of Engineering & Technology, Kandlakoya, Hyderabad, Telangana, India.

BAT ALGORITHM BASED SELECTIVE HARMONIC ELIMINATION PWM FOR AN ELEVEN LEVEL INVERTER

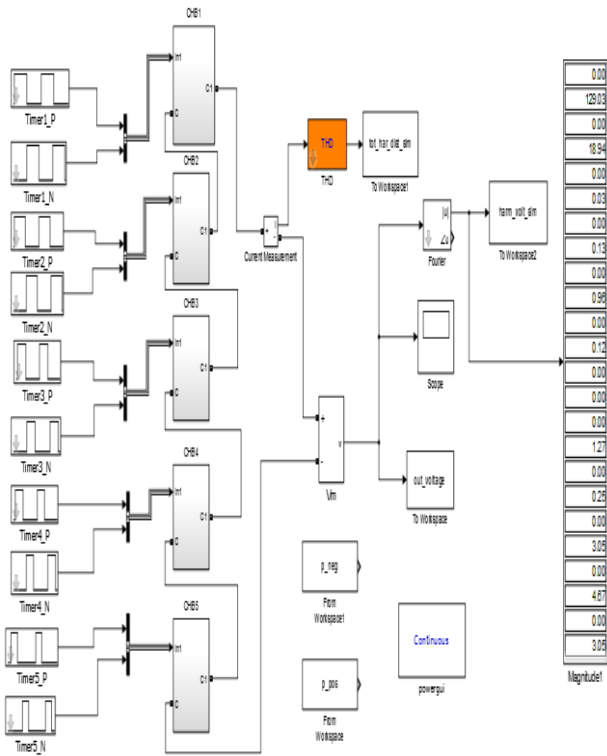


Figure 1. Simulation diagram of an eleven level inverter

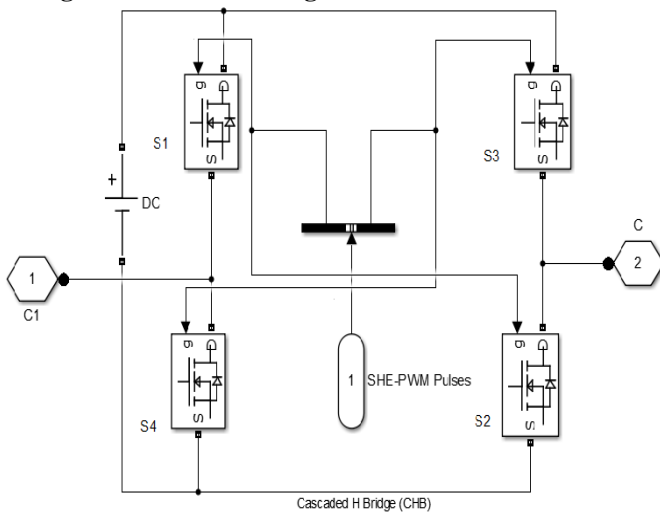


Figure 2. Cascaded H-bridge with MOSFET switches required ac output voltage from various DC voltage sources connected to the individual H-bridge inverter units is the purpose of this multilevel inverter. A cascaded multilevel inverter needs separate DC voltage sources for every cell in every phase unlike the flying-capacitor and diode-clamped topologies and it has its own advantages. A cascaded multi-level inverter is having ‘(2s+1)’ number of levels in its phase-voltage output, where the total quantity of DC voltage sources is represented as ‘s’ [4]. In variable speed drive applications and in ac power supply systems, this CHBI topology becomes very popular nowadays. The voltage balancing capacitors or extra clamping diodes can be avoided by means of this inverter topology.

2.2 Formulation of the Problem

The stair case output voltage of an inverter which is having multiple levels is decomposed via Fourier theory and is given in equation (2.1).

$$V(\omega t) = \sum_{k=1,3,5,\dots}^s \frac{4V_{dc}}{k\pi} (k_1 \cos k\alpha_1) + \dots + k_2 (\cos k\alpha_2) \quad (2.1)$$

The following equation (2.2) gives the limitation on the degree of the triggering angles $\alpha_1 - \alpha_s$:

$$0 \leq \alpha_1 \leq \alpha_2 \leq \dots \leq \alpha_s \leq \frac{\pi}{2} \quad (2.2)$$

The frequency level of the fundamental voltage and its integer multiples is decided by the switching angles $\alpha_1, \alpha_2, \dots, \alpha_s$. This problem is transcendental in nature because here the trigonometric angles are associated with algebraic equations and solving these equations is very tough by means of the conventional methodologies. The switching pulses are optimized by eradicating the selective, lower order harmonics and by maintaining the lowest possible THD for a superior level of the fundamental voltage component. In case of three phase connections, the triplen harmonics will cancel itself. ‘(S-1)’ number of harmonics like 5, 7, 11 and 13 can be minimised from the inverter’s voltage output. The seventh order harmonics in the voltage output of an eleven-level inverter can be eliminated by satisfying the below mentioned expressions (2.3) and (2.4).

$$k_1 \cos(\alpha_1) + k_2 \cos(\alpha_2) + \dots + k_5 \cos(\alpha_5) = \left(\frac{\pi}{2}\right)M \quad (2.3)$$

$$k_1 \cos(7\alpha_1) + k_2 \cos(7\alpha_2) + \dots + k_5 \cos(7\alpha_5) = 0 \quad (2.4)$$

Here, M = Modulation index; V_1 = fundamental component. Modulation Index ‘M’ is defined as $M = V_1 / sV_{dc}$.

The objective function for solving the optimized triggering angle is given in the equation (2.5).

$$f(\alpha_k) = 100 \times \left[\left| M - \frac{V_1}{sV_{dc}} \right| + \left(\frac{|V_5| + |V_7| + \dots + |V_{2s-2}| + |V_{2s-1}|}{sV_{dc}} \right) \right] \quad (2.5)$$

The equations (2.6) and (2.7) give the expression for Total Harmonic Distortion (THD)

$$THD = \left(\frac{V_H}{V_1} \right) \times 100\% \quad (2.6)$$

where

$$V_H = (V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2 + V_7^2 + \dots)^{1/2} \quad (2.7)$$

Solving the equations from (2.1) to (2.4) is so difficult and hence evolutionary based Bat algorithm is proposed in this work.

III. PROPOSED BAT ALGORITHM

Bat Algorithm is a type of algorithm inspired from the nature. Bats are the only mammals with wings and also have superior ability of echolocation. Their size ranges from the tiny bumblebee bat (of about 1.5 to 2g) to the giant bats with wingspan of about 2m and weight up to about 1 kg. Echolocation is used by most of the bats to a certain level. Extensive use of echolocation is done by micro bats than megabats [21]. Micro bats use a type of sonar, named as, echolocation, to identify prey, pass up blockage, and find

their roosting gap even in the dark. These bats produce an extremely loud sound pulse and pay attention for the echo that returns back from the nearby things. Their pulses differ in properties and can be related with their tracking tactics, depending on the genus. Frequency-modulated and short signals are used by most of the bats to sweep through about an octave, whereas constant-frequency signals are frequently used by other bats for echolocation. This echolocation behaviour of the micro bats can be related with the objective function to be optimized to formulate new optimization algorithms.

A few of the echolocation characteristics of micro bats can be idealized for developing a variety of bat-inspired or bat algorithms. The idealized or approximate rules to be followed are:

- a) Echolocation is used by all the bats for sensing the distance and the dissimilarity between background hurdles and prey/food can be known by them through some magical way;
- b) Bats fly randomly at position (xi) with velocity (vi), varying wavelength (λ), fixed frequency (fmin), and loudness (A0) to look for prey. The rate of pulse emission $r \in [0, 1]$ can be automatically adjusted by them by means of adjusting their frequency (or wavelength) of their emitted pulses depending upon the proximity of their target.
- c) Even though the loudness can be different in several ways, it is to be assumed that the loudness differ from a large (positive) A0 to a minimum constant value Amin.

3.1 Pseudo Code

```

f(x), x = (x1,...,xd)T - Objective function
Bat population, Pulse rates rk& loudness Ak Initialization
xk = (k = 1, 2, ...,n) and vk
Pulse frequency defined when fk at xk
While (t < Imax); Imax – Maximum no. of iterations
New solutions creation by fine-tuning frequency,
and revising locations/solutions and velocities
    if (rand > ri)
        Select a solution out of all the best solutions
        Generate a local solution around the
        selected best solution
    end if
    Generate a new solution by flying randomly
    if (rand < Ai & f(xi) < (f(x*)))
        Accept the new solutions
        Increase ri and reduce Ai
    end if
    Rank the bats and find the current best x*
end while
Post procedure results and visualization
    
```

IV. DISCUSSION OF RESULTS

Five numbers of Cascaded H-Bridge inverter modules are required for an eleven level inverter. Every CHB is having four number of MOSFET switches. For 11-level inverter, 5 switching angles are required. The switching pulses for numerous values of ‘M’ and its consequent THD values for BAT algorithm is provided in table 1. It is noticeable from the table 1 that from the modulation index 0.47 to 1.075, the THD values are reducing progressively. It is to be noted that for values of ‘M’ above 0.7, the values of THD are less than 5%.

Table 1. Switching pulses and THD Values for Different Values of ‘M’

Sl. No	M	$\alpha 1$	$\alpha 2$	$\alpha 3$	$\alpha 4$	$\alpha 5$	Fitness value	THD Calculated	THD Simulated
1	0.47	38.1	50.5	69.3	84.3	89.6	6.02	10.7	9.86
2	0.50	37.7	54.5	66.5	83.5	88.7	7.32	8.12	8.91
3	0.70	12.7	30.4	48.0	89.4	89.9	3.71	6.32	6.40
4	0.80	8.65	22.7	38.9	69.2	86.5	1.88	4.91	4.94
5	1.00	6.42	14.9	25.4	37.9	58.9	2.42	3.12	3.14
6	1.07	3.43	11.9	20.7	28.5	42.7	1.43	2.96	3.02

Where M – Modulation index

The results of harmonic voltages with respect to the switching angles given in table 1 are provided in table 2. The harmonics in the order of 5, 7, 11 and 13 can be eliminated in 11-level inverter. Generally in three phase connection, the triplen harmonic voltages in the order of 3, 6, and 9 gets cancelled themselves.

Table 2. Voltage Harmonics for Different ‘M’ values

Sl. No	M	V1	V5	V7	V11	V13
01	0.47	47.8607	3.4347	1.6123	0.6312	1.2214
02	0.50	48.997	0.8163	2.5445	2.2532	0.2332
03	0.70	67.9679	1.2230	0.0901	0.1952	1.9721
04	0.80	80.0001	0.6100	0.0001	0.0003	2.5972
05	1.00	99.9932	0.1971	0.3004	0.1611	0.1112
06	1.07	107.001	1.9982	1.9662	1.7170	0.4982

Where M – Modulation index

From the modulation index 0.8 to 1.0, the harmonic voltages are very well reduced as obviously reflected in the table 2. Only a small number of harmonics are in significant altitude in all the modulation indices when compared with other harmonics, which are nearer to zero in value. The harmonic voltages V7 and V11 are somewhat leading in M = 0.5 and for M = 0.7 & 0.8, V13 is slightly major. However, when comparing with the fundamental voltage component these voltage values are very minor. All the remaining harmonic values are almost zero.

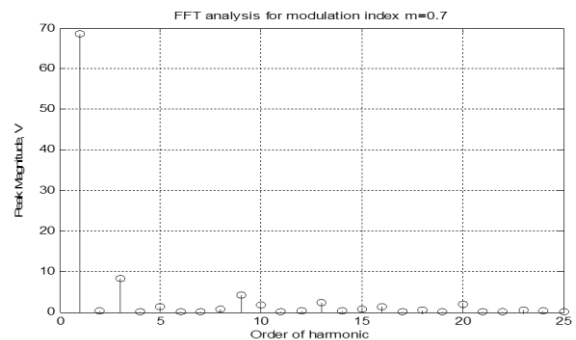


Figure 3. FFT Scale for M=0.7



BAT ALGORITHM BASED SELECTIVE HARMONIC ELIMINATION PWM FOR AN ELEVEN LEVEL INVERTER

The simulation results of Bat Algorithm (BA) for various modulation indices are specified in figures from 3 to 6. Various values of 'M' Vs Voltage Harmonics is represented in figure 7.

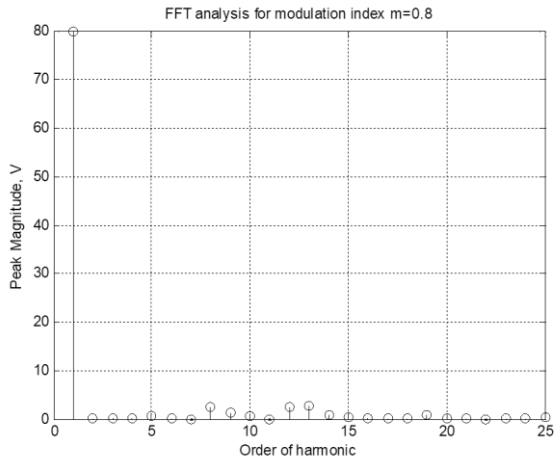


Figure 4. FFT Scale for M=0.8

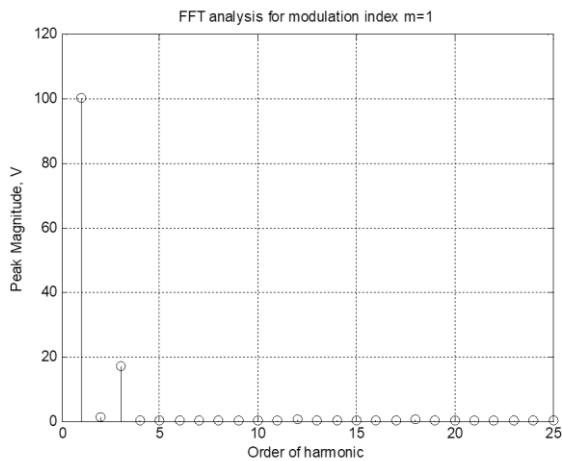


Figure 5. FFT Scale for M=1.00

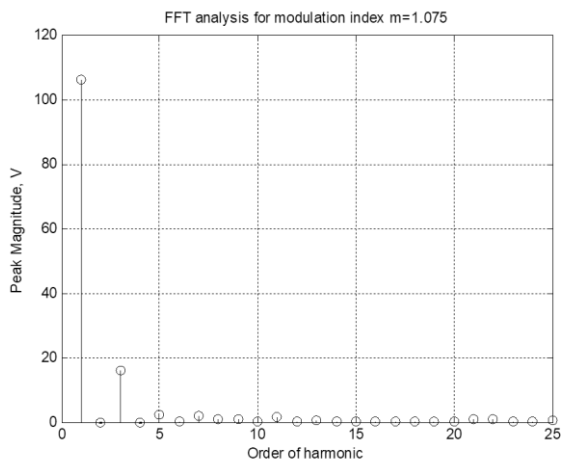


Figure 6. FFT Scale for M=1.075

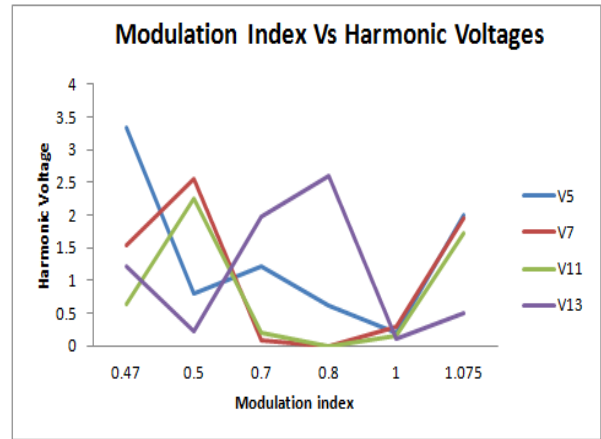


Figure 7. 'M' Vs Voltage Harmonics

THDs for various algorithms such as Bat algorithm (BA), GA and FPA are given in table 3. The results of GA and FPA [4] are taken from Srinivasan et al.. The table 3 shows that the THD values for BA and FPA are better than GA apart from M=0.7. At M=1.075 [4] the simulated and calculated values of THDs are 3.2360 and 3.2073 respectively using GA algorithm and they are 3.1730 and 3.1967 respectively for FPA algorithm, however these values are 3.02 and 2.96 respectively for BA algorithm. The THD comparison chart for BA, FPA and GA are given in figure 8. There is smaller deviation in these values for modulation index 0.47.

Table 3. THD comparative Study for BA, FPA and GA algorithms

S. No	M	BA		FPA		GA	
		THD Calculated	THD Simulated	THD Calculated	THD Simulated	THD Calculated	THD Simulated
1	0.47	10.7	9.86	10.819	10.795	10.648	9.7561
2	0.7	6.32	6.40	7.891	7.941	6.4064	6.4026
3	1.07	2.96	3.02	3.1730	3.1967	3.2073	3.2360

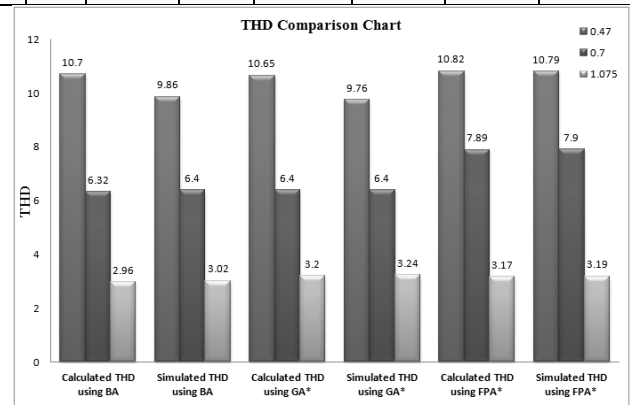


Figure 8. THD Comparative Study for BA, GA and FPA algorithms

4.1 Hardware Description

The switching pulses for the inverter unit can be produced using AVRAtmega16a Processor. BA is preferred for solving Fourier based non-linear transcendental equations for various modulation indices. A look up table is formed using these switching angles and subsequently programmed in AVRAtmega16a chip to



create triggering angles for 11-level inverter. The hardware circuit for an eleven level inverter is shown in figure 9. IR2110 is used in the driver circuits and IRF 840 MOSFET is utilised for the Cascaded H Bridges.

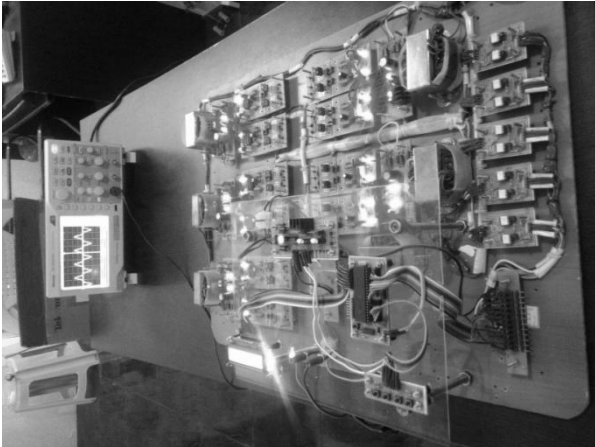


Figure 9. Hardware Circuit of an eleven level inverter

The unequal voltages of $V_{dc1}=26V$, $V_{dc2}=24V$, $V_{dc3}=22V$, $V_{dc4}=20V$ and $V_{dc5}=18V$ are given as isolated voltages. The hardware voltage output magnitude produced by using BA algorithm for the $M=1$ is given in figure 10a and its FFT wave form is given in figure 10b. While comparing the results of simulation with hardware, it is obviously shown that the harmonic contents are reduced to a minimal level.

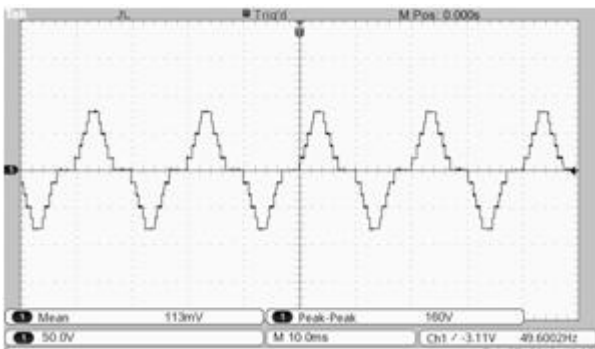


Figure 10a. Time Vs Voltage Magnitude for M=1

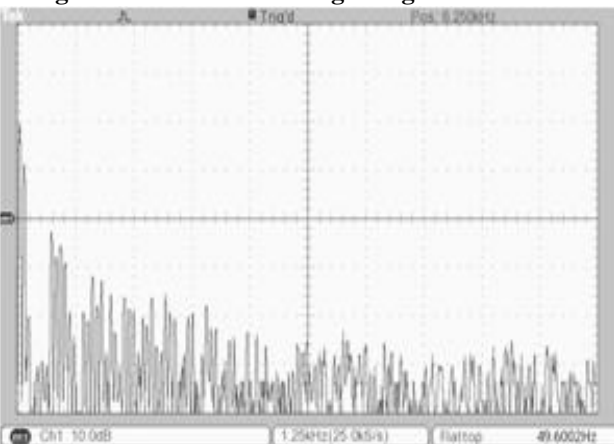


Figure 10b. FFT Scale for M=1

V. CONCLUSION

The output voltage of an eleven level inverter is shaped as a nonlinear transcendental equation using Fourier theory and is made as a constrained optimization problem, which is easily resolved by means of the proposed Bat algorithm (BA) to find out the triggering pulses. This switching pattern is

simulated in the Matlab2010Ra and utilized offline to produce triggering pulses for the hardware circuit. The simulation results were presented and validated using hardware circuit. The THD values are less than 5% particularly for the modulation indices 0.8, 1 and 1.075. The THD values have been very well minimized to 2.9 by means of the proposed work for the modulation index 1.075 when comparing with the best results arrived by GA and FPA algorithms as 3.2 and 3.1 respectively in the earlier stage. Consequently the eradication of low-order harmonics using SHEPWM method was scrutinized.

REFERENCES

1. BD Reddy, NK Anish, MP Selvan and S. Moorthi, "Embedded Control of n-Level DC-DC-AC Inverter", IEEE Transactions on Power Electronics, vol.30, no.7, pp. 3703-3711, 2015.
2. S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B.Wu, J. Rodriguez, M. Perez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters", IEEE Trans. Ind. Electron., vol. 57, no. 8, pp. 2553-2580, Aug. 2010.
3. Mariusz Malinowski and K. Gopakumar, "A Survey on Cascaded Multilevel Inverters", IEEE Transactions on Industrial Electronics, vol. 57, no. 7, July 2010
4. S.Srinivasan and R.Ganesan, "Flower Pollination Algorithm based Selective Harmonic Elimination PWM for an Eleven Level Inverter", Asian Journal of Research in Social Sciences and Humanities, vol.6, no.6 special, pp.69-84, June 2016.
5. S.Srinivasan and R.Ganesan, "Selective Harmonic Elimination Algorithm for a Boost H Bridge Inverter with Reduced Switch Configuration", Journal of Electrical Engineering, vol. 18, no. 1, pp. 1-6, 2018.
6. Holmes, DG & McGrath, BP 2002, 'Multicarrier PWM strategies for multilevel inverters', IEEE Transactions on Industrial Electronics, vol. 49, no. 4, pp. 858-867.
7. Holtz 1992, 'Pulse width Modulation-A Survey', IEEE Transactions on Industrial Electronics, vol. 39, no. 5.
8. J. Chiasson, L.M. Tolbert, K. Mckenzie, and Z. Du, "Eliminating harmonics in a multilevel converter using resultant theory", Proc. Power Electron. Specialists, 2002, pp. 503-508.
9. J. I. Leon, S. Vazquez, J. A. Sanchez, R. Portillo, L. G. Franquelo, J. M. Carrasco, and E. Dominguez, "Conventional space-vector modulation techniques versus the single-phase modulator for multilevel converters", IEEE Trans. Ind. Electron., vol. 57, no. 7, Jul. 2010.
10. Ahmadi, D., Zou, K., Li, C., Huang, Y., & Wang, J, "A Universal Selective Harmonic Elimination Method for High-Power Inverters", IEEE Transactions on Power Electronics, vol.26, no.10, pp.2743-2752, 2011.
11. Pulikanti, R.Sridhar and Vassilios G. Agelidis, "Hybrid Flying-Capacitor-based Active-Neutral-Point-Clamped Five-Level Converter Operated with SHE-PWM", IEEE Transactions on Industrial Electronics, vol.58, no.10, pp.4643-4653, 2011.
12. Khaled El-Naggar and Tamer H. Abdelhamid, "Selective Harmonic Elimination of New Family of Multilevel Inverters using Genetic Algorithms", Energy Conversion and Management, vol.49, pp.89-95, 2008.
13. Kavousi, Ayoub, et al., "Application of the Bee Algorithm for Selective Harmonic Elimination Strategy in Multilevel Inverters", IEEE Transactions on Power Electronics, vol.27, no.4, pp.1689-1696, 2012.
14. S.Srinivasan and R.Ganesan, "Enriching Electric Power Quality

BAT ALGORITHM BASED SELECTIVE HARMONIC ELIMINATION PWM FOR AN ELEVEN LEVEL INVERTER

- by using Bee Algorithm in Shunt Active Fileters”, International Review on Modelling and Simulations, Vol.7, no.4, pp. 605-612, 2014.
15. H.Taghizadeh, and M. TarafdarHagh, "Harmonic Elimination of Cascade Multilevel Inverters with non-equal DC Sources using Particle Swarm Optimization", IEEE Transactions on Industrial Electronics, vol.57, no.11, pp.3678-3684, 2010.
 16. Maia, H. Z., Mateus, T. H., Ozpineci, B., Tolbert, L. M., & Pinto, J.O, "Adaptive Selective Harmonic Minimization based on ANNs for Cascade Multilevel Inverters with Varying DC Sources", IEEE Transactions on Industrial Electronics, vol.60, no.5, pp. 1955-1962, 2013.
 17. Javier Chivite-Zabalza, Miguel Angel Rodriguez Vidal, Member, Pedro Izurza-Moreno, Gorka Calvo, and Danel Madariaga, "A Large Power, Low-Switching-Frequency Voltage Source Converter for Facts Applications with Low Effects on the Transmission Line", IEEE Transactions on Power Electronics, vol. 27, no.12, pp.4868-4879, 2012.
 18. S. Muthubalaji, N. Karuppiah, and R.Anand, "Performance Improvement of Distribution System by Optimal Placement and Sizing of Distributed Energy Storage Systems and DGS Using Particle Swarm Optimization Algorithm", Jour of Adv Research in Dynamical & Control Systems, Vol. 10, 14-Special Issue, pp.864-871, 2018.
 19. J.Shanmugapriyan, N. Karuppiah, S. Muthubalaji and S. Tamilselvi, "Optimum Placement of Multi Type DG Units for Loss Reduction in a Radial Distribution System Considering the Distributed Generation Suitability Index using Evolutionary Algorithms", Bulletin of the Polish Academy of Sciences Technical Sciences, vol. 66, no. 3, pp.345-354, 2018.
 20. S.Muthubalaji, R.Anand, N.Karuppiah, "An Integrated Optimization Aapproach to Locate the D-STATCOM in Power Distribution System to Reduce the Power Loss and Total Cost", Periodicals of Engineering and Natural Sciences, Vol.6, No.2, pp. 283~294, 2018.
 21. X.-S. Yang, A New Metaheuristic Bat-Inspired Algorithm, in: Nature Inspired Cooperative Strategies for Optimization (NISCO 2010) (Eds. J. R. Gonzalez et al.), Studies in Computational Intelligence, Springer Berlin, 284, Springer, 65-74 (2010).