Performance Research of Seven Level Multi-Level Inverter with Reduced Switches using Various PWM Techniques

Boya. Anil Kumar, R.Anand

Abstract: ***A inverter is basically a device that usually converts DC to AC voltage without causing any power loss, applicable to only low to medium voltage applications. But in case of medium to high power applications, it has demerits like high switching losses, reduced cost and low efficiency. To overcome these demerits a Multilevel inverter applicable to high voltage and high-power applications which have low total harmonic distortion (THD) is introduced. This paper is mainly focused on seven-level inverter with five switches and four dc sources. with low total harmonic distortion, less switching loss without adding any complexity to the circuit. The switching topology is integrated with various SPWM techniques like Phase Disposition (PD), Phase Opposition Disposition (POD) and Anti Phase Opposition Disposition (APOD). For better performance of the inverter above three PWM techniques will be compared and analyzed to find the low THD configuration. The simulation of switching topology is done by MATLAB/Simulink.***

Keywords: Reduced switches, different PWM techniques, low harmonic distortion, MATLAB/Simulink.

I. INTRODUCTION

Generally, an inverter is a two-level inverter which means a conventional two-level inverter which generates only up to two levels of the output voltage. The conventional two-level inverter produces THD around 55% under normal operating conditions with power loss caused by AC utilities at high-frequency applications [1].

For high voltage applications, switches are connected in series, there is a voltage sharing between them.

Even if a converter is to be in OFF state there is a reverse voltage sharing takes place. For high current applications, switches are connected in parallel, a large amount of current stress present because each switching device cannot have a phase shift by 180 degrees, the heat generated will cause damage to the device[1].

To overcome the above demerits a Multilevel inverter was introduced [2], which presents an increased number of switches instigating high THD.

I. Existing Topologies

Use of a single DC power source (e.g., a battery or a fuel cell stack) with the remaining n-1 DC sources being capacitors a cascaded multi-level inverter is designed [3].

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Efficient multicarrier SPWM for cascaded H-Bridge symmetrical multilevel inverter was proposed to enhance the better quality of the output voltage waveform with a better harmonic spectrum [4]. Derived from the conventional two-level inverter SPWM technique multi-carrier Sine Pulse Width Modulation (SPWM) techniques are being broadly used for different multilevel inverter topologies [5]. Symmetrical Multilevel inverter (SMLI) topology with three-phase system is introduced to reduce the THD values [6]. A bipolar and unipolar PWM technique offers the features of effectively doubling the switching frequency of the output voltage, under different conditions of modulation index, the pattern is utilized to estimate the harmonics [7]. Level Shifted [LS] Scheme is applied to the Cascade H-bridge multilevel inverter for medium voltage high power efficiency inverters in industrial application [8]. A topology of single phase five level cascaded H-bridge multilevel inverter by using only five switches and two DC power source for lower electromagnetic interference generation and high output voltage was introduced [9]. Derived from the conventional two-level inverter SPWM technique multi-carrier Sine Pulse Width Modulation (SPWM) techniques are being broadly used for different multilevel inverter topologies [5]. Modular Multilevel Converter with Cascaded H Bridge Inverter using Five, Seven and Nine levels were introduced [10]. Specific Harmonic Elimination (SHE) technique for angle optimization of modulation index was introduced to get low THD values [11].

The cascaded Multilevel H bridge inverter is to operate in single phase and three phase. In the case of single-phase, two H bridge having two legs totally 8 devices will be present. The single H bridge full wave inverter will produce a positive, negative and zero voltages.

The five-level inverter generates output voltages +2Vdc, +Vdc, 0, -Vdc, -2Vdc by two dc sources with different combinations of four switches. There is no current on switching devices because each switch phase shift by 180 degrees, produces a staircase waveform with positive, negative legs switching devices[3].

The generalized equation for single phase H bridge inverter is

N=(2*V)+1

N=Number of levels

V= Number of voltage sources.

For e.g., we assume the number of voltage sources to be two then the number of voltage levels will be five.

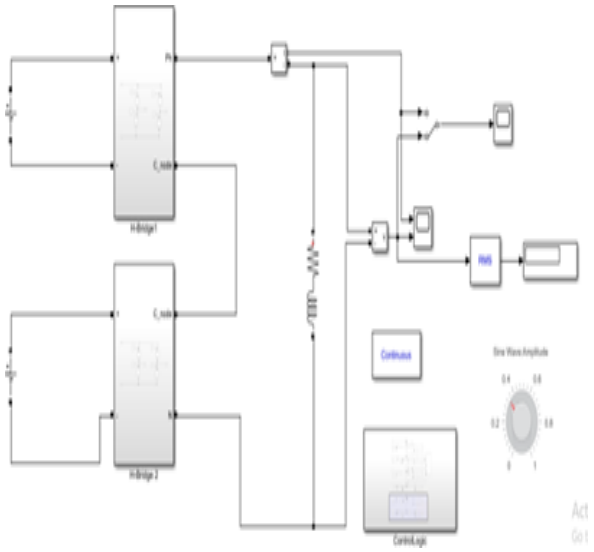

Fig.1: Simulation circuit of a five-level inverter

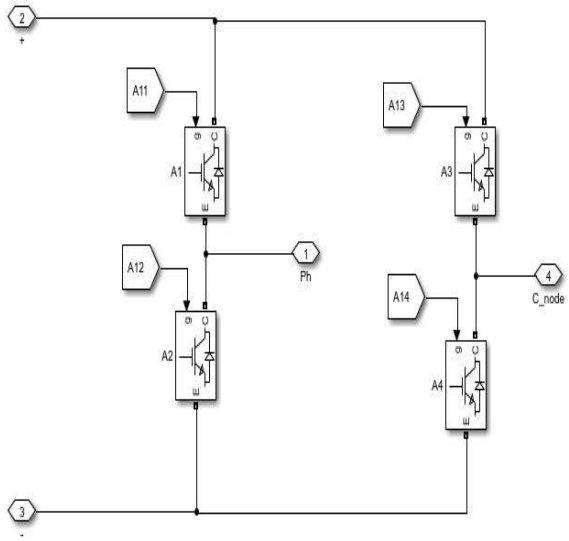

Fig.2: H Bridge for first dc source

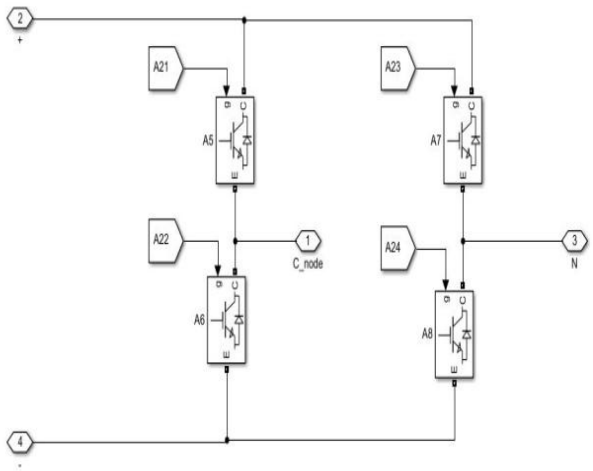

Fig.3: H Bridge for second dc source

From the control logic circuit shown below, consisting of four carrier generator because for

Number of carrier = Number of levels - 1
= 5 - 1
Number of carrier = 4

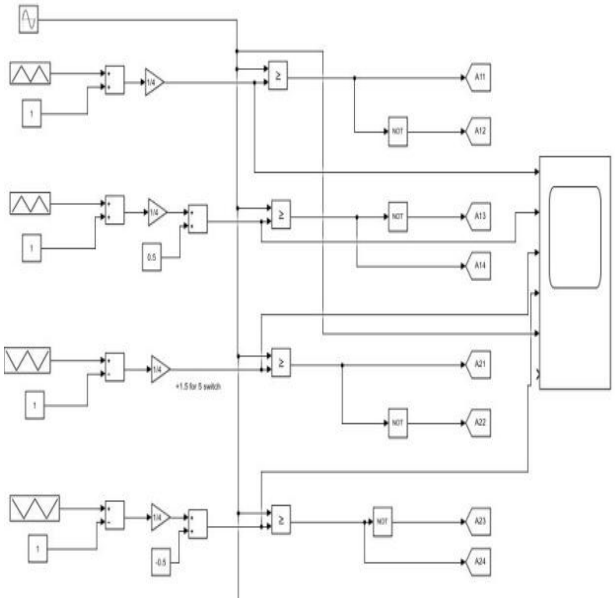

Fig.4: Control Logic circuit for five level

And also in which two triangular generators above zero phase are with the same phase shift and remaining phase shifted by 180 degrees below zero phase and one sine wave as a reference by comparing with triangular generator produces a switching pulse[7].

Switching Pulse:

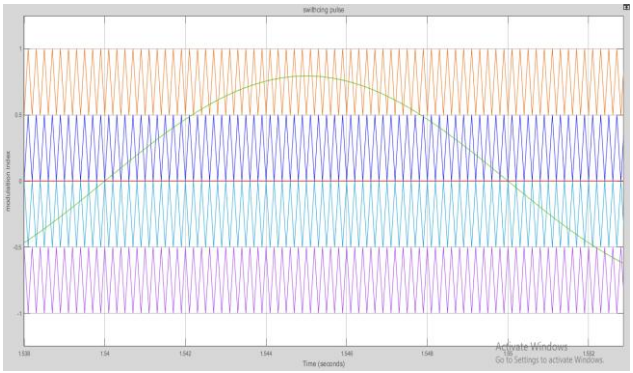

Fig.5: Switching pulse for five level

Output Waveform:

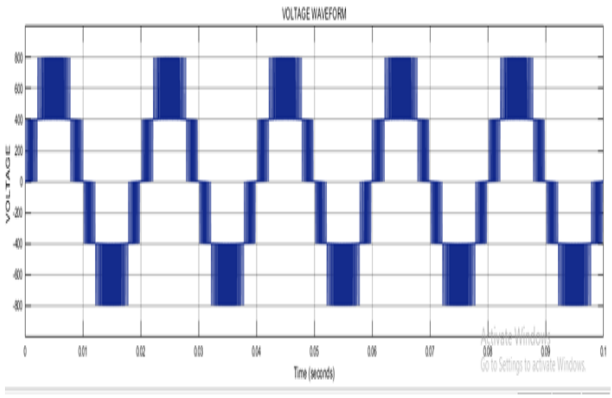

Fig.6: Five level waveform

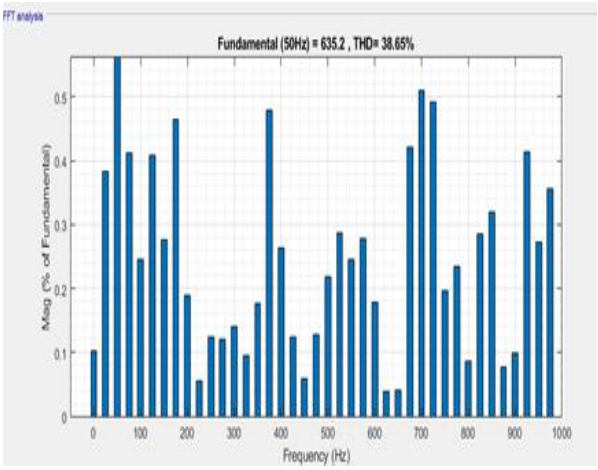

Fig.7: Five level THD

The FFT analysis gave a THD of 38.65% with 8 switches and two dc sources. To reduce the THD, anew topology for a Seven level inverter with 5 switches using four dc sources is designed. It also employs various Pulse Width Modulation Techniques and results are compared and analyzed.

II. PROPOSED SEVEN LEVEL 5 SWITCH TOPOLOGY USING FOUR DC SOURCES

The proposed seven-level inverter consists of 5 switches and 4 dc isolation sources. It is the simplest design and it can produce 7level for 4 dc source and 9 levels for 5 dc sources.

Table:1 Switching topology for seven level

S NO	S_1	S_2	S_3	S_4	S_5	OUTPUT VOLTAGE
1	OFF	OFF	ON	OFF	ON	$+V_{dc}$
2	OFF	ON	OFF	OFF	ON	$+2V_{dc}$
3	ON	OFF	OFF	OFF	ON	$+3V_{dc}$
4	OFF	OFF	OFF	OFF	OFF	0
5	ON	OFF	OFF	ON	OFF	$-V_{dc}$
6	OFF	ON	OFF	ON	OFF	$-2V_{dc}$
7	OFF	OFF	ON	ON	OFF	$-3V_{dc}$

From fig.8 we can observe that the switches S1 S2, S3 are to be unidirectional otherwise the output waveform will get distorted. For reducing a switching losses is done by reduces the switches.

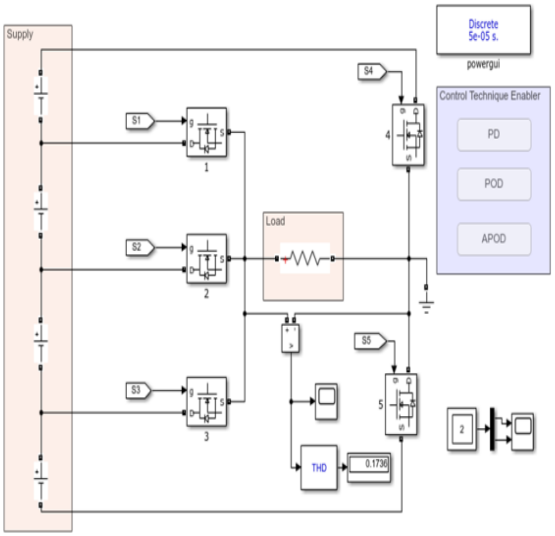

Fig.8: Basic simulation circuit for seven level

III.METHODOLOGY

Pulse width modulation: The pulse width modulation technique is the controlling technique of an inverter. For a conventional two-level inverter used in adjustable speed drive has a large amount of THD which is usually above 60%.

For such multilevel inverters to make the THD as low as possible the number of voltage levels has to be increased which will make the circuit more complex. There are three alternative pulses with different phase relationships. For the level shifted multicarrier modulation three alternative carrier disposition pulse modulation strategies are commonly used.

The switching topology is carried with two different techniques like phase shift and level shift in which level shift will give THD low compared to phase shift. This level shifting is further divided into three techniques.

- Alternative phase opposition disposition[5],[6],[8]
- Phase opposition disposition[5],[6],[8]
- Phase disposition[5],[6],[8]

IV.SIMULATION RESULTS OF SEVEN LEVEL FOR VARIOUS PULSE WIDTH TECHNIQUES

The below diagram is the basic simulation circuit

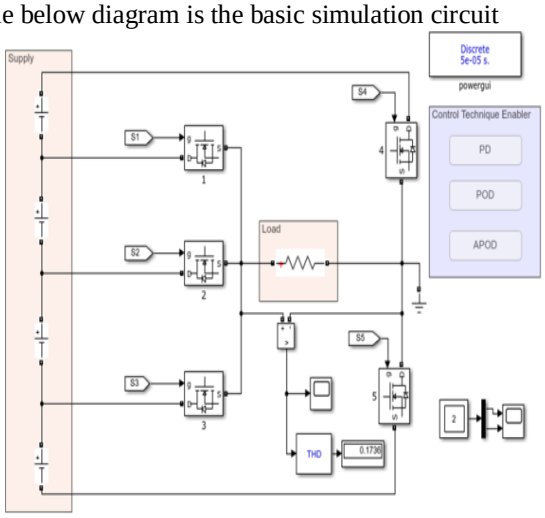

Fig.9: For the switches are ON and OFF with respect to the switching pattern

For S3 and S5 ON

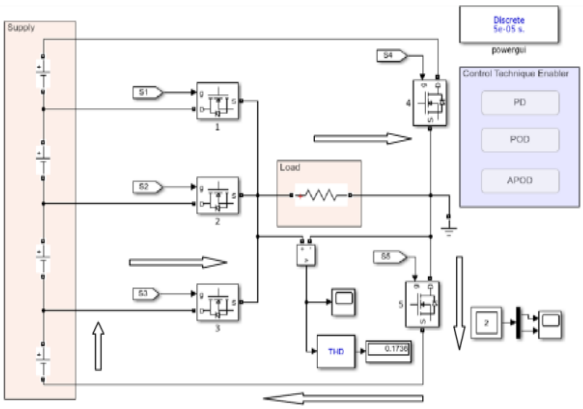

Fig.10: switch S3 and S5 on

Working

The output voltage +Vdcis estimated by S3 and S5 on as shown above in fig.10. Then the current will flow through S3 to R load to S5, it will produce initial voltage +Vdc.

For S2 and S5 ON

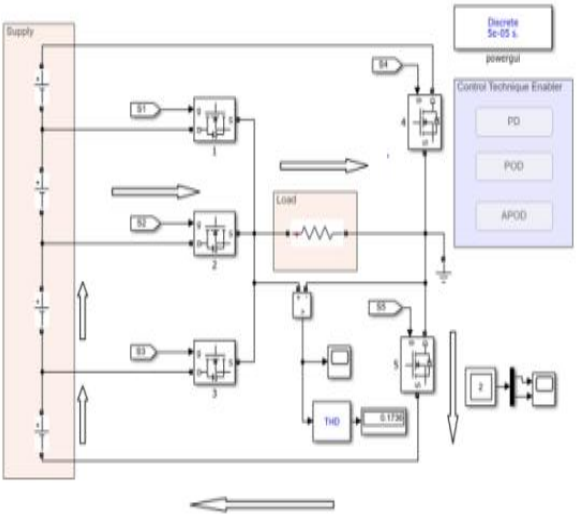

Fig11: S2 and S5 ON

Working

Output voltage +2Vdc is estimated by S2 and S5 on as shown in the above-labeled diagram. The current will flow through S2 to R load to S5, it will produce the initial increment of voltage.

For S1 and S5 ON

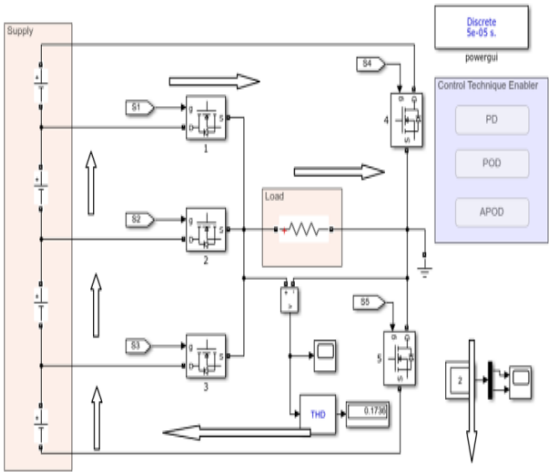

Fig.12: S1 and S5 ON

Working

The output voltage of +3Vdc is generated when S1 is ON as shown above in the labeled diagram. Then current will flow through to S1 to R-load to S5, the output voltage will be incremented.

V.SIMULATION AND PULSE GENERATION RESULTS

The pulse generation is done by Simulink for the existing topology using eight switches and two dc sources. The harmonic distortion is seen by FFT window in Matlab.

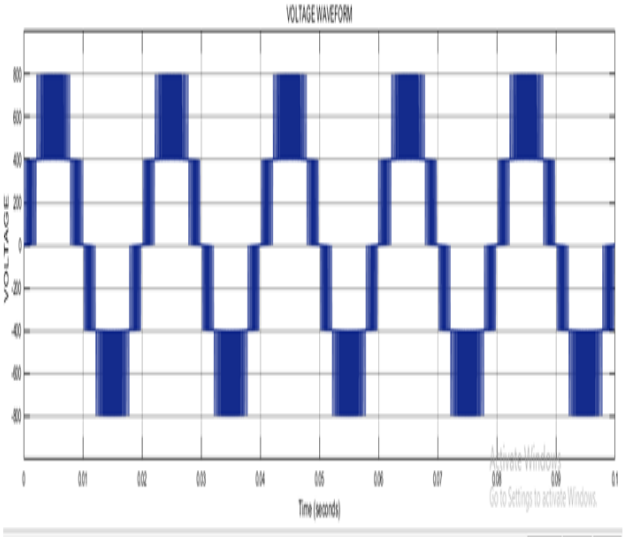

Fig.13: Five levels using two H bridges

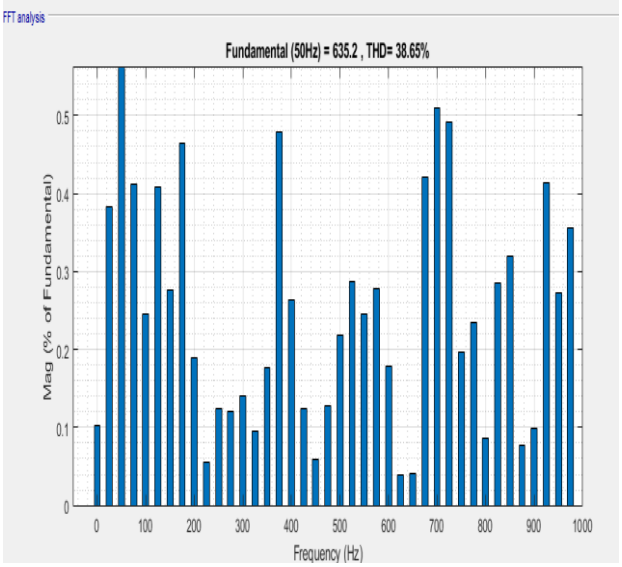

Fig.14: Five level THD

Proposed topology simulation results

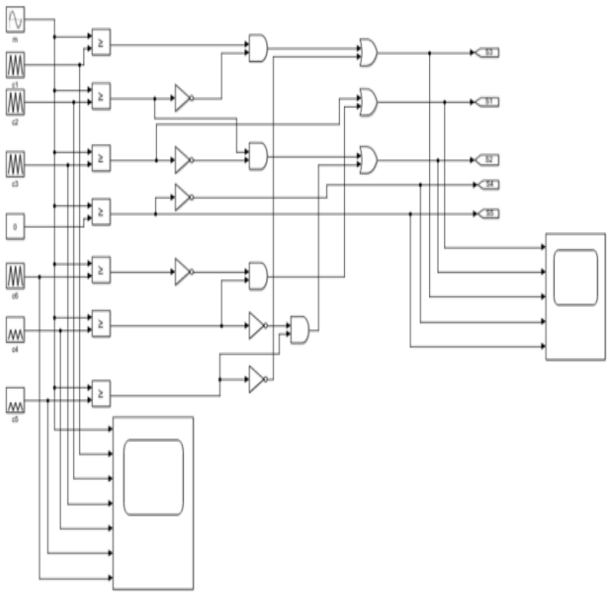

Fig.15: pulse generation circuit for PWM techniques

From the above control logic circuit, we conclude that carrier signals are generated by seven-level inverter based on below,

Number of carrier waves= Number of levels - 1

=7 - 1

Number of carrier waves = 6

For example, consider only switching pulse for POD

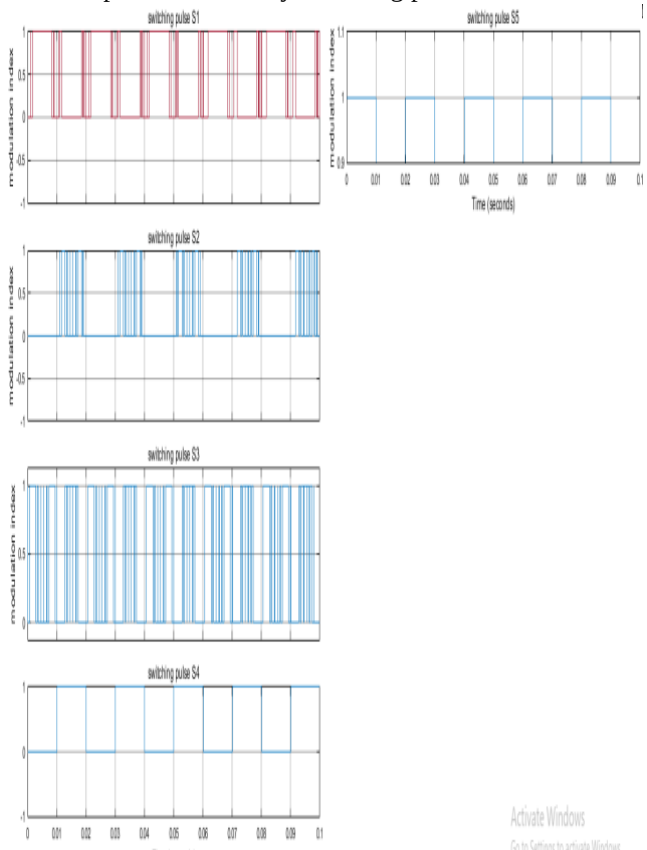

Fig.16: Switching pulse POD

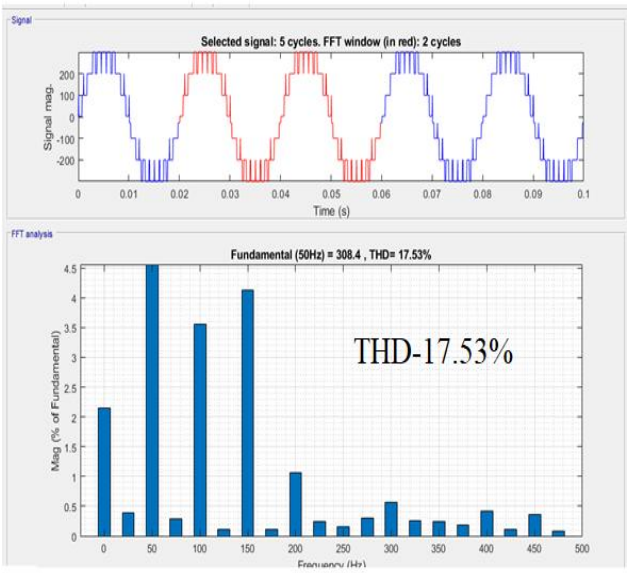

Fig 17: THD with PD

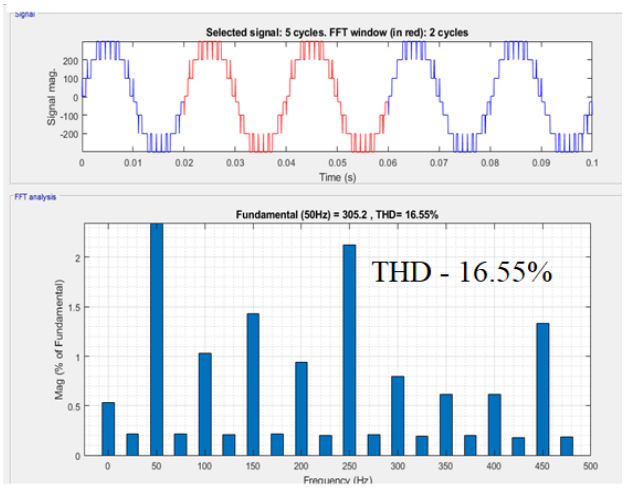

Fig 18: THD with POD

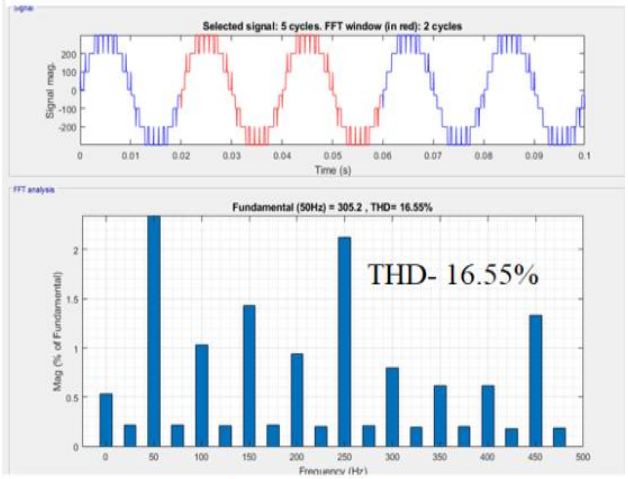

Fig 19: THD with APOD

For proposed topology, In Matlab, signal to analyze and FFT analysis seen by clicking a powergui in which tools>>>select FFT Analysis it will display the THD. Here the cycles/sec = 2, selected signals =5 from that it produces the signal window which is the voltage magnitude, in this case, it produces an output voltage +300 to -300.

The existing and proposed topologies THD values are as shown below

Table:2 comparison between existing and proposed topology

Existing topology	THD	Proposed topology	
Cascaded H bridge Five level inverter	38.65%	PWM TECHNIQUE	THD
		PD	17.53%
		POD	16.55%
		APOD	16.88%

VI. CONCLUSION

In this paper, a new topology of seven-level inverter with 5 switches, 4 dc sources is proposed and simulated by MATLAB/SIMULINK. It can be seen that low THD

reduction takes place in POD as compare with APOD, PD techniques, for improvement of efficiency, reduce cost, low harmonic distortion.

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