Performance Research on Variable Data Rate Reconfigurable Architecture for SDR Receiver

Nataraj URS, R Venkatasiva Reddy

Abstract:- In Early days, communications systems used amplitude and frequency modulation schemes in which bandwidth constraint is one of the major challenge to accommodate more data rates. As the data rate requirement increased drastically till date, The applications demands more data rates for communication using less bandwidth is considered as an efficient communication system. For achieving communication with high data rates using less bandwidth, technology migrated to digital modulation schemes. In this phase new modulation techniques like ASK, FSK, PSK were realised. ASK and FSK modulation schemes bandwidth efficiency is less as compared to PSK schemes. For best utilisation of bandwidth efficiency and less inherent noise levels, PSK schemes are used, which is suitable for high data rate applications. In this paper QPSK modulation and demodulation technique is selected for realising the variable data rate in the range of 1.2MBPS as the best bandwidth with efficient reconfigurable architecture designed for software defined radio receiver.

Keywords— Modulation, SDR, QPSK, QAM, FPGA, Reconfigurable Architecture.

I. INTRODUCTION

Digital modulation techniques have great utility in present communication systems. Communications systems can be broadly classified into three categories, which are cost efficient, bandwidth efficient, and power efficient techniques. Bandwidth efficiency defines whether a modulation technique can accommodate data into limited bandwidth. Power efficiency defines about the system ability at the lowest practical power levels to send information reliably. Among these bandwidth efficiency is given highest priority. The optimization of particular system has been done depending on the specifications of that particular system.

Digital modulation techniques have greater capability to pass information in larger amount than compared to analog modulation techniques. Digital modulation techniques can be easily designed and executed with I/Q modulators. Majority of the digital Modulation systems maps the data to a number of discrete points on the I/Q plane. These discrete points called as constellation points. The amplitude and phase modulation takes place when the signal transits from one point to another. Efforts are made to execute amplitude modulation and phase modulation techniques (difficult and complex) are promptly done at the maximum extent. PSK is widely used in the communication industries forbuilding latest technology radios etc. There are 3 types of QPSK models they are quadrature PSK (QPSK), differentialQPSK (DQPSK) and offset QPSK (OQPSK). Out of these models we are studying only QPSK modulation schemes.

Quadrature Phase shift keying (PSK)

Compared to all other M-PSK techniques, QPSK method is most widely used since the BER degradation will not be affected when there is an increase in bandwidth efficiency. In other MPSK schemes, BER performance will be affected due to increase in bandwidth efficiency.

QPSK signals are defined as

$$S_i(t) = A \cos (2\pi f_c t + \theta_i), \quad 0 \le t \le T, \quad i = 1,2,3,4$$

where $\theta_i = (2i -1) \pi / 4$

II. PURPOSE AND METHODOLOGY

New technology radios that are under development in development and engineering, military communication equipments like LTE, PTMP radio, High data rate radio relay, Wimax, Software defined radios this waveform is used for reliable communication.

QPSK modulation and demodulation waveform is widely used in communications systems. Where reliable communication is an important criteria. Recent developments in radio communication field will have QPSK modulation as one of modulation scheme.

Implementation of QPSK modulation and demodulation waveform on virtex-4 FPGA platform with 1.250Mbps data rate has been realised and demonstrated with real time application in this project, and also this waveform developed with Verilog HDL and can be ported directly to any Xilinx FPGAs.

The Transmitter and Receiver of QPSK modem are Simulated on System Generator (Simulink Matlab). This model can be synthesised to be used as a Component in the FPGA after ensuring that the Simulation is giving the required parametric results in terms of the symbol recovery, Symbol Spread, Symbol convergence time, Carrier Recovery and true bit recovery. The phase, amplitude and frequency impairments can be added to the Test Modulated QPSK signal given to the demodulator during simulation. And this simulated matlab blocks is converted into Verilog code with Xilinx system generator by assigning the data rate and clock signals in virtex-4 base band processor card as per the hardware, the required waveform has been developed.

The QPSK receiver is targeted for a BER of 10e-6 BER. An AWGN channel is simulated and the input to the receiver

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Nataraj Urs H D, Associate Professor, & Research Scholor, School of ECE, REVA University, Bangalore, Karnataka, India.(Email: ursnatraj@gmail.com)

Dr. R Venkatasiva Reddy, Professor, School of ECE,REVA University Bangalore, Karnataka ,India.(Email: venkatasivareddy@reva.edu.in)

would have AWGN noise added transmitted wave. Five Main Algorithms run in the receive path to faithfully recover the Transmitted data at the given BER during the Demodulation process. The Signal received would have undergone Phase, Amplitude impairments in the channel Medium, AWGN noise too adds up to the received signal.

These impairments are nullified by the following algorithms running together.

1. Timing recovery Algorithm (Gardner Timing Recovery)
2. Automatic gain Control.
3. Carrier Frequency Correction algorithm (Costal loop)
4. Phase imbalance Correction algorithm.
5. Time Domain Equaliser.

III. DESIGN APPROACH & RESULTS

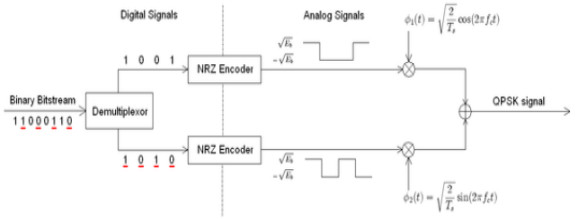


Figure 1: Transmitter block diagram

A. Scrambler

Scrambler is used to Randomize the incoming data to prevent Repeating bit pattern which may lead to a poor Gardner timing recover Performance and poor bandwidth utilization. Without scrambler the PA would be expected to be highly linear.

The polynomial used is $1+x^{18}+x^{23}$

The PRBS sequence will repeat after (2^23)-1 bits. The scrambler used is a multiplicative scrambler which has the self-synchronizing capability.

$$y[n]=x[n]+y[n-18]+y[n-23]$$

When the randomized data is given as the input to the scrambler then at the descrambler the output was perfect without any errors.

Preamble appending Module

Preamble	Data_bits	Preamble	Data_bits	Preamble	Data_bits	Preamble

Figure 3: Preamble appending module

This module Appends a known Pattern of data of 16 bytes to every 512 bytes of data received from the DLL layer for Framing purpose.

Sync_pattern = 16 bytes of data

Data_bits = 4096 bits of data

The Preamble denoted in the image above is formed using a programmable sync pattern. The data bits remain the same. For framing all the incoming data, an FSM has been designed. The FSM transmits the sync pattern followed by 4096 bits of actual data to be transmitted. The output of the Framing block is sent to FEC Encoder for Encoding. There is no change in the data rate.

B. NRZ coding and Symbol Mapper

In QPSK, the phase shifts are 0°, 90°, 180°, −90° corresponds to data '00', '01', '11', '10'. In order to restrict the erroneous symbol decisions to single bit error, the adjacent symbols in the transmitter constellation should not differ more than one bit.

Symbol rate is given by the ratio of Bit rate to the No of bits per symbol.

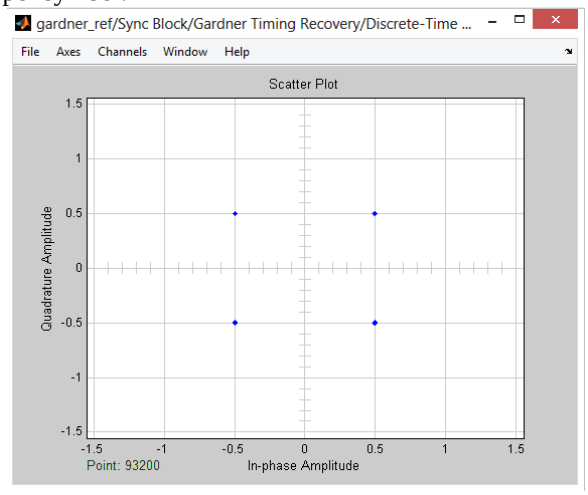


Figure 2: Transmitter Constellation Mapper Output

symbol rate derivations:

Input data rate of modem = 2Mbps
FEC = NA
Over Head Data = 1.15 Mbps
Data rate after FEC = NA
DQPSK => 1 symbol = 2 bits
Symbol rate = 1.575 = 3.15/2 Mbps
Samples per symbol = 16
Sampling rate = (3.15Mbps/2)*16;

Hence effective sampling rate for 3.15Mbps with 16 samples per symbol = 25 Mega samples per second => 25 MSPS

Receiver Block

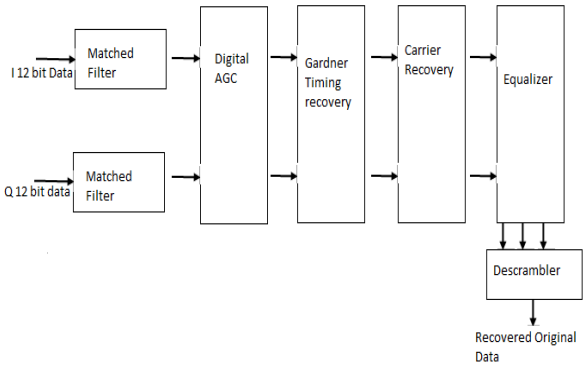


Figure 4: Receiver block diagram

C. Matched Filter:

SRRC filter used in the transmitter is used in receiver. The received samples are convolved with the SRRC filter. The SRRC filter is the matched filter. The number of taps in the receiver SRRC filter is dependent on the sampling rate. Since the sampling rate is 25 MSPS, there are 16 samples per symbol. Hence the number of coefficients for the SRRC filter is 16x6 = 96. After filtering the eye opening is formed and the

0 ISI sample can be picked in the timing synchronization algorithm. Digital AGC has been bypassed in this work.

D. Symbol timing offset estimation and correction: (Gardner Algorithm):

Symbol timing synchronization is a method which estimates clock signal that is aligned to both phase and frequency with the clock used for generating data in transmitter. Because it is not efficient in allocating spectrum (which transmits separate clock signal from the transmitter) to the receiver for the purpose of synchronization of timings, the data clock must be extracted from the noisy received waveform that carries the data. For matched filter detectors, the clock signal is used to identify the instants when the matched filter output are sampled.

Gardner algorithm is based on ZCTED which is based on detecting zero crossing in eye diagram. It is a purely non data aided algorithm. The error signal is calculated using the Equation below.

$$e(k) = x\left((k-1/2)T_s + \hat{\tau}\right)\left[x\left((k-1)T_s + \hat{\tau}\right) - x\left(kT_s + \hat{\tau}\right)\right].$$

The Timing recovery Algorithm has four sub modules:

1. Interpolator
2. TED Module
3. Loop Filter
4. Interpolator controller

Interpolator

The interpolator module works on the principle of Piece wise Polynomial interpolation. Whose underlying equation is, (with reference to the figure below)

$$x((m(k)+\mu(k))T) = c_1((m(k)+\mu(k))T) + c_0.$$

$$x((m(k)+\mu(k))T) = \mu(k)x((m(k)+1)T) + (1-\mu(k))x(m(k)T)$$

Input Specification:

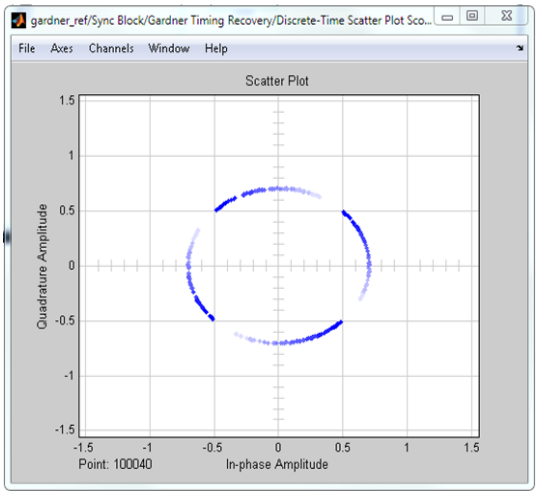
The I and Q input SNR for achieving BER 1E-06	Minimum : 14 dB Nominal : 16dB
The I and Q input Voltage level	Minimum: 400Vpp Nominal : 1Vpp

General Specification:

1. Max Power Consumption at 19.476 Msps: 12.5W
2. Max Current Drawn by the card at 5V input: 2.5A
3. LVDS Clock and Data input voltage : 2.5V
4. LVDS Clock and Data output voltage: 2.5V

E. Receive chain Simulink model

The matlab Simulink model captured for complete demodulation scheme that has been implemented as per the design approach to recover the clock and data.



Figurev5:IQ output after carrier signal (Gardner recovery)

This is the carrier recovered signal with carrier offset measured in chipscope, where carrier offset of 90 degrees is intentionally made present to show the constellation looks like an circle.

This is the original demodulated signal without carrier offset to show the simulated result which meets the design requirement for recovering the original required data.

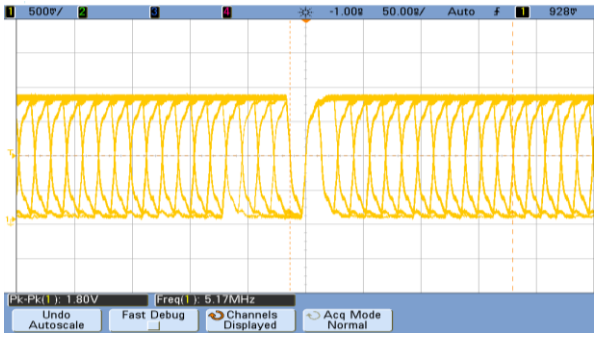


Figure 6 : ADC digital I and Q data output

This screen shots indicates that the I and Q signals are captured in Xilinx chipscope are further analyzed during the implementation of the algorithm.

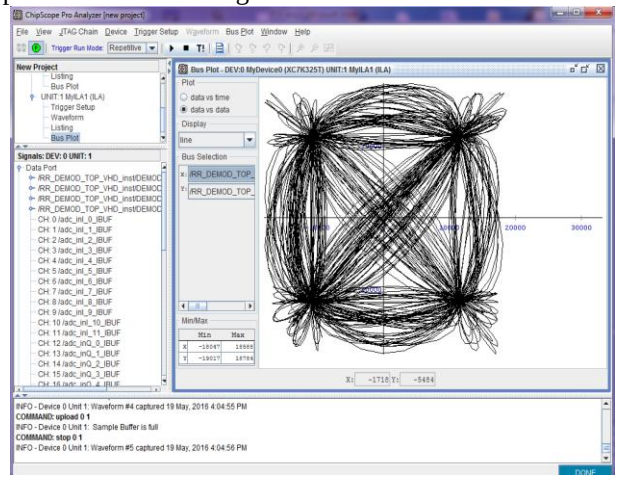


Figure 7 : I and Q constellation for QPSK

The I and Q constellation measured in chipscope without any offset in the received signal.

IV. ADVANTAGES

1. Since this design is done with Verilog HDL and can be ported directly to any Xilinx FPGAs.
2. For development of higher modulation schemes, this can code can be directly used only with minor modifications in the software portion.
3. Reduces designer's development time.
4. Cost effective solution for the system developers.

V. APPLICATIONS

1. Used in 8/34Mbps Radio Relay as one of the modulation scheme for realising the radio.
2. Used in SDR radio for realising low data rate and high data rate waveforms.
3. Used for concept proving and realisation of point to multi point radios etc.

VI. CONCLUSION AND FUTURE WORK

The QPSK demodulation scheme is an bench mark for achieving demodulation of other higher order modulation schemes like 16QAM, 32QAM, 64QAM etc. this can be achieved by only doing change in gardner timing error detector the rest demodulation process remains the same. This reduces significant time in re writing the whole demodulation algorithm for higher modulation schemes. But to achieve 0 BER, the receive SNR needs to be better than that of QPSK. Moreover the transmit signal quality should be better than that of QPSK. As the complexity of receiver or baseband hardware increases for higher modulation schemes, only minor modifications required to be changed in the software for achieving the required output.

QPSK modulation and demodulation waveform is used in radio development and application projects like PTMP radio and High data rate radio relay, Software defined radios.

Since this waveform developed with verilog HDL and can be ported directly to any FPGAs for realising the higher data rate modulation schemes.

REFERENCES

1. A. Kapoor, "A Reconfigurable Architecture of Software-Defined-Radio for Wireless Local Area Networks," 2005.
2. A. kumar Kaushik, "A Comparative Study of Software Defined Radio and Cognitive Radio Network Technology Security," pp. 104–110.
3. M. B. Blanton, "An FPGA Software-Defined Ultra Wideband Transceiver An FPGA Software-Defined Ultra Wideband Transceiver," Master Sci., 2006.
4. X. Zhang, J. Ansari, M. Arya, and P. Mähönen, "Exploring parallelization for medium access schemes on many-core software defined radio architecture," Proc. Second Work. Softw. radio Implement. forum - SRIF '13, p. 37, 2013.
5. F. Buchali, F. Steiner, G. Böcherer, L. Schmalen, P. Schulte, and W. Idler, "Rate Adaptation and Reach Increase by Probabilistically Shaped 64-QAM: An Experimental Demonstration," in Journal of Lightwave Technology, 2016.
6. C. Zhang, Dynamically Reconfigurable Architectures for Real-time Baseband Processing, no. May. 2014.
7. L. Zhao, H. Shankar, and A. Nachum, "40G QPSK and DQPSK modulation," Inphi Corp., 2008.
8. P. Dong, C. Xie, L. Chen, L. L. Buhl, and Y.-K. Chen, "112-Gb/s monolithic PDM-QPSK modulator in silicon," Opt. Express, 2012.
9. Nataraj Urs H D and Dr.Venkat Siva Reddy, "Implementation and Analysis of Low Frequency Transceiver for SDR Platforms," Jour Adv Res. Dyn. Control Syst., vol. 10, no. 04–Special Issue, pp. 1–9, 2018.
10. Nataraj Urs H D and T. Lavanya, "Design and Implementation of FM modem on FPGA for SDR using Simulink," vol. 5013, no. 5, pp. 1058–1061, 2016.
11. Nataraj urs H D and Dr.Venkat Siva Reddy, "Implementation and Analysis of Low Frequency Transceiver for SDR Platforms," Jour Adv Res. Dyn. Control Syst., vol. 10, no. 04–Special Issue, pp. 1–9, 2018.
12. C. Y. Chen, F. H. Tseng, K. Di Chang, H. C. Chao, and J. L. Chen, "Reconfigurable software defined radio and its applications," Tamkang J. Sci. Eng., vol. 13, no. 1, pp. 29–38, 2010.
13. P. Suarez-Casal, A. Carro-Lagoa, J. A. Garćia-Naya, and L. Castedo, "A multicore SDR architecture for reconfigurable WiMAX downlink," Proc. - 13th Euromicro Conf. Digit. Syst. Des. Archit. Methods Tools, DSD 2010, no. Cc, pp. 801–804, 2010.
14. H. Goyal, J. Saxena, and S. Dewra, "Performance Evaluation of OWC Using Different Modulation Techniques," J. Opt. Commun., vol. 37, no. 4, pp. 33–35, 2016.
15. V. Kumar, Nataraj Urs. H. D, and R. V. S. Reddy, "Software Defined Radio : Advancement to Cognitive Radio and Basic challenges in Spectrum Sensing," pp. 166–169.
16. Chaitra C, Nataraj Urs H D, "Performance of SDR Transceiver Using Different Modulation Techniques" International Journal of Advanced Engineering Research and Science (IJAERS) , Vol-3, Issue-5 , May- 2016, ISSN: 2349-6495.