

# Design of a New Prototype of a MLI

Sangram Sekhar, Raseswari Pradhan, Smita Mohanty

**Abstract:** This paper presents design of a T-type multilevel inverters (MLI). Now-a-days, MLIs are usually require lesser number of elements like switches, capacitors as compared to conventional two-level inverters. Hence, MLIs are becoming very vital component in the area of power Electronics applications. Therefore, lots of research works are going on in this field for improvement in the topologies of MLIs. The main area of investigation in the design of MLIs are to maintain fixed level of voltage, less modulation index and switching losses. In this paper, a new type MLI such as a five-level based T-type MLI is designed and implemented. For that a prototype of the MLI is constructed. Then its performance is analyzed with appropriate simulation and experimental results. Again, its results are compared with that of another topology called five-level Cascaded H-Bridge type MLI. For better comparison, same type of modulation technique; Sinusoidal Pulse Width Modulation technique is used in both cases. The comparison is based on circuit complexity, modulation index and Total Harmonic Distortion (THD) of output voltage. From the analysis it is found that performance of the proposed MLI is better compared to that of the Cascaded H-Bridge type MLI.

**Keywords :** MLI, T-type, Cascaded H-Bridge, sinusoidal PWM.

## I. INTRODUCTION

Inverters are structures using which there is a possibility of getting steady alternative voltage, irrespective of type of load connected to it. They have gained a foothold in the field of AC motor drives, UPS and Renewable Energy Systems (RES) etc. In general, multilevel inverters (MLIs) have considerable advantages over two level inverters in getting more sinusoidal output voltage and better power quality. Five level Cascaded H-Bridge (CHB) MLI having 8 semiconductor switches reduces the harmonics in the output [3]. Multi State Switching Cell (MSSC) based five level T-type inverter gives five levels output voltage with higher order harmonics that could be easily filtered with R-load [4].

As the number of levels are increased, consequently THD will be decreased, which is actually desirable, but increasing the number of levels increase the complexity of circuit, thus needs more hardware, as a result complicated control circuit has to be designed. Choosing a MLI topology is a settlement between an output voltage closer to sinewave with lower THD and circuit complexity to maintain a balance between price and weight.

There are basically three types of multilevel inverters. These are Diode Clamped or Neutral Point Clamped MLI, Flying Capacitor multilevel inverters, Cascaded H-bridge

multilevel inverters. With recent researches, other MLIs are proposed having better power quality with low conduction losses and reduced volume and weight of magnetic components [1].

Proposed five level T-Type inverter is a Multi-State Switching Cell (MSSC) based Five-level T-type inverter having several advantages over five level Neutral Point Clamped (NPC)-MSSC topology. No clamped diodes are used in this topology, hence reduces the number of semiconductors used, thus reduces the cost of the converter. This topology solves the major problem of higher level MLI that is the circuit complexity. Thus the number of turned on semiconductors is less, representing a reduction in total losses during the operating intervals, thereupon, a better efficiency [4].

A comparative study of THD based on FFT analysis is done for both converters. Comparison is done considering same input voltage, same load connected and same LC filter in both converters. Section 2 confers about operation principle of the five-level CHB multilevel inverter and five-level T-type MLI. Conventional Sinusoidal Pulse Width modulation (SPWM) technique is employed for this T-type MLI. Section 3 consists of the results and discussion whereas Section 4 deals with the concluding remarks.

## II. MODEL DESCRIPTION

In this paper, two topologies of five-level type MLIs has been discussed such as five-level CHB and five-level T-type. In this section, model and working of these two MLIs are described one after another.

In this topology there are total eight controlled or regulated IGBT switches. Similar to CHB type, in this case also each switches have their respective intrinsic diodes connected in antiparallel manner with switches. However, one autotransformer with windings  $N_1$  and  $N_2$  (1:1) is used as interphase transformer as shown in Fig 3. Switches are named as  $S_1$ - $S_8$  and diodes are named as  $D_1$ - $D_8$ . In this MLI, there is an active bidirectional switch between the dc-link midpoint and the midpoint of each leg. This helps in making the output voltage level to five without even use of any filter as follows.

$$v_o = +Vin/4, +Vin/2, 0, -Vin/4, \text{ and } -Vin/2. \quad (1)$$

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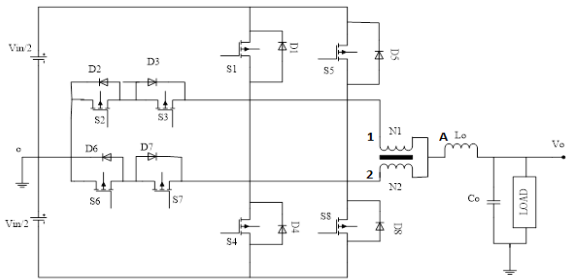


Fig. 4. Five level T-type MLI

The modulation technique used for the proposed converter is the conventional SPWM as shown in Fig. 5. The carrier signals are the drive signals for switches  $S_1$ - $S_8$  respectively. For SPWM, considering sinusoidal reference signal and comparing that with the respective triangular carrier signals suggested by colors red, purple, sky and green. Similarly, drive signals of switches  $S_i$  with  $i = 1, 2, 5$  and  $6$  are obtained respectively. Complementary of the drive signals for switches  $S_i$  with  $i = 1, 2, 5$  and  $6$  are the drive signals for switches  $S_i$  with  $i = 3, 4, 7$  and  $8$  respectively. According to the states of switches, output voltage appears in two manners: overlapping and non-overlapping.

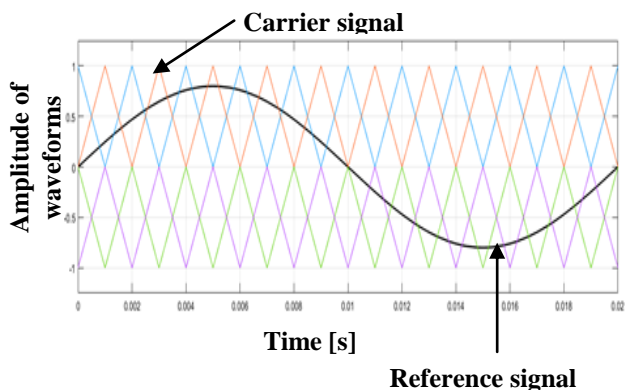


Fig. 5. SPWM modulation technique

When switches with  $i = 1$  and  $5$  are on concurrently during positive half cycle or  $i = 4$  and  $8$  are turned on together during negative half cycle of output voltage, we get output voltage in an overlapping manner. Output voltage in non-overlapping manner takes place during no simultaneous turn on of switches with  $i = 1$  and  $5$  or  $4$  and  $8$  during +ve or -ve half cycle of output voltage respectively shown in table 1. In this table, Overlapping and Non overlapping are taken as OL and NL. Further, the switching sequence of the T-type MLI is defined in table 2.

Table 1. Operation stages of five level T-type Inverter

Operation Positive Stages in half cycle				
Stage	mode	Switches $S_i$ ON	$V_{A0}$	Stage
1 <sup>st</sup>	OL,NL	5, 2, $D_3$	$+V_{in}/4$	1 <sup>st</sup>
2 <sup>nd</sup>	NL	2, $D_3$ , 6, $D_7$	0	2 <sup>nd</sup>
3 <sup>rd</sup>	OL,NL	1, 6, $D_7$	$+V_{in}/4$	3 <sup>rd</sup>
4 <sup>th</sup>	OL	1, $D_5$	$+V_{in}/2$	4 <sup>th</sup>
Operation Negative Stages in half cycle				
Stage	mode	Switches ON	$V_{A0}$	Stage
1 <sup>st</sup>	OL,NL	8, 3, $D_2$	$+V_{in}/4$	OL,NL
2 <sup>nd</sup>	NL	3, $D_2$ , 7, $D_6$	0	NL
3 <sup>rd</sup>	OL,NL	4, 7, $D_6$	$+V_{in}/4$	OL,NL
4 <sup>th</sup>	OL	$S_1$ , $D_5$	$+V_{in}/2$	4 <sup>th</sup>

Table 2. Switching Sequence of five level T-type Inverter

$S_i$ with $i =$	1	5	4	8	$V_{10}$	$V_{20}$	$V_{A0}$
Positive Semi cycle	0	1	0	0	0	$+V_{in}/2$	$+V_{in}/4$
	0	0	0	0	0	0	0
	1	0	0	0	$+V_{in}/2$	0	$+V_{in}/4$
	1	1	0	0	$+V_{in}/2$	$+V_{in}/2$	$+V_{in}/2$
Negative Semi cycle	0	0	0	1	0	$-V_{in}/2$	$-V_{in}/4$
	0	0	0	0	0	0	0
	0	0	1	0	$-V_{in}/2$	0	$-V_{in}/4$
	0	0	1	1	$-V_{in}/2$	$-V_{in}/2$	$-V_{in}/2$

### III. RESULTS AND DISCUSSION

#### A. Simulation Results

To analyze the working of the two topologies of MLIs as discussed in the previous section, their respective model has been designed in MATLAB/SIMULINK and corresponding results are compared. The parameters for each of the MLI models are defined in table 4. For better comparison between the efficiency of both the topologies, we have considered same input DC voltages, modulation index, loads and filters respectively for both cases. The number of controlled and uncontrolled switches are also made same and fixed. As shown in table 3, there is no auto transformer required for CHB topology.

Table 3. Parameters used in the design of the MLI topologies

Parameters	T-type MLI	CHB MLI
Input Voltage(DC)	$V_{in}/2 = 300V$	$E = 150V$
No. of controlled switches used	8	8
No. of uncontrolled switches used	8	8
Auto transformer used	Yes	No
Modulation Index	$M = 0.8$	$M = 0.8$
Resistive load	$150\Omega$	$150\Omega$
Filter Inductor	20mH	20mH
Filter capacitor	10 $\mu F$	10 $\mu F$

Input to the topology is shown in Fig. 6. Analysis is done from the result obtained from SIMULINK model of each topology as shown in Fig. 7. Comparing the output voltage waveforms of individual configuration as shown in Fig. 7 (a) and (b), it can be seen that waveform for CHB is looking distorted with more harmonic content compared to that of output voltage of T-type MLI.

To verify this finding, further FFT analysis has been done for both models and the results are shown in Fig 8 (a) and (b). From these figures, it can be seen that the THD for CHB is around 7.47% whereas for T-type it is limited to 4.03%. As it is already mentioned that, for both cases, same components have been used including LC filter. Even then, the THD for T-type is within allowable limit but that is not happening in CHB based MLI. Therefore, T-type MLI is found to be showing better performance than that of the CHB based MLI.

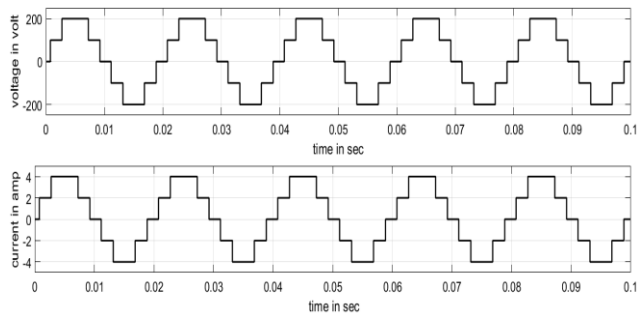
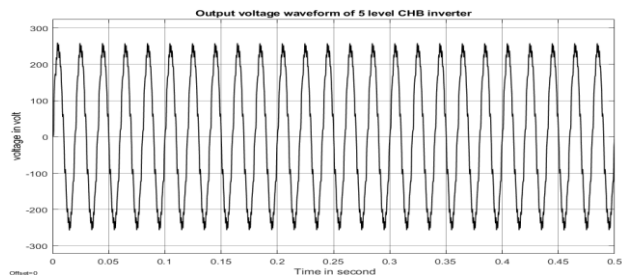
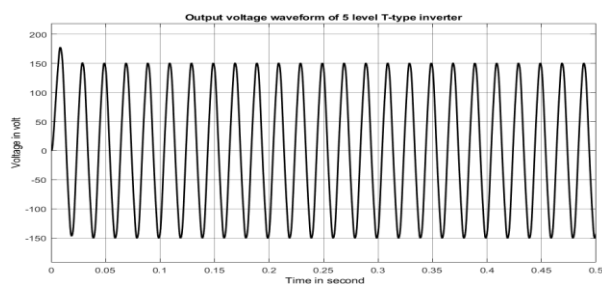


Fig. 6. Output Voltage and output current waveform for five-level Cascaded inverter under fault free condition

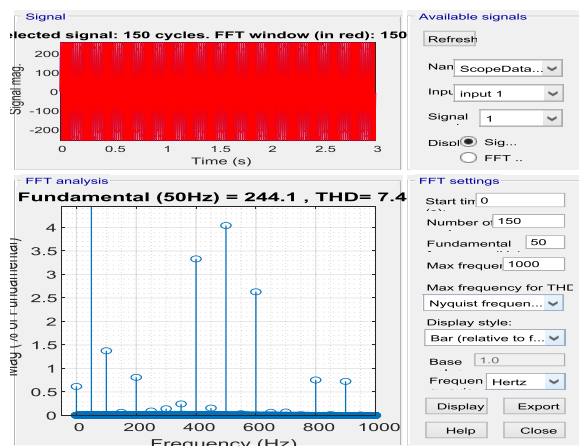


(a)

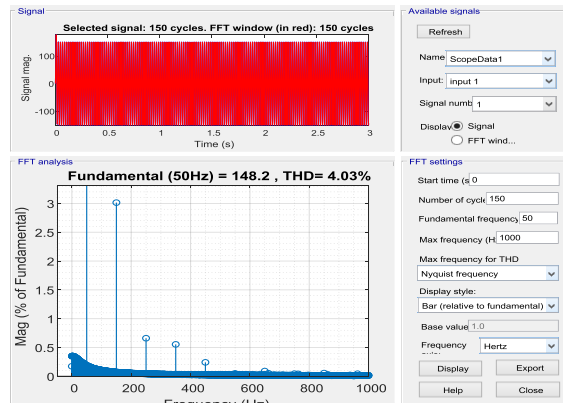


(b)

Fig. 7. Output voltage waveform of (a) five level CHB MLI and (b) five level T-type MLI



(a)



(b)

Fig. 8. THD analysis in case of (a) five level CHB inverter and (b) five level T-type inverter.

## B. Experimental Results

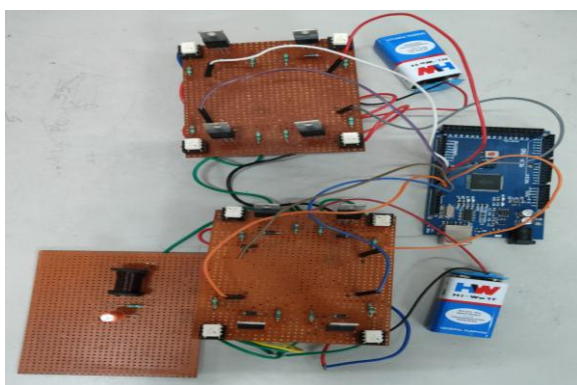
Prototype of five-level T-type MLI has been designed. The output voltage of proposed prototype is obtained for a resistive load with filter and without filter. For better comparison between two inverters same components are used for both. In table 4 parameters used for hardware setup of five-level CHB inverter has been listed. Total eight IRFZ44N MOSFETs switches are used. IRFZ44N is an N-channel enhancement mode type MOSFET. As electrons are the current carriers of an N-channel MOSFET, thus comparatively higher  $i_d$  is obtained. So N-channel is preferred over P-channel MOSFET. In table 4 parameters used for hardware setup of five-level CHB inverter has been listed. Total eight IRFZ44N MOSFETs switches are used. IRFZ44N is an N-channel enhancement mode type MOSFET. As electrons are the current carriers of an N-channel MOSFET, thus comparatively higher  $i_d$  is obtained. So N-channel is preferred over P-channel MOSFET. Hardware implementation of five-level CHB inverter is done. And output voltage of proposed prototype is obtained for a resistive load with filter and without filter. FFT analysis is done for THD calculation using DSO. Values of all parameters used in this prototype are given in Table 4.

TABLE 4. COMPONENTS REQUIRED FOR HARDWARE SETUP

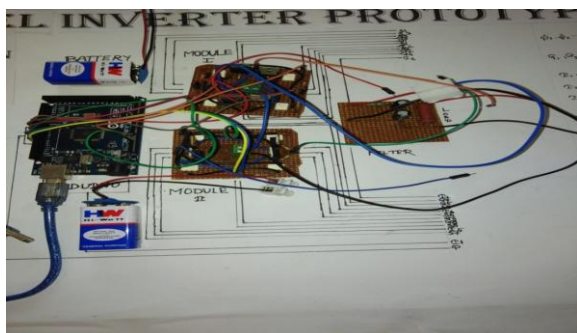
Sl.No.	Component name	Specification	Quantity
1	MOSFET	IRFZ44N 4	8
3	Opto-coupler	MCT2E	8
4	Battery	9V	3
5	Resistor	220 $\Omega$ , 10k $\Omega$	8,8
7	Capacitor	50 $\mu$ F	1
8	Inductor	3.5 mH	1
9	Microcontroller	Arduino mega	1



Fig. 9 (a) shows the experimental setup for five-level T-type inverter. In this experimental setup there is an Arduino microcontroller connected in 1st stage for controlling the gate signals. Fig. 9 (b) shows experimental setup for five-level CHB inverter. In this experimental setup there is an Arduino microcontroller connected in 1st stage for controlling the gate signals. After that through the jumper wires, two H-Bridge cells are placed with cascaded connection, where in each bridge four MOSFETs are connected which are controlled by the Arduino. 9V dc supply is given from battery to each H-Bridge. After that output of the inverter is fed to the filter circuit where two capacitors and a resistor are connected in parallel in series with the inductor. Inductor and capacitors are used for filtering purpose and output is obtained across the resistor.



(a)



(b)

Fig.9. Experimental setup for (a) five-level T-type inverter and (b) five level CHB inverter

Input voltage waveform of the experimental setup is shown in Fig. 10. Output voltage waveforms obtained from experimental setup across R load without filter and with filter are shown in the Fig. 11 (a) and (b) respectively. FFT analysis done in DSO for THD calculation of the T-type prototype is done in Fig. 12 (a) and (b).

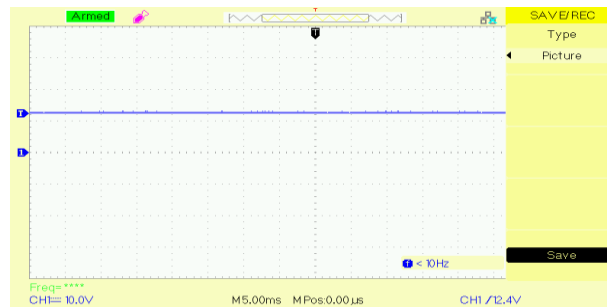
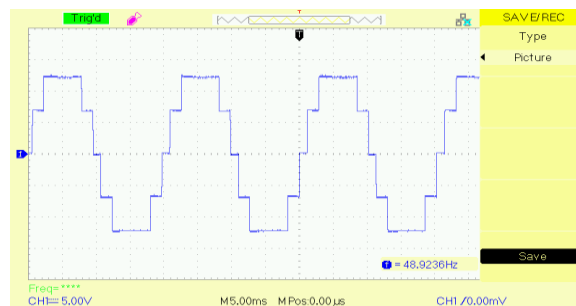
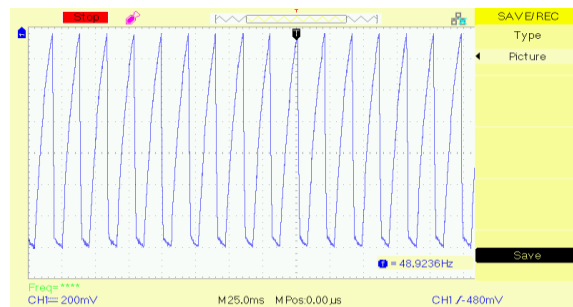


Fig. 10 Input voltage waveform of prototype for T-type MLI

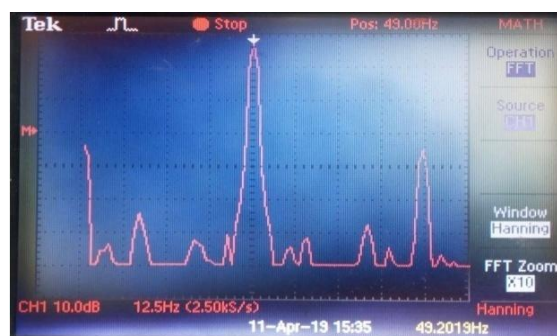


(a)

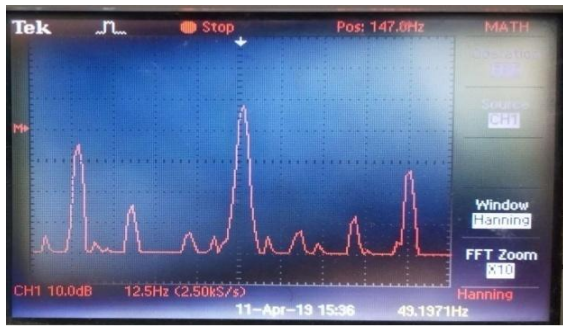


(b)

Fig. 11 (a) Output voltage waveform across R-load without filter (b) Output voltage waveform across R-load with filter for T-type MLI



(a)



(b)

Fig. 12 Magnitude of (a) third harmonic content and (b) Magnitude of fundamental component in DSO in case of T-type MLI

THD of the prototype output voltage is calculated with the help of digital oscilloscope as shown in Fig. 12 and is found to be 4.15%. From Fig. 7, THD obtained from simulated model of five-level CHB is 7.47%.

Same experimental analysis is also done with that of the five-level CHB prototype. Then, a comparative analysis between the both set of results has been done. The results of comparative study of simulation as well as experimental results for both the studied topologies have been given in table 5. For better comparison, same input voltages have been taken for both topologies such as 150V in case of simulation and 9V in case of experiment. From this table, it can be seen that, although the output voltage is less in case of T-type MLI, but the output current and THD are less compared to that of CHB-type MLI for both simulation and experimental studies.

TABLE 5. COMPARATIVE ANALYSIS OF RESULTS OBTAINED FROM CHB-TYPE AND T-TYPE FIVE LEVEL MLI

Parameters	CHB-Type Five-Level MLI		T-Type Five-Level MLI	
	Simulation Results	Experimental Results	Simulation Results	Experimental Results
Input Voltage (V)	150	9	150	9
Output Voltage (V)	300	16	200	7.5
Output Current (A)	4	$69 \times 10^{-3}$	2.9	$43 \times 10^{-3}$
Modulation index	0.8	-	0.8	-
THD (%)	7.47	8.58	4.03	4.15

#### IV. CONCLUSION

In this paper, a new topology of MLI has been designed. It is a T-type based five-level MLI. Its simulation and experimental performances are analyzed. The results are compared with that of the five-level CHB type MLI. In this analysis, comparison has been made in terms of their circuit complexities such as number of semiconductor switches and filter components etc. and THD of output voltages. For better comparison same type of components like input DC voltages, modulation index, loads and filters respectively have been considered both topologies. T-type MLI has only one extra auto transformer in its model. Although five level CHB is preferred over five level T-type inverter considering circuit complexity due to this extra auto transformer, but its output voltage waveform is more distorted. Also, the THD level for this case is more than that of the T-type MLI. Therefore, it is

verified that five level T-type multi-level inverter gives better performance in low voltage applications due to voltage stress obtained across the switches in comparison to that of the five level CHB based MLI.

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