Gate Diffusion Input Technique for Power Efficient Circuits and Its Applications

Priyanka Tyagi, S.K. Singh, Piyush Dua

Abstract*: - *In present scenario world become completely digital. In digital devices the speed and life of the battery is the biggest issue .To resolve these problems there are my techniques for design the devices. A low power design technique is Gate Diffusion input (GDI). This review has the study of GDI technique which is most recent research in low power designing field. In this study many paper were reviewed. The review has structure of THE GDI cell, modeling and application. This review also presented the comparison of GDI technique with other technique of designing. The purpose of the study to find out most recent research in field of GDI. From this study we find out this technique mostly used for digital circuits. This review provides the current state of research and future scopes in this field.

Index Terms:* *CMOS, CNTFET, GDI, MGDI, PDP.

I. INTRODUCTION

In present era the use of portable digital devices increased. for these devices the power and speed are the major component. the digital device which has speed and less power consumption is better. all the digital devices has the logic circuits. by improving the performance of the logic circuits devices can be improved. from last two decades CMOS technology was used to improve the performance of the devices [1]. but for the low power we have to modify the technique that is pass transistor logic(PTL). pass transistor logic is for nMOS. the function of PTL is the control signal applied on the gate of nMOS and the data signal on the source terminal of the nMOS transistor [2]. In literature PTL circuits are reviewed [2],[3], [5]-[8].the main advantages of PTL are 1. because of small node capacitance PTL designs has high speed. 2. due to small area the interconnection effect are low [8],[9]. 3. count of transistor is low so the power dissipation also low. PTL designs have two disadvantages that are 1. at lowest voltage level the operation is slow due to the drop in threshold across the single channel which reduced the current derive in PTL. 2. static power dissipation is higher at high level voltage. at high level voltage in inverter pMOS is not completely turned off[5]. number of PTL technique used to resolve these disadvantages mentioned above [6] 1. complementary pass transistor logic(CPL) : the main feature of the CPL is low power dissipation due to the low internal node swing. low swing at output inverter gates results static power consumption. to resolve the problem cross coupled transistors are used. 2. transmission gate CMOS (tg): less number of complementary transistors are used to realize complex logics. by using the nMOS and pMOS it solve the low logic level swing problem [2]. 3. double pass-transistor logic (dpl): to reduce the dc power and for full swing operation complementary transistors were used. restoration circuit is not used due to the complementary logic. pMOS transistor increase the area of the logic circuit [7]. for resolving all the problems the GDI technique introduced. GDI can implement the complex logic function by using two transistors. this technique provides high speed, less delay and power dissipation.

II. GATE DIFFUSION INPUT TECHNIQUE

ArkaidyMorgenshtein et al.GDI (Gate diffusion input) A new technique for low power designing introduced in this paper. This technique used only two transistors that is NMOS and PMOS for designing digital logic designs such as gates, adders etc. This technique reduces the number of transistor in logic design which affects the size of the devices. It reduces the size of digital devices and reduces the power dissipation. GDI techniques improve the static power characteristics and using small cell library for design top down approach of the circuit [12].

A. GDI Cell Structure

GDI primitive cell is very similar to the CMOS logic. GDI has the 3 terminals. Gate terminal G, P node for the PMOS and N node for the NMOS. CMOS and GDI had the difference in structure that the bulk of the PMOS and NMOS connected to their diffusions. Gate is the common terminal for the NMOS and PMOS. The body terminal connected to the diffusions to minimize the body effect of the logic Figure 1 shows the basic GDIcell.

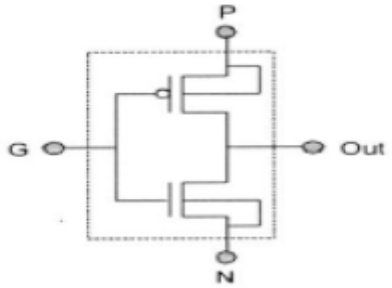

Fig1 : Basic GDI of Cell

Divya soni et al described that the sub threshold leakage current and the gate leakage current both decreased in the GDI technique. GDI is not good when fabricated in the p well progression. GDI cell fabricate on the twin tub process or the SOI (silicon on insulator)[10].

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The threshold voltage is increased when substrate attached to the drain and body effect is destroyed when the substrate is attached to source [11].

B. Operational Analysis Of GDI

AS we discussed earlier in review that PTL logics had the problem of the low swing due to threshold voltage drop in the single channel. To resolve the problem GDI introduced. Low swing occurs at the lowest possible logic. To understand the operation of low swing logic P node is B input, Gate is A, output is the function F1. N node connected to the ground. The low swing condition is A=0, B=0, In this condition F1 =Vtp due to poor high to low transition of PMOS. A=1, B=0, In this condition F1=Vtn A=1,B=1, F1=0, work as simple inverter A=0, B=1. F1=0, work as simple inverter The above conditions shows that when the B= VDD=1 the GDI cell was inverter and has full voltage swings [10].

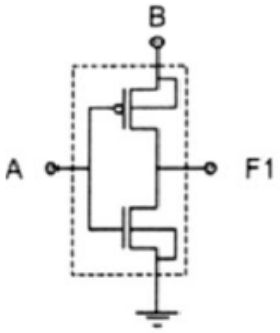

Fig 2 : Input Logic States

C. Applications of GDI

ArkaidyMorgenshtein et al. GDI technique was applied on different asynchronous circuits. These asynchronous GDI circuits compared with the traditional CMOS asynchronous designs. In comparison of typical CMOS designs GDI asynchronous design are smaller in size. The speed of GDI designs was30% better than the typical CMOS designs. The power consumption of GDI circuits was better than CMOS they consume 85% less power as compare to the CMOS. GDI circuits had less power delay product. It required one third delay and half area for the same power consuming circuit in the CMOS design. GDI also had the property to enhance the hazard tolerance [13]. ArkaidyMorgenshtein et al. (2004) Flip flops are the basic unit of the storage. Using GDI basic memory element D-FF was implemented. [1]. Due the GDI designing that is based on the two transistors the gate area of the device was reduced as compare to the other D-FF designs. Performance was better than the CMOS and other D FF logic designs. Proposed design had 45% PDP (power delay product) and had area and size reduction. All these characteristics enhance the performance and speed of the D FF [14]. Massimo Alioto et al.(2007) Adders are the basic elements in any digital circuit. In this paper 5 different style methods that is mixed topology [13] . The technique span from 90nm to .35 um. Mixed style designing was better over single style and also improve the property of down scaling [15]. Adarsh Kumar Agarwal et al. (2009) this paper focused on propagation when the circuit implemented using the long inverter chain. GDI Full adder implemented using mixed technology [1]. This GDI adder followed by inverters in the long full adder chain. This implementation resolve the problem of signal degradation due the propagation [16]. R. Uma (2011) Self resetting logic was used to design 4 bit adder. Dynamic logic was compared with SRL at gate level and performance level. Dynamic gates had issue of clock skew and delay with CAD tools. When they used clock distribution and routing in dynamic logics. The main disadvantage of SRL was the silicon area occupy by the logic [17].

TABLE 1. INPUT logic versus OUTPUT SWING

A	B	F1	Operation
0	0	Vtp	Pmos trans gate
0	1	1	CMOS inverter
1	0	Vtn	NMOS trans Gate
1	1	0	CMOS inverter

Kunal et al. Design of comparator and multiplier was obtained using GDI. The proposed designs compare with existing TG and N-PG techniques. The result shows 45% reduction in PDP. Combinational logics synthesized and realized using single cell library in GDI technique [18]. Mrs. K.Kalaiselvi et al. proposed the Self resetting adder circuit. In proposed design adder circuit was modified and the number of transistors reduced. The purpose of the design to implement high speed adder that used to implement the fast processors. The adder was designed by using 120nm CMOS technology [19]. K.Nehru et al.This presented 16 bit counter using GDI technique. As we know counter are implemented using master slave Flip flops. This implementation used Flip flop. Using basic GDI primitive cell D FF was implemented [1]. CMOS and GDI based counter analyses at different voltage levels. The results showed 30% reduction in transistor count and 20% reduction in PDP [20]. Mohan Shoba et al. proposed the design of full adder using full swing XOR, OR and AND gates. Full swing gates resolve the problem of the threshold voltage .The design use the 45nm technology. The proposed design also improve the current driving capability and consume less power as compare to the other design [21]. Sheel et al.1 bit full adder implemented using GDI technique and the performance compare with the conventional adder. Conventional adder that is CMOS adder. Comparison done for the number of transistors , power dissipation,delay , area and speed of the circuit. The power dissipation reduced 25% and delay reduced 50% . These parameters made full adder more effective and efficient [22]. P.A Irfan et al. Multiplication is an arithmetic operation which the very important in the signal processing application. In DSP the multiplication has the key unit. Multipliers used in Fast Fourier transform and convolution and other operation. Vedic multiplier designed using the GDI technique which improves the speed and performance of the multipliers. Vedic multiplier based on the Vedic sutra that means multiply done vertically. In processors multiplier is the main parameter to introduce the delay. By using GDI to design multiplier delay and power dissipation was reduced [23]. R. Uma et al. GDI SRL used to design the low power adder.

GDI implementation in pull down tree eliminates the overlapping of conductance between N M O S a n d P M OS device [6]. This implementation provides high output voltage and power dissipation by reducing the short circuit current [24]. Munesh Tirpathi et al.this paper presented the Manchester Encoder. The encoder had the property to work in high frequency without any additional circuit. For this structure author replaced the adders, DFF and logic Gates with GDI DFF and GDI XOR gate [12,14]. GDI based encoder has less no of transistors and less complex circuit. The performance is also better with GDI technique without changing its properties [25]. Nagalaxshmi et al. In this paper 4 bit ALU design using GDI presented. ALU design had 4:1 MUX , 2:1 MUX, Full adder which had previously designed using GDI[1,7]. This GDI block of MUX and adder used to design ALU. GDI ALU had the better delay and power consumption parameter [26]. N.Suresh et al.The low power full adder designed using GDI MUX.GDI MUX design reduce the size and count of the transistors. In this design the transistor count was 12T. This improve the speed and reduce the power dissipation [27].

III. MATHMODIFIED GATE DIFFUSION INPUT (MGDI)

A. Introduction

P. Balasubramanian et al .introduced the new technique that was much better than the GDI. Modified GDI cell was introduced in this paper. MGDI cell similar to the GDI CELL in structure the difference was that the bulk of the NMOS constantly fixed to the GND and bulk of the PMOS fixed to the VDD. The MGDI technique resolve the problem to threshold voltage in GDI technique, MGDI improves the area, speed and Power dissipation parameters as compared to the GDI [28].

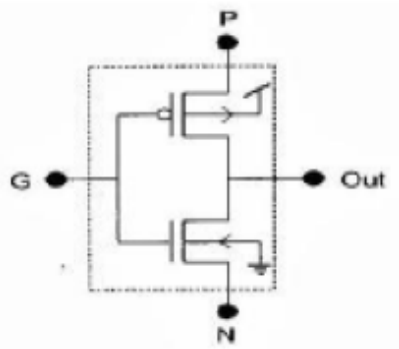

Fig 2 : MGDI Cell

B. Applications Of MGDI

R. Uma et al. Modified-GDI is introduced. MGDI is the modified primitive cell which had the many advantages over the basic GDI primitive cell . Twin well CMOS and the SOI(silicon on insulators) process was used for GDI fabrication. MGDI fabrication is less complex and expensive in comparison of GDI primitive cell. Performance comparison of 5 different models of full adder using MGDI and GDI. The performance, speed and count of transistor of MGDI primitive cell was better than the GDI cell, CMOS and PTL logics. Power dissipation, delay and PDP are less in MGDI designs. The transistor count in MGDI had 16T, 14T, 12T, 10T, 8T but GDI had 18T, 16T, 14T, 12T, 10T respectively. The transistor counts in CMOS implementation almost double as compared to the MGDI implementation [29]. R. Uma et al. In this paper SRL block replaced by the MGDI block. In the traditional CMOS structure PMOS connected to the supply and NMOS connected to the GND. This arrangement provides a low impedance path between the supply(VDD) and GND. The low impedance path resolve by using the MGDI block in place of NMOS . The combination of the SRL and MGDI low power delay product and high speed [30]. Pankaj verma et al .described the advantages of the MGDI that the leakage current sub threshold and the gate leakage current problems resolve in the MGDI cell. Due to reduction in short circuit current this technology used in the repeaters and synthesizers implementation. The DC transient analysis was also better as compared to the GDI and CMOS [31]. Krishnendu Dhar et al. designed FULL ADDER using MGDI AND MVT technique. Mixed threshold technique with MGDI used to improve the performance of adder. The transistors count also less in the MGDI. The no of transistors are 10 in this technique and delay, power consumption were less as compared to the GDI [32]. Krishnendu Dhar et al. this paper presented the clock sequential circuit using MGDI technique. The paper proposed Clocked NOR based JK Flip flop. The purpose to implement the JK flips flop because it is the universal flip flop. From this other flip flop can also designed. JK flip flop resolve the condition of not defined in the SR flip flop [33]. Deepali Koppad et al. presented a full wing full adder using MGDI cell. MGDI used to get full swing logic 0 and logic 1 . The performance of the MGDI full adder compared with other logic style by using VIRTUOSO based on 45 nm technology [34].

IV. CARBON NANOTUBE FIELD EFFECT TRANSISTOR (CNTFET)

P.Parkash et al.In today electronic industry the semiconductor are the most prominent component. All the digital devices are depends on the semiconductor. In 90's the CMOS technology was used to design the devices. Because the CMOS has the less area covered and less power dissipation. NOW the CNTFET used in place of MOSFET. IN CNTFET silicon was replaced by the carbon nanotube [35]. Mehrabani YS et al. was explained that MOSFETs are replaced by the CNTFETs to improve the performance of the devices. The electrical properties of the carbon nanotubes are very efficient as compared to the silicon .The carrier mobility is greater in Carbon nanotube in comparison of the silicon. CNTFET are the most promising component in the nanoelectronics [36]. Soheli Farhana et al. proposed different logic gates based on high frequency CNTFET. The NOR, NAND and OR logics are realized using high frequency CNTFET. These devices had the high frequency response and the sharp VTC .CNTFET could be used to design any digital logic with high speed and less power dissipation [38].

Rajendra Prasad Somineni et al. introduced full adder using CNTFET. CNTFET based design improve the performance of the CMOS based adder. CNTFET used the stacking for p type transistors that help to retain the data in standby mode. The power dissipation was less in the CNTFET design [39].

V. MGDI CNTFET

A. Introduction

CNTFET MGDI cell has the same structure as the CMOS MGDI cell. The difference is that it used CNTFET in place of the CMOS. The silicon channel is replaced by the carbon nano tubes. Due to the carbon nanotube current conducting properties the CNTFET is used for the high speed applications [39].

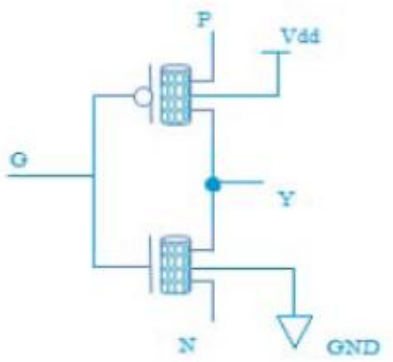

Fig 3 : CNTFET MGDI CELL

B. Applications of CNTFET MGDI

P.Reena et al.This paper introduced union of GDI technique with the high performance CNTFET. The results of this combination were less complexity in logic circuits, high performance, less power dissipation. In this structure the N-CNTFET and PCNTFET fabricated on the same substrate. GDI technique had no need of twin tub process for fabrication. Basic logic expression were implemented using GDI with CNTFET [40]. Nazir Ahmed et al.Nanotechnology combine with the GDI to analysis the performance of circuits . 12 T CNTFET adder compared with CNTFET adder with GDI technique. Both circuit had reduced the power consumption due to the short current. GDI CNTFET had better power consumption and Power Delay Product (PDP) . One bit Full Adder cell based on the CNTFET had the characteristics better than its CMOS implementation. Performance, delay and gate area was much less than the conventional CMOS adder. CNTFET adder better than CMOS adder and GDI CNTFET was much better than CNTFET adder [41]. EbrahimAbiri et al.This paper presented 8T –SRAM based on MGDI technique. SRAM was implemented with carbon nanotube field effect transistor technology using Stack forcing. In this paper 8T SRAM was presented for reading and writing blocks with array structure. The simulation is done using HSPICE at 32 nm and PDP for the implementation was 18% less for reading cycle and 36% for writing cycle [42]. Chandrashekar et al. A new design technique used in the paper CNTFET. CMOS replaced by CNTFET. CNTFET overcomes the CMOS drawbacks. CNTFET merged with the GDI technique to implement the full adder. CNTFET Full adder using GDI had better power and delay parameters. The transistor count was also less in the design. In place of transistor we use carbon nanotubes [43]. Priya et al. presented the full adder with GDI and CNTFET. In this paper CNTFET 32 nm technology was used for the implementation. The XOR was designed with 4 transistor and used for sum and carry output. The design was compared to the CMOS GDI and had the less power and energy consumption [44].

Ebrahim arbari et al. introduced Dual modulus frequency prescaler that is main block of the frequency synthesizer circuit. Frequency synthesizer is the main component in the communication application. He proposed the CNTFET based N/[N+1] DMFP using MGDI technique. CNTFET based circuit had effective delay and power delay product. The presented design was able to perform with frequency range with high figure of merit. The proposed design had the larger noise immunity [45].

VI. CONCLUSION

As the technologies are going to advance new technique of system designing are introduce. The paper reviewed the GDI technique and its various application .All the digital application are designed using GDI has the low power and less count of the transistors. The designs with GDI had the less PDP in comparison of CMOS. But GDI had the problem of threshold leakage. Then MGDI technique introduced which can eliminate the problem of the GDI. MGDI was the modified version of the GDI technique .The performance of MGDI is better than the GDI in terms of power, delay and count of the transistors. Many applications were based on the full adder because adder is the key component for many other devices and the processor units. Then the paper reviewed the high performance CNTFET circuits. CNTFET has the many advantages over the CMOS. Then to improve the technique the CNTFET combine with the MGDI technique which can improve the device many times. CNTFET with GDI devices has the less transistors count , high speed and the power delay product is less due to the carbon nanotubes characteristics. There are only few applications using CNTFET with GDI. In future many other devices and applications can be modified for high speed and low power dissipation using CNTFET with MGDI.

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