A Metaheuristic Algorithm for VLSI Floorplanning Problem

S. Venkatraman, M. Sundhararajan

Abstract*: Floorplanning plays an important role within the physical design method of very large Scale Integrated (VLSI) chips. It's a necessary design step to estimate the chip area before the optimized placement of digital blocks and their interconnections. Since VLSI floorplanning is an NP-hard problem, several improvement techniques were adopted to find optimal solution. In this paper, a hybrid algorithm which is genetic algorithm combined with music-inspired Harmony Search (HS) algorithm is employed for the fixed die outline constrained floorplanning, with the ultimate aim of reducing the full chip area. Initially, B*-tree is employed to come up with the first floorplan for the given rectangular hard modules and so Harmony Search algorithm is applied in any stages in genetic algorithm to get an optimum solution for the economical floorplan. The experimental results of the HGA algorithm are obtained for the MCNC benchmark circuits.

Keywords: Genetic algorithm (GA), Harmony Search algorithm (HAS), Hybrid Genetic algorithm (HGA), slicing floorplan

I. INTRODUCTION

Floorplanning might be a basic stride, since it sets up the base work for a legit format. Nonetheless, it's computationally very burdensome off and on again the undertaking of floorplanning is done by a plan build, rather than a computer aided design tool. The strategy for determinant square shapes and positions with space minimization goal and proportion request is said as Floorplanning [1]. A standard procedure for pieces floorplanning is to work out, inside the first part, the relative area of the squares to each unique upheld association cost criteria. Inside the second step, square size is performed with the objective of limiting the general chip space and along these lines the area of each piece is finished [1]. All through floorplanning, every area and introduction of a gathering of rectangular pieces zone unit set indicated no squares cover. The interconnect is set by the include of the lengths of the considerable number of nets. Usually half perimeter inter connect length (HPICL) is employed as an estimate of the whole inter connect length. The slicing floorplan is solely explains that the kids of all composite cells may be obtained by bisecting the cell horizontal or vertical direction fig 1, the floorplan is named slicing floorplan.

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Within a slicing floorplan a composite cell is shaped by consolidating its youth's horizontal or vertical (putting ensuing to each other from left to right or stacking the on prime of each other).A regular approach to speak to a slicing floorplan is by implies that of a slicing tree [2]. The composite cell is nothing however cell that territory unit made of leaf cells zone unit known as composite cells. The leaf is that the least level cells region unit known as leaf cells.

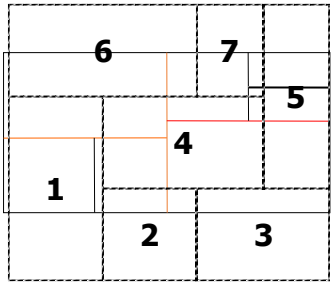


Figure 1: Non-Slicing Floorplan

The non-slicing floorplan is exclusively clarifies that the children of every single composite cell can't be acquired by bisecting the cell horizontal or vertical direction fig 2, the floorplan is named non-slicing floorplan. Not all floorplans range unit slicing for example, inside the wheel or winding floorplan. Here the children of the given cell can't be acquired by division. The composite cell must be made out of at least five cells in order to not cut [2].

Independent of the equipment usage elective, enhancement is required at all the outline levels to get the easiest execution of the objective application. A few of the floorplanning advancement issues inside the plan stages are NP-complete issues. Unsatisfiable heuristics is usual rapidly secure a response for the NP-complete issues. In any case, unsatisfiable heuristics don't claim any system to escape out of locally best arrangements. Because of this reason, they'll end in arrangements of frightfully poor quality as they'll stall in local optima. Stochastic streamlining techniques like simulated annealing, Molecule swarm improvement and genetic algorithms make utilization of random moves to escape out of local optima. Specifically time, the random streamlining techniques ordinarily have the ability to accomplish the internationally best determination [3].

Despite the fact that the need for a legit worldwide streamlining strategy inside the equipment style technique is self-evident, the criticality of the change procedures can fluctuate with the arranging levels and furthermore the type of equipment usage. In VLSI ASIC design, the circuit combination and physical design arranges square measure the chief significant stages as they assume a major part in getting the best framework usage.

In FPGA based generally equipment design, design adaptability and change openings square measure limited contrasted with full custom ASICs on the grounds that the arrangement of rationale cells and interconnections is mounted. Henceforth, the FPGA style cycle is greatly touchy to the abnormal state model of the framework. In this way, producing partner degree right and brief behavioral model of the framework is critical in FPGA based for the most part equipment style. This re-repeats the necessity for rich IP modules which will be re-utilized by the designer all through abnormal state displaying. The accessibility of an IP module library lessens the many-sided quality of abnormal state displaying. With whole frameworks being implemented on consistent FPGA, a few FPGA styles require irregular change centers as a piece of the machine itself [4] [5]. Since the necessities of the applications square measure far reaching, a tough stochastic change strategy that is direct to actualize in equipment is required.

A genetic algorithm (GA) is a stochastic improvement method demonstrated on the hypothesis of advancement in nature. It has been effectively utilized for a wide assortment of problems including NP-complete problems, for example, the Voyaging Sales representative problem [6], continuous problems, for example, reconfiguration of evolvable equipment [6] and other enhancement problems that have complex imperatives. Genetic algorithms are anything but difficult to execute in programming and equipment. They can likewise be effectively adjusted to a wide assortment of problems. They can make utilization of existing learning about a problem by fusing fruitful existing administrators into their enhancement structure. They are a multi-specialist advancement method and consequently can be effectively adjusted for multi-target improvement.

The Harmony Search (HS) technique could be a metaheuristic change algorithmic program proposed in [17] [19]. It emulates a melodic act of spontaneity strategy inside which the artists in a symphony/band attempt and understand a perfect condition of amicability through melodic act of spontaneities. When performers form harmonies, they commonly endeavor fluctuated potential combos of the music contributes put away their memory. This algorithmic program was intended to impersonate the approach a performer utilizes memory and subsequently the past encounters to lead his/her to the note that prompts the principal satisfying agreement once strive close by the inverse artists. HS is easy to execute and may effectively be connected to determine for all intents and purposes any disadvantage that might be planned on the grounds that the abatement or amplification of a goal performs. This sort of financial investigate for a perfect condition of harmonies is said to the method of finding the ideal or close ideal answers for a tangle. When determination a chose issue, each performer is considered as a call variable. In this way, the correct concordance implies that the global or nearly optimal solutions.

I. Problem Description

The floorplanning issue considered in this review is that the issue of putting a gathering of circuit squares on a semiconductor chip with the objective of limiting chip size and aggregate wire length. Here, the chip size is characterized on the grounds that the space of the littlest VLSI floorplanning might be an all-around considered issue that a scope of enhancement strategies are connected together with simulated annealing (SA), numerical programming, and genetic algorithms [7]. Early floorplanners disallowed space improvement alone. However with the entry of the profound sub-micron administration, floorplanners moved their concentration to improving interconnect. Be that as it may if interconnect is that the exclusively target to be streamlined, the resulting floorplan can have a lot of unused space. Thus, some floorplanners attempted to enhance each space and interconnect. Inside the single standardized weighted total (SNWS) way to deal with multi-target advancement, simultaneous enhancement of two goals infers that the streamlining agent utilizes measure up to weights to duplicate the standardized destinations before adding them along to get the one standardized weighted whole. Established (framework free) floorplanners bolstered Simulated annealing [8] utilize the one standardized weighted total way to deal with streamline the two targets, particularly space and aggregate interconnect. These SA-based floorplanners take issue exclusively inside the information structure, Arrangement combine [8] or transitive Conclusion Chart, used to speak to the floorplans. Such floorplanners kind one scalar target perform abuse the two standardized destinations and furthermore the client sketched out weights for each goal as appeared in Condition underneath.

Genetic algorithms were initially made arrangements for circuit position by Cohoon and Paris. The essential hereditary lead for floorplanning was arranged by Cohoon et al and utilized Standardized Clean expressions to speak to floorplans. Afterward, a few diverse hereditary floorplanners were arranged that created novel crossover methods for different floorplan portrayal plans. Hatta et al proposed the essential hereditary floorplanner bolstered the Grouping pair portrayal that improved floorplan space. Their hereditary floorplanner utilized two new crossover administrators, particularly One-point partially Coordinated Crossover (OPX) and Uniform partially Coordinated Crossover (UPX) [11]. Hatta et al consolidated the notable partially Coordinated Crossover (implied for stage based chromosomes) with two parallel crossover administrators to define two new crossover administrators (OPX and UPX) that would deal with the Succession combine floorplan portrayal. OPX might be a blend of the one reason crossover and thusly the part Coordinated Crossover. On the inverse hand, UPX might be a mix of the uniform crossover and hence the partially Coordinated Crossover administrators.

The proposed floorplanner works explicitly on correspondent change of space and interconnect utilizing the particular Non-commanded Sorting based Hereditary run the show. It's to be noticed that the anticipated floorplanner are regularly basically reached out to perform affixed diagram floorplanning by joining a punishment perform or by utilizing a changed wellness task.

II. Proposed Method

Representation of Floorplan

Polish notation is used to model Cutting Floorplans. The double Tree is used to state a polish notation, E= e1 e2...e2n-1 where ei € {1, 2... n, H+, V-}. Here, each number addresses a module and H+, V-addresses an even and vertical cut independently in the cutting floorplan.

The Perfect expression is the postfix asking for of a matched tree, which can be gotten from the post-orchestrate traversal on a binary tree. Clean expression length is 2n1, where n – is number of modules.

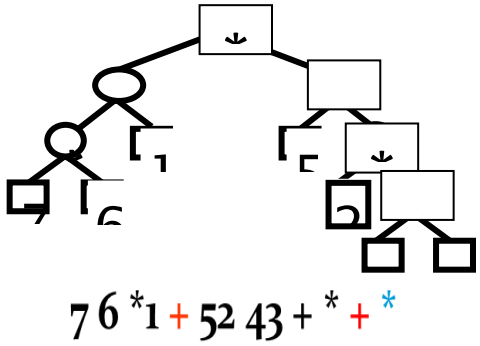
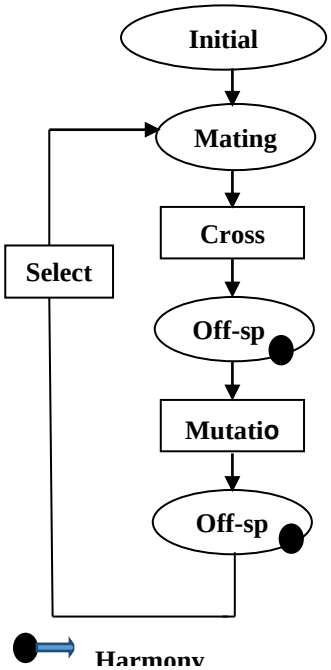


Figure 3: Normalized Polish Expression

The proposed blend genetic floorplanner starts with a hidden masses of every which way made by clean expression and presentation vectors with a readiness set of benchmark circuits from both the MCNC benchmark circuits suites were directed to filter out the qualities for the HGA parameters that offer the best results maintained the delayed consequences of the test studies, Condition 1 has been resolved to see the GA people measure reinforced the issue gauge, i.e., extent of modules (n). This condition was then associated with measure the people by the proposed floorplanner for each one of the benchmarks. To the best of the Maker's data, this is routinely the basic genetic floorplanner that varies the people measure as per the measure of modules (n) show inside the benchmark circuit.



Population size = 10*n ---------- (ii)

Figure 4: Proposed Method

The proposed floorplanner sorts the entire populace into changed non-control levels regarding space and total interconnect toward the begin of every era. Every one of the general population inside the present populace are apportioned a non-mastery rank extending from zero. The fittest people have the littlest sum non-control positions.

Best Individuals

The quantity of first class people inside the present populace of the anticipated GA fluctuates with each era. Every one of the people with extremely shabby no mastery rank (zero) sort this arrangement of first class people. These people don't appear to be liable to transformation. Along these lines, people containing hereditary information contributory to diminished space or interconnect will be safeguarded for the more drawn out term eras.

Mating Pool Selection

The size of this pool is prepared to a large portion of the populace estimate as proposed in. On the off chance that the amount of tip top people is greater than this size, then the best people with the most critical swarming separation range unit picked to make the mating pool to affirm that a different arrangement of individual's territory unit kept up inside the populace.

Parent Determination

The proposed GA utilizes swarmed competition determination to choose the two guardians for hybrid from the mating pool of people. In competition determination, a gathering of parent candidates is chosen randomly from the mating pool. A competition is played between these candidate people to decide the fittest two people of the gathering.

Crossover

The crossover operator is utilized by hereditary calculations to blend sensible characteristics from the guardians to make to a great degree work posterity. A decent hybrid administrator ought to moreover ensure that the posterity doesn't nearly coordinate either parent. These properties ensure that the hybrid administrator investigates totally unique promising territories inside the determination range. The crossover rate (cx_rate) limits the amount of hybrid performed in any era

Mutation

The three mutation operators employed in the proposed floorplanner are described below

- Complement a chain (vertical-horizontal).
- Exchange a sub tree and a leaf.
- Rotate a module (M) or sub floorplan.

III. Harmony Search Algorithm

The main control parameters of Harmony Search algorithm (HS) are harmony Memory (HM), Harmony Memory Size (HMS), Harmony Memory Considering Rate (HMCR), Pitch Adjusting Rate (PAR), and Bandwidth (BW). Here, HM is a memory location where all the solution vectors are stored; HMCR and PAR are parameters that are used to improve the solution vector.

It's one amongst the algorithm's parameters that have to be set manually. Memory is structured as a matrix with every row represents an answer vector, and also the final column represents the vector's fitness value. Within the HS formula, $\hat{H}$ represents the harmony and $f(\hat{H})$ denotes the melody of harmony $\hat{H}$. during an N-dimensional problem, the HM would be described as:

$$\begin{matrix} \hat{H}_1^1 & \hat{H}_1^2 & \hat{H}_1^3 \cdots & \hat{H}_1^n & | W_1 \\ \hat{H}_2^1 & \hat{H}_2^2 & \hat{H}_2^3 \cdots & \hat{H}_2^n & | W_2 \\ \vdots & \vdots & \vdots \cdots & \vdots & | \vdots \\ \hat{H}_{HMS}^1 & \hat{H}_{HMS}^2 & \hat{H}_{HMS}^3 \ldots & \hat{H}_{HMS}^n & | W_2 \end{matrix}$$

The HMCR is one in all the HS parameters that has to be manually chosen. A random number is generated for every call variable. If it's less than the HMCR, the memory is taken into consideration; else, a price is at random chosen from the vary of potential values for that dimension. The Pitch Adjustment Rate (PAR) is set throughout initialization, and it controls the quantity of pitch adjustment done once memory thought is employed. Another random number is generated. If it's smaller than the PAR, the makeshift value is pitch adjusted using (1):

$$\hat{H}new = \hat{H}new + Random\ ().BW \text{ --- (iii)}$$

Ĥnew is that the new pitch-adjusted value, is that the previous value chosen exploitation memory thought, random () could be a random value between −1 and 1, and BW is that the bandwidth parameter

If the new improvisation includes a higher fitness, it replaces the vector with all-time low fitness. This method of improvisation and update continues iteratively till some stopping criterion is consummated, or the utmost variety of iterations is reached.

Harmony Selection

The values of a style variable are often chosen from the values keep in HM with likelihood HMCR. It are often more adjusted by moving to a neighbor value of a specific value from the HM with a likelihood of PAR, or, it can be chosen at random from the set of all candidate values without considering the stored values in HM, with the chance of (1 - HMCR).

Update Harmony Memory

If the New Harmony vector is better than the worst vector, based on the objective value and/or constraint violation, the new vector will replace the worst one.

Termination criterion

HS algorithm is terminated if the stopping criterion (maximum number of improvisations) has been met.

Fitness function

The main objective of the floorplanning is to minimize the total chip area. The formula for calculating the total area of the chip that contains 'i' modules is given in (2):

In every iteration, the priority of the answer vector is graded

$$Area = \sum_{i=1}^{n} (L(i) * W(i))$$

consistent with the fitness value calculated using the fitness function. By maximizing or minimizing the fitness values in every generation, the global optimum value may well be found. The fitness operates for the proposed method is given in (5).

Here, φ and ω values are treated as the weighting factors. In

$$f(X) = \varphi * Area$$

this proposed work φ value is taken as 1 and ω value is taken as 0.25.

Benchmark Circuit	apte	ami 33	ami 49	Xerox	hp
B-tree	46.92	1.27	2.98	19.83	8.95
Simulated Annealing	48.47	1.23	2.7	20.42	9.48
Hybrid Simulated annealing	48.12	1.25	2.6	21.86	9.43
PSO	47.44	1.24	2.4	20.2	9.6
Harmony Search	46.7	1.28	2.5	20.64	9.01
Hybrid GA (Proposed method)	47.01	1.19	2.8	20.14	9.13

Table 1: Comparison of the proposed work with existing methods

IV. Result & Conclusion

The proposed genetic floorplanner combined with Harmony search algorithm was applied using C++ and assembled the experiments; the proposed genetic floorplanner was run with a crossover rate of 1.0 and mutation rate of 0.1 and for Harmony search algorithm the used parameters are as HMCR value 0.9, HMS value may be set as 50,100,150,200, The number of iteration will be 1000, PAR value set by 0.3 and band width values defined as 0.01.These GA and HAS parameter values were empirically determined all the experiments were run on a Linux machine with a 3.16GHz Intel Core i3 processor and 2GB RAM.

VLSI Floorplanning has reworded in to a multi-objective improvement problem with the recent advances in integration technology. Genetic algorithms combined with Harmony search algorithm are extensively employed in entirely dissimilar forms to resolve many more VLSI floorplanning issues. In this paper the hybridized algorithm for multi-objective floorplanner achieves global solution for the MCNC benchmark circuits as compared to alternative floorplanners that perform synchronal improvement of space. Thus, genetic algorithms combined with HAS are often used effectively for multi-objective improvement in VLSI floorplanning problems

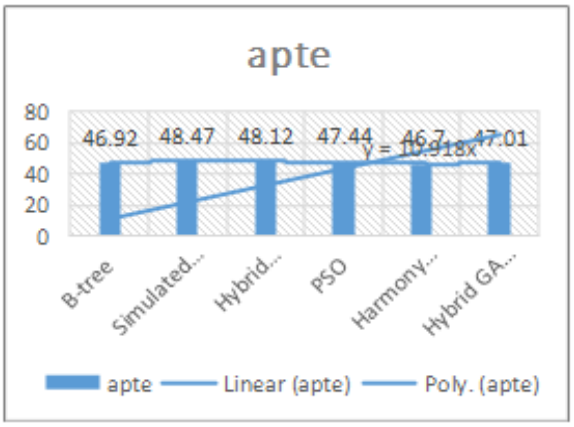


Figure 8: Comparison result of apte benchmark circuit.

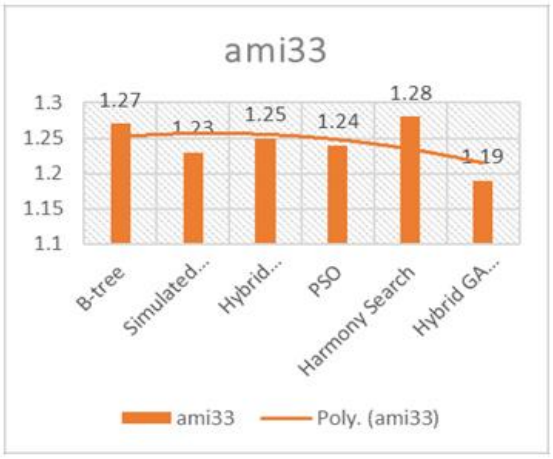


Figure 9: Comparison result of ami33 benchmark circuit.

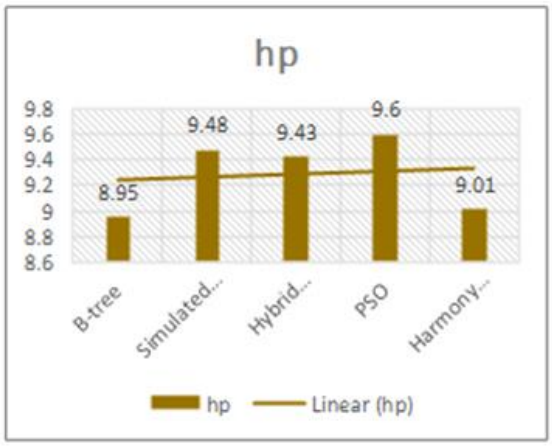


Figure 10: Comparison result of ami49 benchmark circuit.

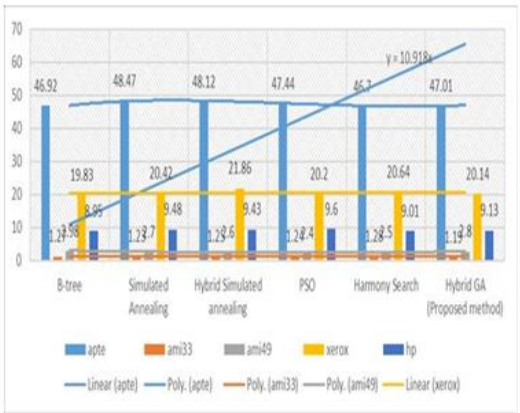


Figure11: Comparison result of hp benchmark circuit.

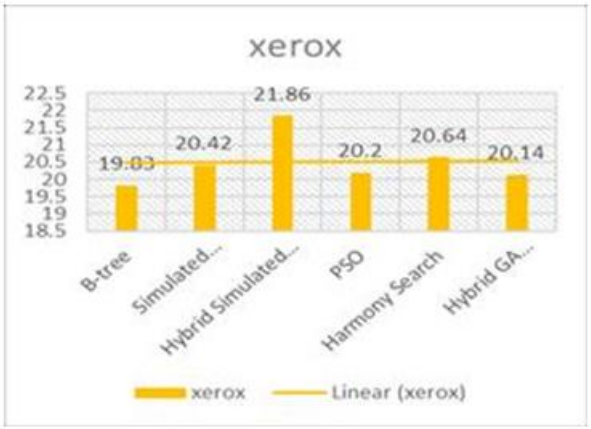


Figure 12: Comparison result of Xerox benchmark circuit.

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