

Path Delay Optimized Booth Radix-8 Architecture

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Abstract: In this paper, a quick and low power marked MAC Unit is proposed with reconfigurable Modified stall calculation (MBE). The proposed engineering depends on adjusted corner radix-8 with consolidated 2's supplement and MUX units with a low basic way postponement and low equipment multifaceted nature. Here corner-based methodology for incomplete items ages and Tree based methodology for halfway items decrease in increases. The new decreases design the equipment intricacy of the summation arrange utilizing consolidated swell convey viper and convey look forward (CLA), along these lines lessens the general power and multifaceted nature. Expanding the speed of activity can be broadened utilizing marked corner radix-8 based MAC unit with noteworthy execution enhancement. We can stall augmentation into two sections, incomplete item age and halfway item amassing. Accelerating augmentation, hence, must point (I) accelerating fractional item age, (ii) decreasing the quantity of incomplete items, (iii) accelerating halfway item summation or (iv) a combination of the above.

Index Terms: Marketing, Segmentation, Technology and Buying Behaviour.

I. INTRODUCTION

The Multiply-Accumulate Unit (MAC) is the fundamental computational portion in DIP structures. The MAC is the urgent factor of deciding force and the speed of the general framework; it generally lies in the basic way. Thus, growing rapid and low power MAC is essential to utilize DSP later WSN. In the multiplication process, the multiplication process is performed by summing the decomposed partial product. For fast multiplication, we need to apply a booth radix recording multiplication process. Now days the advancement in technology booth algorithm technique is changed from 2s-complement method to a signed and unsigned digital format from the given subsequent set. This is known as modified booth algorithm. Multiplication relater function such as Multiply and Accumulate (MAC) and partial product are among some of the frequently used Computation-Intensive Arithmetic Functions (CIAF) applicable in any Digital Signal Processing (DSP) applications such as convolution, Fast Fourier Transform (FFT), filter and in Arithmetic and logic unit [ALU] in Microprocessors and micro controller [1]. Since multiplication is demanding process and it has highest percentage of execution time taken

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be the DSP operation, so there is a need of faster multipliers. In current scenario, multiplication time is still the dominant factor in determining the instruction cycle time of a DSP chip. The demand for high speed processing has been increasing because of expanding computer and signal processing applications[9-11].

Higher throughput arithmetic operations are important to achieve the desired performance in many real-time signal and image processing applications [2]. One of the key arithmetic operations in such applications is multiplication and the development of fast multiplier circuit has been a subject of interest over decades. Reducing the time delay and power consumption are very essential requirements for many applications.

II. BOOTH'S ALGORITHM:

1) Let multiplicand = 4 bits, multiplier = 4 bits, and output = 8 bits.

Product: {0000, Multiplier, 0}

2) Now, take the two least significant bits of the product and depending on the value proceed with one the following:

- 00: No changes to a product.
 - 01: Add the multiplicand to the left side of the product.
 - 10: Subtract the multiplicand from the left side of the product.
 - 11: No changes to a product.
- 3) Right, shift the product by 1 bit.
- 4) Repeat the process x number of times, where x is the number of bits in the multiplicand.

Table 1: Operation to be performed on multiplicand

0000	0
0001	1 x Multiplicand
0010	1 x Multiplicand
0011	2 x Multiplicand
0100	2 x Multiplicand
0101	3 x Multiplicand
0110	3 x Multiplicand
0111	4 x Multiplicand
1000	-4 x Multiplicand
1001	-3 x Multiplicand
1010	-3 x Multiplicand
1011	-2 x Multiplicand
1100	-2 x Multiplicand
1101	-1 x Multiplicand
1110	-1 x Multiplicand
1111	0



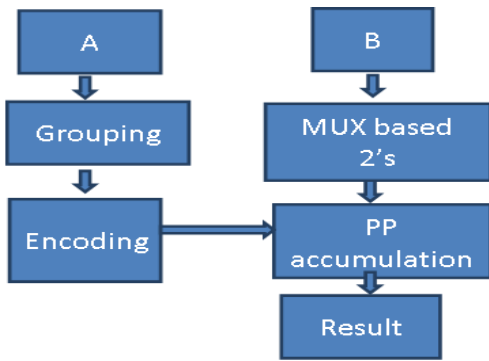


Fig 1. Block diagram for booth multiplier
 Chattopadhyay T, and Gayen, D in the year of 2017 proposed All-optical 2’s complement number conversion scheme without binary addition. In their study they proposed that Generalized 2’s complement converter is designed with binary notations and Input selection based partial products are added for results. The disadvantage of this process is Efficiency is not compared with all other high-speed multiplier and PP reduction scheme not used leads poor speed shown in fig 1.

Qian L, Wang C, Liu W in the year of 2016 proposed Design and evaluation of an approximate Wallace-booth multiplier this paper states Here they proposed hierarchical overlay tree based 8x8 booth multiplication using booth followed by tree-based Partial Product addition architecture for high speed. The disadvantage of this process is Can’t possible to perform higher order binary digits and Sign multiplication is not performed.

Chuang P, Sachdev M, and Gaudet V in the year of 2014 proposed A 167-ps 2.34-mW single cycle 64-bit binary tree comparator with constant-delay logic in 65-nm CMOS this paper states that Generalized bounded comparator model is designed for reduced PP generation and Path selection is modified for final producing results. The disadvantage of this process is Performance Efficiency is not achieved and Poor latency leads Proposed antenna designs for different substrate

III. SOFTWARES USED:

Model sim, and Quarters II are used, Quarters II is used for synthesis and Model sim are design verification.

IV. PROPOSED SYSTEM:

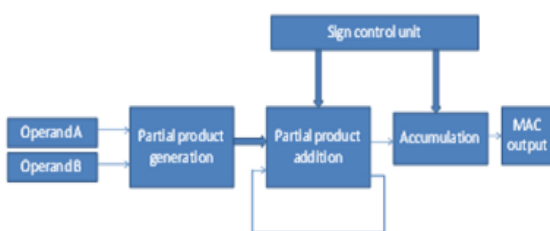


Fig 2. Block Diagram for radix 8 multiplication
 • The Operand A and Operand B are the Input values given to the MAC. Or they can be considered as Multiplier and

Multiplicand shown in fig 2. Here we are considering 8 bits as the size of the operand. In a conventional multiplier, several partial products are formed first by multiplying the multiplicand with each bit of the multiplier. These partial products are then added together to generate the product ‘P’. we can break down multiplication into two parts, namely partial product generation and partial product accumulation. Speeding up multiplication, therefore, must aim
 (i) speeding up partial product generation
 (ii) reducing the number of partial products
 (iii) speeding up partial product summation
 (iv) a combination of one or more of the above.

• The next step involves the addition of these partial products in the fastest manner possible. Speeding up the addition of partial products required faster adders. One of the major problems with fast addition was always due to carry propagation. This can be designed using RB number systems. In an RB number system with the digit set [1,0,1], each digit is coded with two bits. An RB digit X_i can, therefore, be represented by the bit pair (X_i, X_{i+}) . The adder produces a double-precision result of $2n$ bits that must be added to the accumulator content, which are also $2n$ -bits wide. Typical microprocessors will complete the multiplication operation and follow that with a double-precision accumulation operation. This is delay intensive, since both the multiplier and accumulator will each have a delay that is almost $2n$ times the delay of a one-bit full adder. MAC operation can be merged to make the MAC operation take as much delay as a regular multiply operation.

V. SYNTHESIS METHODOLOGY:

The first step in the synthesis process is to read all the components in the design hierarchy. There are three components in the 3-level design hierarchy that needs to be synthesized. Since the RTL model utilizes a Verilog “Package”, then the synthesis tool needs to enable the semantics of a package. In addition, the synthesis tool needs to know if there are multiple instances of calling an automatic function in the design, to preserve separate values for each instance. After reading the design files, they are “Analysed” and “Elaborated” through which the RTL code is converted into the Synopsys Design Compiler (SDC) internal format. [6] The intermediate results are stored in the defined “working library”. After this step, a 40MHz clock signal is applied to the clock port of the root module, and the synthesis tool is programmed not to modify the clock tree during the optimization phase. In addition, an arbitrary input delay of 5ns with respect to the clock port is applied to all input and output ports (except the clock port itself) to set a safe margin by considering any unintended source of delay such as the delay associated with driving module/modules. Then, the design is constrained with the hypothetical maximum area equal to zero to force the tool to make the gate level net list as compact as possible. In the next steps, the tool is programmed to consider a unique design for each cell instance by removing the



multiply-instantiated hierarchy in the current design. Then, the synthesis script removes the boundaries from all the components in the design hierarchy and removes all levels of hierarchy. Finally, the tool compiles the design with high effort and reports any warning related to the mapping and final optimization step. In the end, the tool generates reports for the optimized gate level net list area, the worst combinational path timing, and any violated design constraint

Experimental Result:

The synthesis tool optimizes the combinational paths in a design. In General, four types of combinational paths can exist in any design: [3]

- 1- Input port of the design under test to the input of one internal flip-flop
- 2- Output of an internal flip-flop to the input of another flip-flop
- 3- Output of an internal flip-flop to an output port of the design under test
- 4- A combinational path connecting the input and output ports of the design under test

The last DC command in the script developed in the previous section, instructs the tool to report the path with the worst timing. In this case, the path with the worst timing is a combinational path of type two. The delay associated with this path is the summation of delays of all combinational gates in the path plus the Clock-To-Q delay of the originating flip-flop, which was calculated as 24.09ns. By considering the setup time of the destination flip-flop in this path, which is 0.85ns, the 40MHz clock signal satisfies the worst combinational path delay. The delays of combinational gates, the setup time of flip-flops and Clock-To-Q values are derived from the LSI_10k library file that was used for the mapping step during synthesis. The synthesis timing report is shown below 4&5:

VI. SYNTHESIS AREA RESULT:

The combination zone report demonstrates the all-out number of cells and nets in the net list. It likewise utilizes the region parameter related with every cell in the LSI_10K library document, to figure the absolute combination and successive territory of the net list. The all-out zone of the door level net list is obscure since it relies upon the all-out zone of the interconnects, which itself is a component of the wiring load display utilized in the physical plan. The all-out cell zone in the net list is accounted for as 22978 units, which is the entirety of combination and successive territories. The amalgamation territory report is appeared as follows :

VII. SYNTHESIS CONSTRAINT NETLIST RESULT:

To enforce the synthesis tool to create the most compact net list, the area of the gate level net list was constrained to zero during the synthesis process. As a result, the only constraint violation, which is expected, is related to the area as shown 3&6.

VIII. CONCLUSION:

In this work, the performance of modified Booth and

approximation-based implication for improved systems. Initially, the Booth and its functionality analyzed using MODELSIM. The proposed algorithm is based on 2's complement encoded model to finely save external resource utilization in addition to implementation of radix 8 encoding in MAC(Multiplication Accumulator Unit). We analyzed the area complexity of the design, Timing and Power consumption. We also illustrated the performance of proposed booth algorithm in numerical simulations, and our algorithm shows a significant complexity reduction and energy measure improvement compared to the conventional booth, while the tradeoff is much lower compared to the conventional approach .

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