Design of 13T SRAM Bitcell in 22nm Technology using FinFET for Space Applications

T.R.Dinesh Kumar, M.Anto Bennet, R.Aishwarya, S.Elamathy, M.Kowsalya, C.Ranti Bownisha

Abstract*: Majority of youngsters' having connected online through internet either through computers or by smart phones. After the entry of Jio in the field of internet, the competition began and the cost of internet service became much cheaper andnoweveryone SRAM can be found in the cache memory which is a part of the RAM digital to analog converter. SRAM is used for high speed register and some of the small memory banks. The risk of these circuits and memory arrays which are capable to radiation effects than circuits powered at minimal supply voltages. when an high energy particle hits a sensitive node in a circuit soft errors like Single Event Upsets(SEUs)occurs. The attainment of radiation hardening of memory blocks is executing large bit cells or single Error Correcting Codes(ECCs). But ECC may require notable area, performance and leakage power penalties. The favorable device characteristic of FinFET avails them as a popular contender for the replacement of CMOS technologies. An optimal approach to reduce the leakage power of a 13T SRAM cell based on 22nm FinFET technology is proposed in this work . The circuit contains a dual- driven separated feedback mechanism to tolerate the upset with charge of deposits . Better immunity is supplied by this cell to soft errors when compared to 6T SRAM cell.

Keywords-Radiation hardening, low voltage, critical charge, Single Event Upset(SEU), FinFET, Static Random Access Memory(SRAM), Memory array, soft errors, Ultra Low Power (ULP).

I. INTRODUCTION

The most important aspects of VLSI chips for space applications where the available energy resources are limited. In future, low cost satellite with low power can be achieved by limiting the use of heavy batteries which reduces the satellite weight. By reducing the supply voltage to near threshold or sub-threshold region the Ultra Low Power (ULP) operation can be attained. But it has serious responsibility to modern electronic systems that are capable to radiation effects than circuits powered at supply voltages. Among them SRAMs which is used in modern microprocessors for high speed computation gets affected. Therefore, leakage current plays a large separation role in total power consumption. The low voltage fault-tolerent memory design arise from two emerged requirements, ultra low-power consumption and Single-Event Upset(SEU)tolerance. SEUs occur in standard terrestrial environment at non negligible rates .To overcome these soft errors there are various solutions such as Error Correction Coding(ECC) and Triple Modular Redunancy (TMR). A multigate device transistor refers to a MOSFET that includes more than one gate into a single device. The FinFET structure consists of thin fin of silicon body on a substrate.

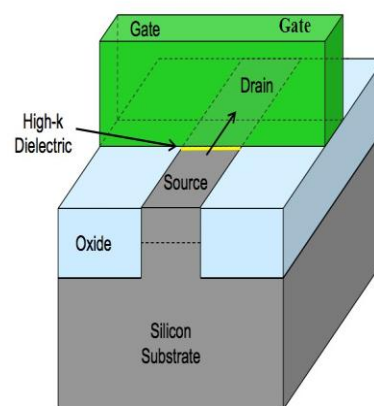

Fig 1:planar of FinFET

The gate is folded around the channel providing excellent control from three sides of the channel. This structure is called the FinFET because its si-body resembles the back fin of a fish. The planar of the FinFET is shown in Fig 1. The 22nm FinFET process technology platform is ideal for high performance, power efficient and high volume applications. FinFET is a promising device structure for scaled CMOS logic/memory applications in 22nm technology

II. CONVENTIONAL 6T SRAM UNDER SEUs

An SRAM bit-cell is the basic unit of SRAM array. Bitcell is used to store one bit of information. It can be used for read and write operation the 6T SRAM bit-cell consists of two cross coupled inverters to form a latch and store binary information .It also contains two access transistors connected to each data storage node. The data current is passed during read and write operation using access transistors and isolate

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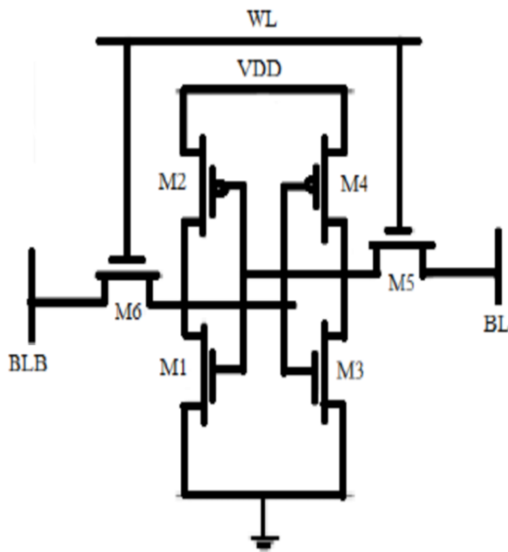
T.R.Dinesh Kumar, Assistant professo, Electronics and CommunicationEngineering, Vel tech, Chennai-600062
Dr.M.Anto Bennet, Professor, Electronics and Communication Engineering, Vel tech, Chennai-600062
R.Aishwarya, Electronics and Communication Engineering, Vel tech, Chennai-600062
S.Elamathy, Electronics and Communication Engineering, Vel tech, Chennai-600062
M.Kowsalya, Electronics and Communication Engineering, Vel tech, Chennai-600062
C.Ranti Bownisha, Electronics and Communication Engineering, Vel tech, Chennai-600062

cell from neighboring node in hold operation. An SRAM bit-cell as three mode of operation: read, write and standby. The design of 6T SRAM FinFET bit-cell is shown in the Fig



2.

Fig 2: 6T SRAM FinFET Bitcell

The conventional 6T SRAM memory cell, shown in Fig. 2 utilizes an active feedback loop between two cross-coupled inverters to retain its stored data value. This structure of the SRAM cell is very sensitive to SEUs, as any upset that causes one of the data nodes to cross the switching threshold of the nearby inverter will result in a bit flip. When operating at low voltages, the switching threshold decreases, thereby increasing the soft-error susceptibility of the circuit. To demonstrate an SEU causing a failure in 6T SRAM bit -cell, the following example will assume that an energy caused by an SEU. Particle strikes a circuit storing a logic 1 (Q = VDD and QB = 0 V). If the particle strikes the drain of the PMOS transistor, M3, charge will be generated, temporarily changing the state of QB. For notation purposes, we will refer to positively charged strike as a 0 to 1 upset at node QB, as opposed to a negatively charged strike, which we will refer to as a 1 to 0 upset at this node. Before the deposited charge can be cleared to the power supply through the conducting transistor of the feedback inverter (M1), the feed-forward inverter (M2 andM4) switches and discharges Q.

Two basic principles to provide the 6T SRAM bit-cell with inherent SEU tolerance.

1) The data are read out from node Q, such that any upset on other nodes can be tolerated.
2) The assisting nodes are designed with redundancy to more than any upset will be blunt by the other nodes.

When a radiation strike causes a value damage on any node of the bit-cell, the other four internal nodes are designed, so the change at this node cannot flip the cell and the disruption is suppressed within a deterministic recovery time. For example, an upset at Q will be suppressed through the dual-driven mechanism created by the internal inverters. Due to their separation, upsets at QB1 and QB2 will not be able to change the state at Q and will return to their original state

III. PROPOSED 13T SRAM BITCELL USING FINFET

The design of SRAM for low voltage operation has began popular in the recent past. Addition of transistor in to the excel topology to the base line of 6T SRAM bit-cell these bit-cell were `operated under standard operating environments and so they do not provide enough robustness to SEUs under high radiation condition. The 6T SRAM cell has the same hardening ability they are extremely low particularly when compared with radiation hardening design. The proposed bit-cell enables robust, high voltage, high radiation environments and ultra low power in space application . This is achieved by designing a dual-feedback, separated-feedback mechanism. The architecture of 13T SRAM bit-cell using FINFET is shown in the Fig 3.

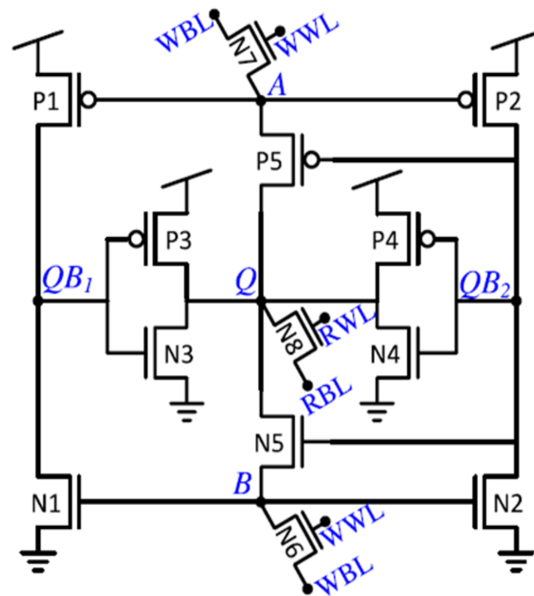


Fig 3: Architecture of 13T SRAM bit-cell

The proposed bit-cell is designed to enable robust, low-voltage, ULP operation in space applications and other high-radiation environments. This is achieved by a dual-feedback, separated-feedback mechanism to overcome the vulnerability due to supply voltage scaling. The schematic representation of the proposed 13T bit-cell is shown in Fig. The storage mechanism of this circuit has five separate nodes: Q, QB1, QB2, A, and B, with the acute data value stored at Q. This node is driven by a pair of CMOS inverters made up of transistors N3, P3, N4,and P4 that are, driven by the inverted data level, stored at QB1 and QB2. QB1 and QB2 are respectively, driven to VDD or GND through devices P1, P2, N1, and N2that are controlled by the weak feedback nodes A and B that are connected to Q through a pair of devices(P5 and N5) gated by QB2. By driving the acute data level by a pair of nodes driven, but independent, inverters, a strong, dual-driven feedback mechanism is applied with node separation for SEU protection.

IV. SIMULATION RESULTS

V. A] 6T SRAM BIT-CELL

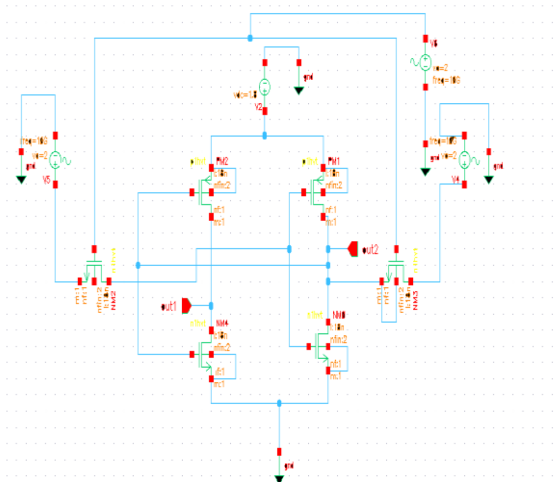


Fig 4:Schematic diagram of 6T SRAM bit-cell

READ MODE

Word line is declared(WL=1),which allow both the access transistor and connect cell from the bit lines BL and BLB. Values stored in the nodes Q and QB are transferred to respective bit-lines BL and BLB. If 1 is stored in node Q then M2 and M4 will on and M1 and M3 will off.BLB will discharge through the driver transistor M4 and BL will be pulled up through the load transistor M2 toward VDD. The schematic diagram of 6T SRAM bit-cell is shown in the Fig 4.

WRITE MODE

Word line is declared(WL=1). If 1 is stored and 0 is to be written in the cell then bit line BL will be 0V and BLB is raised to VDD. For proper functioning of SRAM cell read and write operation have to be taken in mind. This decide the stability of read and write operation.

STANDBY MODE

In this mode word line is not asserted (WL=0), so that assert transistor M5 and M6 will be off and there is no data assert by the bit-cells. The feedback is continued in the cross coupled inverters and hold the data in the latch as it is connected to the supply. The output waveform of 6T SRAM bit-cell is shown in the fig 5.

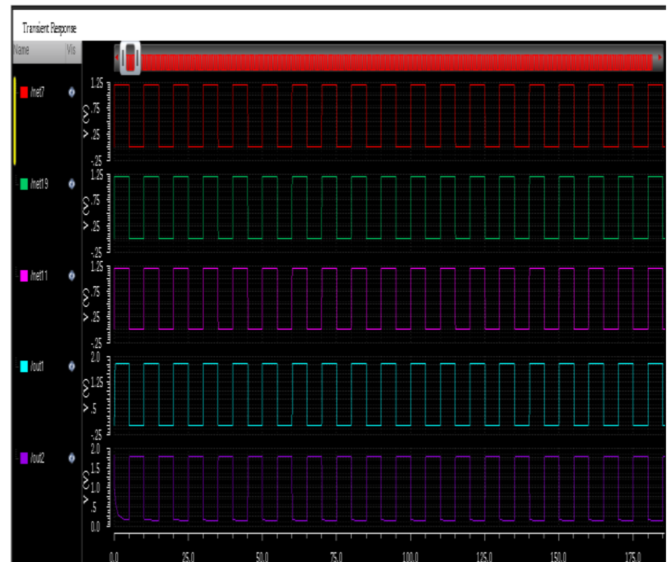


Fig 5:output waveform of 6T SRAM bit-cell

B]13T SRAM BIT-CELL

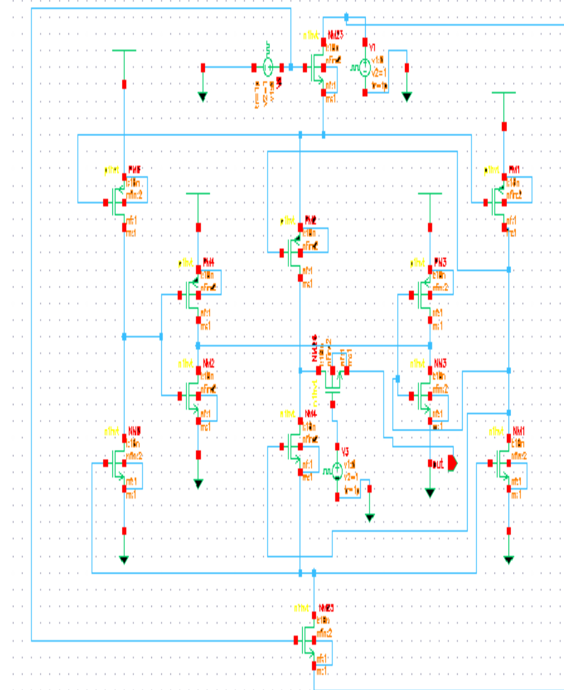


Fig 6:Schematic diagram of 13T SRAM bit-cell(logic 1)

READ MODE

The read access transistor in the proposed 13T SRAM bit-cell is (N8) this is controlled by a separate read word line connected to a read bit line, read operation is discharged depending on the voltage stored at Q. The Q is driven to is stable value due to the dual drive feedback so such operation is robust and faster than read operation. The failure of 6T SRAM occurs when the access transistor is stronger than the pull down transistor due to local variation. The schematic diagram of 13T SRAM bit-cell using FINFET(logic 1) is shown in the Fig 6.

However, the proposed 13T SRAM bit-cell contains pair of pull down transistors (N3

and N4) which decreases the read failure. The output waveform of 13T SRAM bit-cell(logic 1) is shown in the Fig 7.

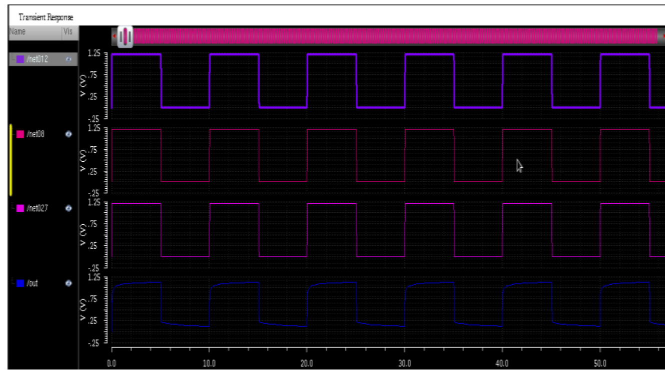


Fig 7: Output waveform of 13T SRAM bit-cell(logic1)

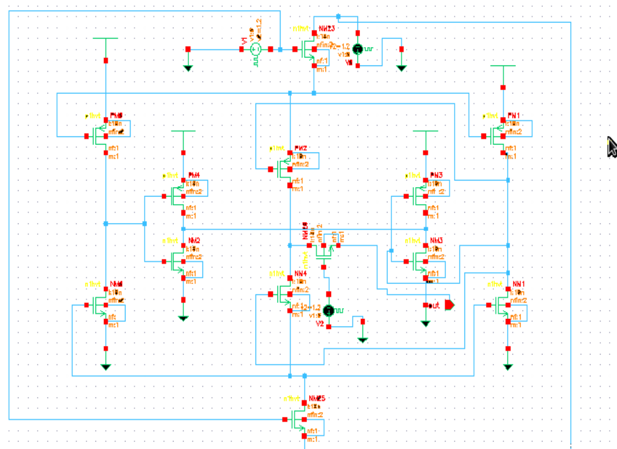


Fig 8:Schematic diagram of 13T SRAM bit-cell(logic 0)

WRITE MODE

The proposed work achieves writes by driving the weak feedback nodes (A and B), thereby removing much of the ratioed contention, inherent to direct access. A pair of write access transistors (N6 and N7) connect a unified write bit-line (WBL) to nodes A and B. The schematic diagram of 13T SRAM bit-cell(logic 0)is shown in the Fig 8. These devices are controlled by a write word line (WWL), such that when WWL is raised, A and B are pulled toward the level driven upon WBL. This virtual connection between A and B creates inverters out of the transistor pairs of N1, P1 and N2, P2, driving QB1 and QB2 to the opposite level of WBL. Accordingly, the written data level is driven back to Q through the dual-driven feedback inverters, bringing the cell to a stable state. The Output waveform of 13T SRAM bit-cell using FINFET (logic 0) is shown in the Fig 9.

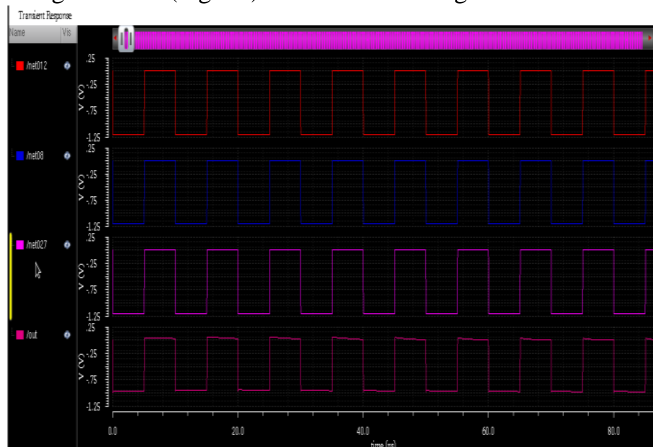


Fig 9:Output waveform of 13T SRAM bit-cell(logic 0)

TABLE 1:POWER CALCULATIONS

TECHNOLOGY	CMOS(45nm)	FINFET(22nm)
6T	2.18W	1.2W
13T	3.17W	1.4W

The power calculations of CMOS and FINFET is shown in the Table1. By Comparing the technology of CMOS(45nm) and FINFET(22nm) for 6T SRAM bit-cell the power of CMOS is 2.18W, the power of FINFET is 1.2W. By comparing the CMOS(45nm) and FINFET(22nm) for 13T SRAM bit-cell the power of CMOS is 3.17W and the power of FINFET is 1.4W

TABLE 2: DELAY CALCULATIONS

TECHNOLOGY	CMOS(45nm)	FINFET(22nm)
6T	1.3W	1.0W
13T	1.5W	1.2W

The delay calculations of CMOS and FINFET is shown in the Table 2. By Comparing the technology of CMOS(45nm) and FINFET(22nm) for 6T SRAM bit-cell the delay of CMOS is 1.3W, the delay of FINFET is 1.0W and also by comparing the CMOS(45nm) and FINFET(22nm) for 13T SRAM bit-cell the delay of CMOS is 1.5W and the delay of FINFET is 1.2W

VI. CONCLUSION

The proposed system of the SRAM is comparatively faster than DRAM. Hence it takes less time for accessing data or information and also has low power consumption compared to DRAM. FinFET reduces leakage power and increases the speed compared to CMOS and both are compared at 45nm and 22nm respectively. The 6T SRAM and 13T SRAM using FINFET is designed in cadence tool. Here, in the proposed work power and delay is reduced using FINFET compared to CMOS.

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