Six Transistor Carbon Nanotube Field Effect Transistors Based RAM Design and Hardware Description Language Code Development

S.Tamil Selvan, M.Sundararajan

Abstract: The goal of this thesis is to develop carbon nanotube field effect transistors (CNFETs) based static random-access memory (SRAM) and implement it into a Very-highspeed integrated circuit Hardware Description Language Analog and Mixed-Signal (VHDLAMS). To achieve this objective, a compact model of the transistor known as enhancementmode MOSFET-like SWCNT-CNFET is used. This circuit-compatible model of CNFET is described using VHDL-AMS and tested for basic electrical characteristics. This model is valid for CNFETs with channel lengths greater than 20 nm. Based on the CNFETs a new SRAM is designed, and implemented in VHDL-AMS. The performance of the proposed SRAM cell is investigated and compared with SRAMs from conventional metal-oxide semiconductor field effect transistors (MOSFETs). The effect of substrate biasing a CNFET is also demonstrated and implemented in designing the SRAM cell. The VHDL-AMS codes of the CNFET and the SRAM are simulated in software known as Ansoft Simplorer. The compact model of the CNFET is organized hierarchically in three main levels. The first level models the intrinsic channel just beneath the gate of the transistor. The second level builds upon the first level and models the doped source and drain regions of the CNFET. The last level represents the complete trans-capacitance model of the transistor and accounts for multiple CNTs. The proposed SRAM cell is composed of four CNFETs and two load resistors. The driver CNFETs of the proposed SRAM cell are substrate biased. Besides, 8-bit complete SRAM architecture based on this cell is indicated. The performance analysis of the SRAM shows that it has better writing and reading speed as well as better stability when compared with SRAM from conventional MOSFETs. Specifically, the newly proposed SRAM cell has read time of twenty five pico seconds, write time of twenty pico seconds and can tolerate a noise of 120 mV at 32 nm node technology.

Keywords----- SRAM, 3 VL, CNTFET, CMOS, low power, highly stable.

I. INTRODUCTION

Beginning from the first decade of the twentieth century electronic circuitry has undergone tremendous changes following the invention of vacuum tube. In those days, the active components (vacuum tubes like triode) and passive components (such as resistors, capacitors and inductors) of circuits were separate and distinct units connected by soldered leads. After the invention of the transistor in 1948, integrated circuits (ICs) were developed in 1959 [1]. When compared with the discrete components, ICs are advantageous due to their very small physical size and mass, high reliability, low power consumption, low cost, improved response time, higher yield and can be easily replaced. ICs started with bipolar processes, and then they were gradually replaced by metal oxide semiconductor (MOS) and complementary metal oxide semiconductor (CMOS) devices. In the first decade of the 21st century, about 88% of the IC market was MOS based and about 8% BJT based. Of the entire semiconductor industry, about 86% were digital ICs. Semiconductor memories such as dynamic random-access memory (DRAMs), static random-access memories (SRAMs), and nonvolatile flash memories made up approximately 25% of the market, microprocessors about 25%, and other application-specific ICs (ASICs) about 20% [1].

The thesis is organized in six chapters and appendices. Chapter one generally introduces the thesis by briefly covering the areas in the center of attention and presenting the motivation and the objective of the thesis. The second chapter describes the concepts underlying CNFET and its modeling. The third chapter enlightens SRAM technology emphasizing on the foundations for designing. Chapters four and five focus mainly on the works done. In Chapter 4, the CNFET and the SRAM cell are described using VHDL-AMS. The SRAM is investigated with different parameters and the results are compared with SRAM from conventional MOSFETs in Chapter 5. Finally, the core body of the paper is terminated by presenting concluding ideas and forwarding future works based on the results obtained from the analysis.

II. CNTFET TRANSISTOR

2.1 Carbon Nanotube Field Effect Transistors Carbon nanotube field effect transistor (CNFET) refers to a field effect transistor that utilizes a single CNT or an array of CNTs as the channel material instead of bulk silicon in the traditional MOSFET structure. The operation principle of CNFET is similar to that of traditional MOSFET. CNFETs are introduced in Section 2.1.4 and CNFET compact model is explained in detail in Section 2.2. 2.1.1 Carbon Carbon, nonmetallic chemical element, known by the symbol C, is the fundamental building block of materials in living organisms. A carbon atom has six electrons. In an isolated carbon atom there are two

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electrons in 1s orbital of the inner shell and four valence electrons in 2s and 2p atomic orbitals with ground state configuration 1s2 2s2 2p2 . The valence shell can hold eight electrons, and atoms in general are much more stable when octet state is satisfied. The carbon atom can attain a stable configuration by forming four covalent bonds. Carbon is unique among the elements in the extent to which it forms bonds between like atoms and in the diversity of compounds that are formed. Carbon atoms form long chains, branched chains, and rings that may also have chains attached to them [4]. Carbon occurs in nature in nearly pure form in diamond and graphite [5, 6]. It is also the major component of coal, petroleum, limestone, and materials in living organisms. The density of diamond is about 3.5 grams per cubic centimeter (g/cm3), graphite ranges from 1.9 to 2.3 g/cm3 [5]. Diamond is one of the hardest known materials, while graphite is one of the softest. In 1985 chemists created a new allotrope of carbon by heating graphite to extremely high temperatures [6]. They named the allotrope buckminsterfullerene, after American architect R. Buckminster Fuller. The original fullerene forms molecules of 60 carbon atoms (with a molecular formula of C60) [6]. The molecules are shaped like tiny soccer balls (called buckyballs). Scientists have since discovered other fullerenes, including very narrow, long tubes and the C70 fullerene, an elongated structure shaped more like a football but rounded on the ends [5, 6].

Graphite is black, soft and conductor of electricity. In graphite the atoms form planar or flat layers. Each layer is made up of rings containing six carbon atoms, with each carbon atom being bonded to three coplanar neighbouring atoms by strong covalent bonds of length 0.142 nm and the distance between planes is 0.335 nm [7]. Since the interlayer force is van der Waals, a single layer of graphite known as graphene can be prepared by a simple peeling of the top layer of highly oriented graphite using a tape [7]. As carbon atoms form graphene, three atomic orbitals namely 2s, 2px, and 2py are hybridized into three sp2 orbitals in the same plane while the 2pz orbital remains perpendicular to other orbitals [8]. The hybridized orbitals are responsible for σ-bonds between the adjacent carbon atoms and the 2pz orbital results in π-bonds out of the plane of graphene [8]. Each atom has three σ-bonds (with 120° between any two of the bonds) and belongs to three neighboring rings. The fourth electron of each atom becomes part of an extensive π-bond system [5]. A sigma bond is a bond resulting from head-on overlap of atomic orbitals while a pi bond is a bond resulting from side-on overlap of atomic orbitals [4]. Generally, electrical transport properties are determined by the electrons (holes) near the Fermi level, since only these electrons (holes) have easy access to the unoccupied (occupied) states. In graphene, the π orbitals, which lie near the Fermi level, are responsible for the electrical transport properties by forming delocalized states [8]. The π-bond does not hold electrons as tightly as the σ-bond holds the first pair; therefore, electrons in π-bonds are much more reactive than are electrons in σ-bonds. In diamond, each carbon atom bonds tetrahedrally to four other carbon atoms to form a three-dimensional lattice. The shared electron pairs are held tightly in sigma bonds between adjacent atoms. Pure diamond is an electrical insulator, colorless and is used in industrialcuttingtools[5].

2.1.2 Carbon Nanotubes A carbon nanotube (CNT) can be viewed as a hollow cylinder formed by rolling a graphene sheet. The end-to-end rolled graphene (the CNT) has already created an explosion of research in nanotechnology since its discovery by Iijima in 1991 [7]. CNTs are electrically and thermally more conductive, chemically and biologically more active, and 6 mechanically stronger than graphene [9]. In addition, topological defects such as pentagons and heptagons can be incorporated into the hexagonal network to form capped, bent, toroidal, and helical nanotubes which allow electrons to be localized. A nanotube is called defect free if it is of only hexagonal network and defective if it also contains topological defects such as pentagon and heptagon or other chemical and structural defects [9]. The electron confinement along the tube circumference makes a defect-free nanotube either semiconducting or metallic with quantized conductance whereas pentagons and heptagons generate localized states [9].

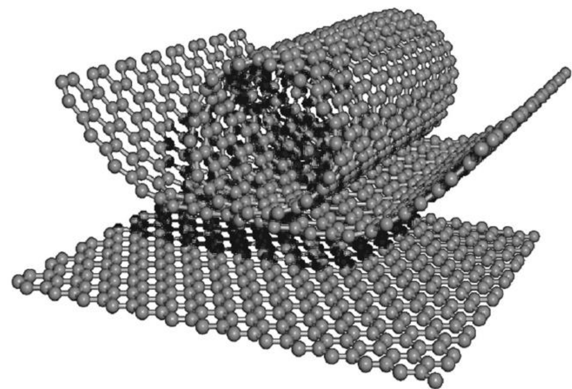

Figure2.1SchematicofGraphene

A single-walled carbon nanotube (SWCNT) is a hollow cylinder of a graphite sheet whereas a multi-walled carbon nanotube (MWCNT) is a group of coaxial SWCNTs. AMWCNT can also be viewed as a scrolled graphite sheet or a spiral graphite sheet, or mixture of scrolled structure and concentric shells. In general, most SWCNTs are defectfree whereas MWCNTs are relatively more defective. The diameter of SWCNT should be at least 0.4 nm large to afford strain energy and at most about 3.0 nm large to maintain tubular structure and prevent collapsing. Typical MWCNT diameter is larger than 2 nm inside and smaller than 100 nm outside [9].

A SWCNT can be uniquely characterized by a chiral vector Ch in terms of a set of two integers (n1, n2) corresponding to graphene vectors a1 and a2 as shown in Figure 2.2 [9,11],

III. STATIC RANDOM ACCESS MEMORY

3.1 Semiconductor Memories

In electronics a memory is a mechanism that stores data for use. Most memories represent data with the binary number system. In the binary number system, numbers are represented by sequences of the two binary digits 0 and 1, which are called bits. In a computer, the two possible values of a bit correspond to the on and off states of the computer's electronic circuitry. A group of eight bits is called a byte. Memory capacity is usually quantified

in terms of kilobytes, megabytes, and gigabytes. One of the semiconductor-based memories that can be read and written by the microprocessor or other hardware devices is random access memory (RAM). The word random implies that information stored in RAM can be accessed in any order, and may be erased or written over. RAM is generally understood to refer to volatile memory since the information is lost after the power is turned off [19].

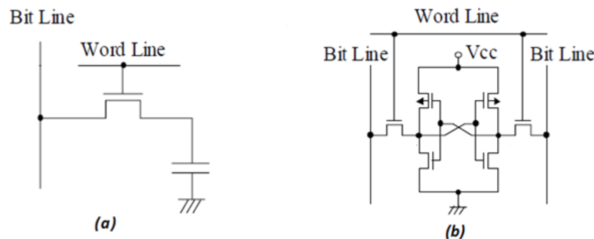

Figure 3.1 (a) One Transistor Cell of DRAM (b) Six Transistor Cell of SRAM [20].

The main types of RAMs are the static random access memory (SRAM) and dynamic random access memory (DRAM). Generally SRAMs store a bit of data in either state of a flip-flop, while DRAMs store a bit as a charge in a capacitor or a transistor gate. The capacitor charge needs to be refreshed to maintain theinformation since there is leakage. Because of this refreshment DRAM is dynamic memory. But SRAM can retain the stored data without any need of periodic refreshment thus it is static memory. DRAM chips are denser than SRAM chips due to their structural simplicity. DRAM is the main RAM used in personal computers, workstations, and servers [5]. There is a growing gap between the processor cycle time and DRAM access time which in turn necessitated the introduction of several levels of caching in modern data processors. In personal computer processors such levels are often represented by L1 and L2 on-chip embedded SRAM cache memories. As the speed gap between processor, memory and mass storage continues to widen, deeper memory hierarchies have been introduced in high-end server microprocessors [21].

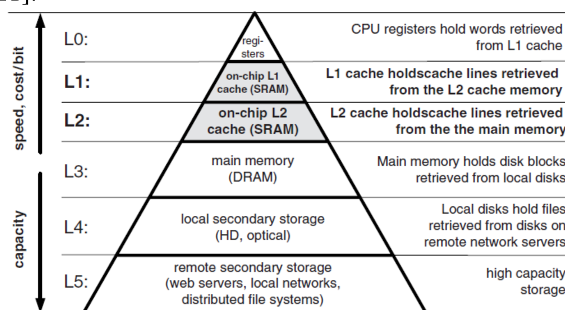

Figure 3.2 Typical Memory Hierarchy of a Personal Computer [21].

3.2 SRAM

The basic architecture of an SRAM includes one or more rectangular arrays of memory cells with support circuitry to decode addresses, and implement the required read and write operations. SRAM memory arrays are arranged in rows and columns of memory cells called wordlines and bitlines, respectively. Each memory cell in a plane has a unique location or address defined by the intersection of a row and column. Each address is linked to a particular data input/output (I/O) pin.

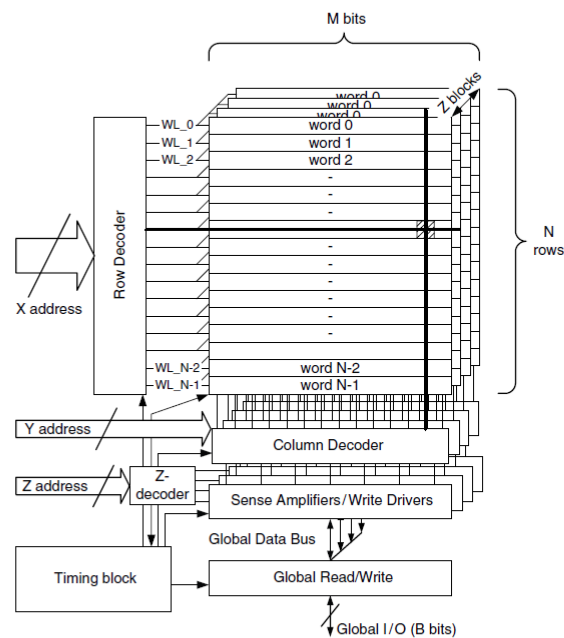

Figure 3.3 Typical SRAM Block Diagram [21].

The number of arrays on a memory chip is determined by the total size of the memory, the speed at which the memory must operate, layout, and the number of data I/Os on the chip. SRAMs can be organized as bit-oriented or word-oriented. In a bit-oriented SRAM, each address accesses a single bit, whereas in a word-oriented memory, each address addresses a word of n bits (where the popular values of n include 8, 16, 32 or 64) [21].Figure 3.3 shows a basic block diagram of an SRAM with four pages of NxM arrays with the corresponding I/O blocks. The SRAM core consists of a number of arrays of NxM, where N is the number of rows and M is the number of bits. A row decoder gated by appropriate timing block signal decodes X row address bits and selects one of the word lines WL_0 – WL_N-1. If an SRAM core is organized as a number of arrays in a page manner, an additional Z-decoder is needed to select the accessed page. Column decoders or column multiplexers addressed by Y address bits allow sharing of a single sense amplifier among 2, 4 or more columns. An additional Chip Select (CS) signal, introducing an extra decoding hierarchy level, is often provided in multi-SRAM chip architectures [21].

3.2.1 Memory Cell

An SRAM memory cell is a bi-stable flip-flop usually made up of four to ten transistors. The flip-flop may be in either of two states that can be interpreted by the support circuitry to be a 1 or a 0. The most common SRAM cells on the market include a siliconbased four transistor cell with a polysilicon load and a silicon-based six transistor cell. The four transistor cell with a polysilicon load is suitable for medium to high performance, this design has a relatively high leakage current, and consequently high standby current. While a six transistor memory cell is highly stable and has low leakage and standby currents. Figure 3.4 shows typical SRAM memory cells.

3.2.2 Support Circuitry

The support circuitry of the SRAM is used to read the data stored in the memory's cells, and write data to the cells.

This circuitry generally includes: address logic to select rows and columns; translation logic that reads the data in a cell and sends that data to the I/O; write logic that takes data applied at the input and stores it in a memory cell; and other control circuitries on the chip.

3.2.3 SRAM Operations

An SRAM cell can be operated in three different states: standby, reading or writing. In standby mode the cell is disconnected from the bit lines but the stored information will be maintained by the cross coupled inverters. In reading mode the stored information will be accessed via the bit lines and delivered to the I/O port by the help of sense amplifier. The sense amplifier amplifies a small analog differential voltage developed on the bit lines by a read-accessed cell to the full swing digital output signal thus greatly reducing the time required for a read operation. Since SRAMs do not feature data refresh after sensing, the sensing operation must be nondestructive. In writing mode the data in the cell is updated by the input drivers.

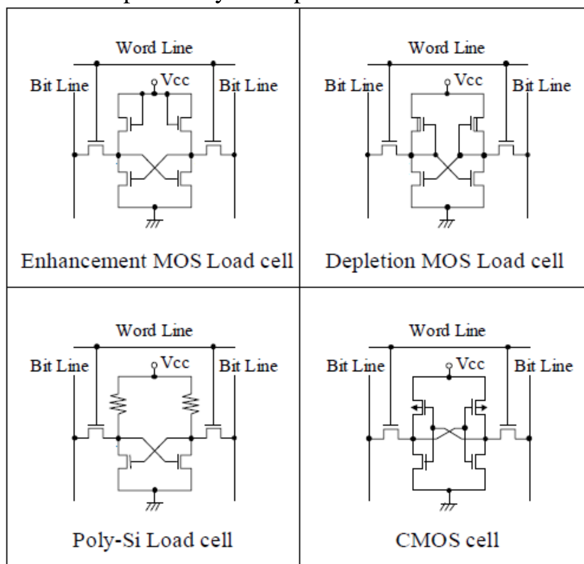

Figure 3.4 Examples of SRAM Cells [20].

3.3 SRAM Design Trends

The process technology scaling for better performance enabled embedding of millions of SRAM cells into contemporary ICs. In several applications, the embedded SRAMs can occupy the majority of the chip area and contain hundreds of millions of transistors [21]. In the early days, the development of SRAMs was focused on low-power applications, especially with very low standby and data-retention power, while increasing memory capacity with high-density technology [22]. After that, however, more emphasis had been placed on high speed rather than large memory capacity, primarily led by cache applications in high-speed micro-processor units (MPUs). These days, the memory capacity is increasing again, reaching more than 200 Mb cache [22].

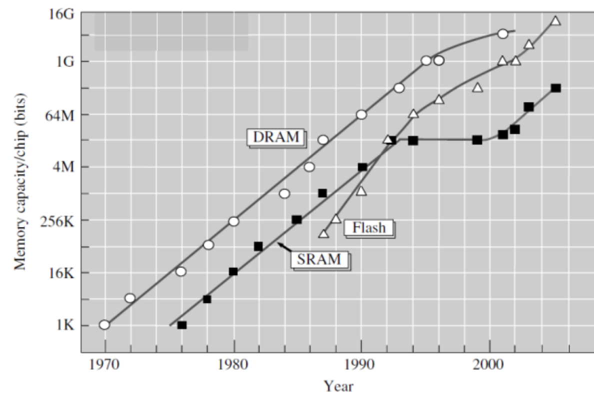

Figure 3.5 Trends in the Memory Capacity of VLSI Memories [22].

As the process technology continues to scale down, the stability of embedded SRAMs is a growing concern for designers. Large SRAM arrays that are widely used as cache memory in microprocessors and ASICs can occupy a significant portion of the chip area. In an attempt to optimize the performance/cost ratio of such chips, designers are faced with a dilemma [21],

- Large arrays of fast SRAM help to boost the system performance.
- The area impact of incorporating large SRAM arrays into a chip directly translates into a higher chip cost. Balancing these requirements is driving the effort to minimize the footprint of SRAM cells. As a result, millions of minimum-size SRAM cells are tightly packed making SRAM arrays the densest circuitry on a chip [21]. Such areas on the chip can be especially susceptible and sensitive to manufacturing defects and process variations. In 2004 International Technology Roadmap for Semiconductors (ITRS) predicted "greater parametric yield loss with respect to noise margins for high density circuits such as SRAM arrays, which are projected to occupy more than 90% of the chip area in 2013" [21, 23]. From Figure 3.5 it can be learnt that there has been tremendous increase in the memory capacity per chip of the semiconductor memories every year except for SRAMs which have stayed with no increment of memory size per chip from 1993 to 2000. Figure 3.6 shows the technology trend in the area per cell of the semiconductor memories as predicted by ITRS in 2008.

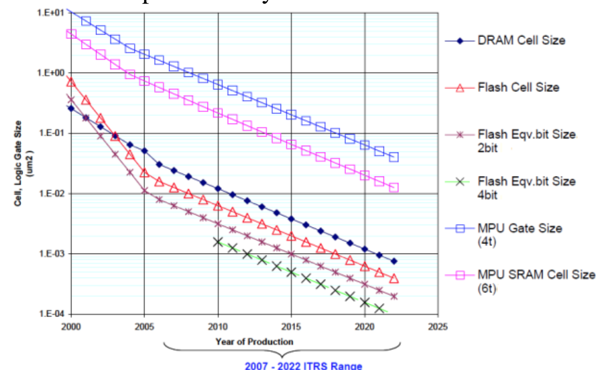

Figure 3.6 ITRS Product Technology Trends [24].

3.3.1 Static Noise Margin

Noise Margin (NM) is the maximum spurious signal that can be accepted by the device when used in a system while

still maintaining the correct operation. A Static Noise Margin (SNM) is implied if the noise is a DC source. It is assumed that noise is present long
enough for the circuit to react, i.e. the noise is “static” or DC. Referring to Figure 3.7 the noise margin high (NMH) and noise margin low (NML)
can be defined as [21]:

NMH =VOH −VIH (3 - 1)

NML =VIL−VOL (3 - 2)

where,

- VIL is the maximum input voltage level recognized as logical “0”,
- VIH is the minimum input voltage level recognized as a logical “1”,
- VOL is the maximum logical “0” output voltage,
- VOH is the minimum logical “1” output voltage.

Any inverter transfer curve, which falls into the shaded area, will have noise margins at least as good as given by the equations above. Input voltage in the range of VIL < Vin < VIH may not be properly recognized by the gate and may cause a logic error.

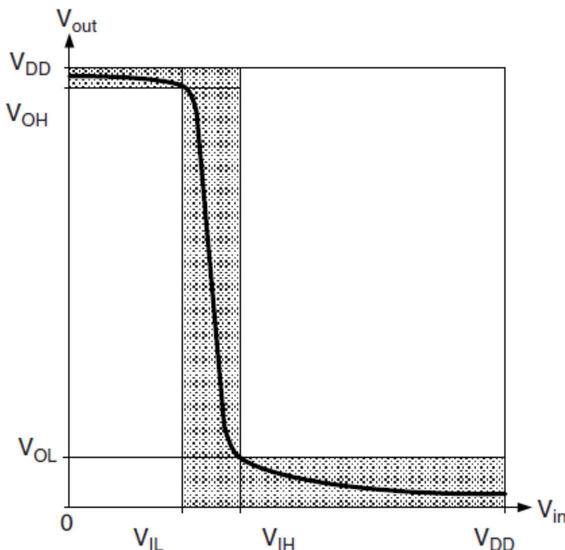

Figure 3.7 Inverter Transfer Curve [21].

3.3.2 Stability Test Setups

An accurate and consistent representation of unstable behavior of an SRAM cell is essential for SNM modeling and evaluation of circuit techniques for SRAM cell stability test. Since the SNM is a measure of SRAM cell stability, its degraded value results in cell stability fault. A stability fault model, illustrated in Figure 3.8, considers the dependence of the SNM on the resistance between node A and node B. The resistor between node A and node B represents cell stability fault model. This SRAM cell has the worst-case SNM in the read-access mode when both the bit lines are precharged and the word line is activated [21].

Each half of a read-accessed SRAM cell can be represented as an equivalent inverter, as
shown in Figure 3.8(b). In a simulation environment, a cell with a resistor of a specified value between node A and node B can imitate a weak cell with a specified SNM value.

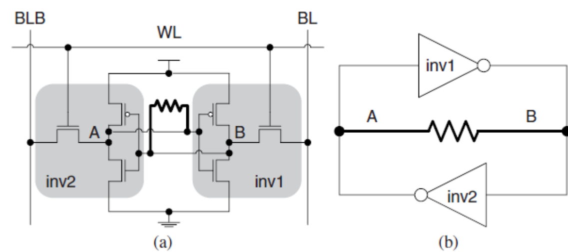

Figure 3.8 (a) Weak Cell Fault Model; (b) Its Equivalent Circuit [21].

IV. CNFET-BASED SRAM

4.1 CNFET Model

We have selected a type of CNFET known as enhancement-mode MOSFET-like SWCNT-CNFET for designing the SRAM rather than the Schottky Barrier CNFET because MOSFET-like CNFET has lower leakage current, no ambi-polar property, better efficiency of injecting carriers from S/D into the channel and better fabrication feasibility. Even though
many physical aspects of the CNFET are captured in the NEGF approach, we have selected the compact model since NEGF involves very intensive calculations and it is very difficult
to develop simple intuitive descriptions of the device physics. It is also difficult to use NEGF modeling to rapidly explore device design spaces. The model of the CNFET used here is based on the works by Jie Deng and H. S. Philip Wong [16, 17, 18].

4.1.1 Compact Model

The compact model of the CNFET is based on the ballistic transport assumption and its complete equivalent circuit model is indicated in Figure 4.1. The VHDL-AMS code of this transistor is also developed by mixed structural and behavioral description as can be understood from the code shown in Section 4.1.2, and Appendices D and E. The ports of the transistor are indicated as SOURCE, DRAIN, GATE and BULK or
substrate in Figure 4.1. The notation for the capacitances can be explained as follows:

Cbd = capacitance between the bulk and the drain at level one of the model

Cbs = capacitance between the bulk and the source at level one of the model

Cgb = capacitance between the gate and the bulk at level one of the model

Cgd = capacitance between the gate and the drain at level one of the model

Cgs = capacitance between the gate and the source at level one of the model

Cbdd = capacitance between the bulk and the drain at level two of the model

Cbss = capacitance between the bulk and the source at level two of the model

Cgdd = capacitance between the gate and the drain at level two of the model

Cgss = capacitance between the gate and the source at level two of the model

Cgtg = gate to gate capacitance at level three of the model

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Cgsub = capacitance between the gate and the substrate at level three of the model

4.2 SRAM Based on CNFET

An SRAM cell can be composed of four to ten transistors. In this paper, we have started from the six transistors based SRAM cell structure and then arrived at a cell composed of four transistors with load resistors; based on the transistors described in

Section 4.1.

4.2.1 New SRAM Cell

To help us propose a new design of CNFET-based SRAM cell, we have started with the cell indicated on Figure 4.2 below by using optimum substrate biasing scheme for each 44 transistor, so as to achieve the best overall performance. In this design each transistor has been properly substrate-biased for each operation i.e. reading, writing and hold modes.

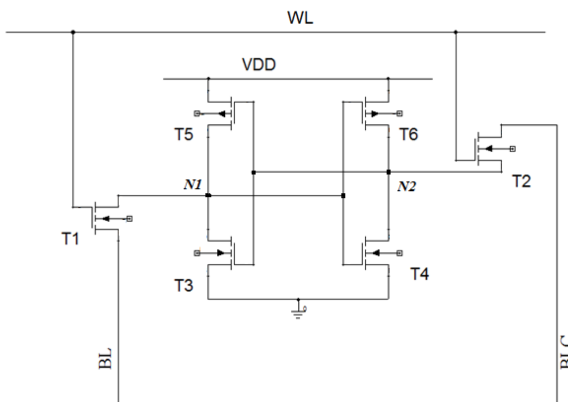

Figure 4.2 Six-Transistor SRAM Cell.

Let's have a brief description on the principles that determine the design. In this SRAM cell four transistors (T5, T6, T3 and T4) comprise cross-coupled inverters and two transistors T1 and T2 provide read and write access to the cell. In other words, T5 and T6

are the pull up or load PCNFETs, T3 and T4 are the pull down or driver NCNFETs, and T1 and T2 are the access NCNFETs. Upon the activation of the word line (WL), the access transistors connect the two internal nodes of the cell to the true bit line (BL) and the bit line

bar or the complementary bit line (BLC). This SRAM cell can maintain the stored data as long as there is power supply, i.e. VDD. The two basic requirements which dictate the design of the SRAM cell are:

1. Reading operation shall not be destructive, i.e. the stored data shall also be available after reading is done.
2. The cell shall allow modification of the data during the writing operation. Therefore, the SRAM cell must be designed such that it provides a non-destructive read

operation and a reliable write operation. These two requirements impose contradicting requirements on the SRAM cell design.

CHAPTER 5

RESULTS

5.1 I-V Characteristics of the CNFET

As discussed in Chapter 2, varying the gate voltage of the CNFET changes its threshold voltage. In addition, varying the substrate voltage can also be used to control the threshold voltage of the transistor. In order to identify and understand the impact of substrate biasing the CNFETs, simulations of both PCNFET and NCNFET have been done at various gate and substrate biasing voltages. The results are indicated in Figures 5.1, 5.2, 5.3 and 5.4. From these simulation results we can infer that if the substrate voltage is decreased the threshold voltage of NCNFET decreases so the current capability becomes higher. In the other case, if the substrate voltage is increased the threshold voltage of

PCNFET decreases. Besides, from Figures 5.2 and 5.3, it can be understood that the substrate can be used as an alternative gate. These simulations are done for a CNFET with CNT of chirality (14, 0) channel length of 32 nm and at a temperature of 300K.

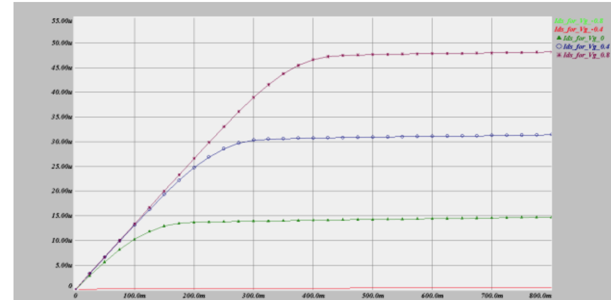

Figure 5.1 NCNFET at Substrate Voltage of -0.6 V and Varying Gate Voltage.

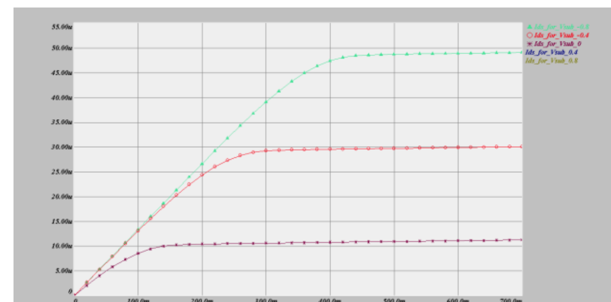

Figure 5.2 NCNFET at Gate Voltage of 0.6 V and Varying Substrate Voltage.

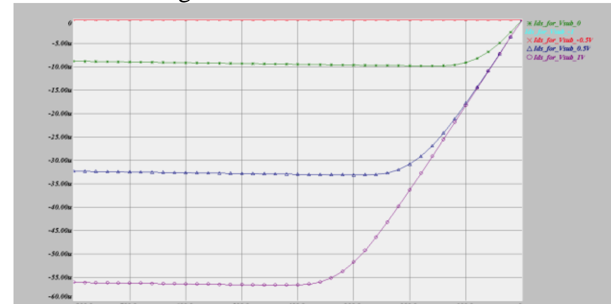

Figure 5.3 PCNFET at Gate Voltage of -0.6 V and Varying Substrate Voltage.

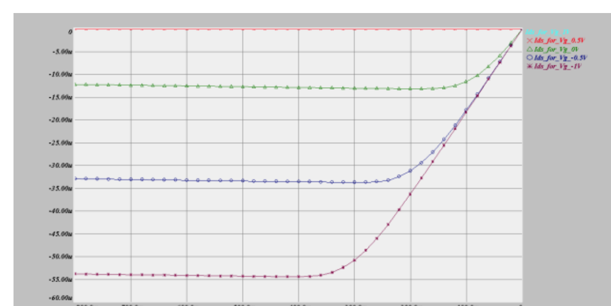

Figure 5.4 PCNFET at Substrate Voltage of 0.6 V and Varying Gate Voltage.

5.2 Read and Write Speeds

The proposed SRAM cell has been simulated for its speed in its reading and writing operations. The time required by the SRAM to change the states of the data storing nodes during its writing operation is named as write time while the time required by the SRAM to
amplify the difference between the potentials of the data storing nodes during its reading operation is named as read time.

5.2.1 Simulation Results

The simulation results shown on Figures 5.5 and 5.6 have been obtained for the
following values:

VDD (voltage source of the SRAM cell) = 0.8 V
PC (pre-charge circuit source) = 0.4 V
RL (load resistances) = 60 kΩ
WL (word line) = 0.6 V at 125 MHz
WE (write enable) = 0.6 V at 200 MHz
RE (read enable) = 0.6 V at 100 MHz Substrate biasing of the driver transistors = 0.3 V.

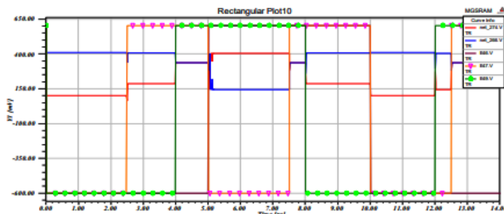

Figure 5.5 (a) The Proposed SRAM Writing '0' and '1'.

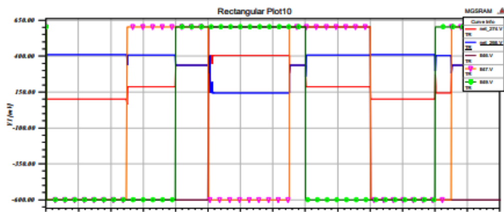

Figure 5.5 (b) The Proposed SRAM Writing '0' and '1' the BL.

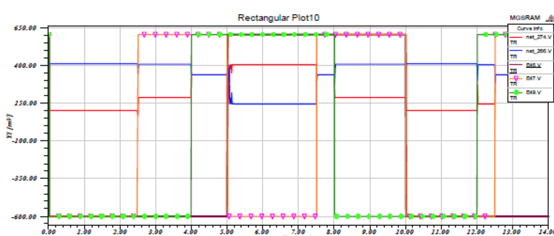

Figure 5.5 (c) The Proposed SRAM Writing '0' and '1'the DI.

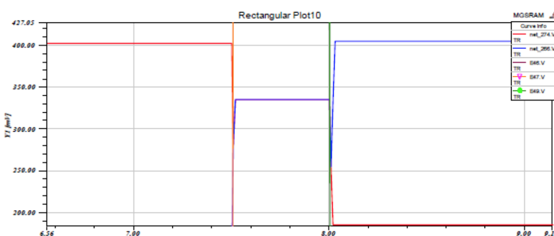

Figure 5.5 (d) The Proposed SRAM Writing '1'at about 8 ns.

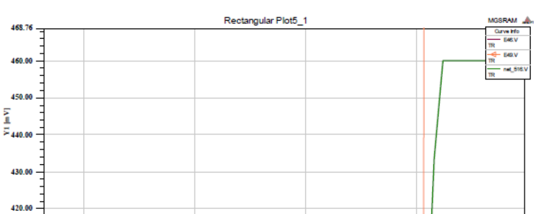

Figure 5.6 (a) The Proposed SRAM Reading '1' at about 12 ns.

In the results of the simulations the representations are as follows:

E47.V for WE (write enable);
E49.V for WL (word line);
Net_274.V for BLC (complementary bit line);
Net_266.V for BL (bit line);
E46.V for DI (data in);
Net_516.V for DO (data out).

The simulation results on Figure 5.5 show the proposed SRAM cell writing logic '0' and logic '1'. Here, it can be observed that the SRAM cell writes when both WE and WL are enabled and changes the data based on the input data i.e. DI. On Figure 5.5(a) the
SRAM writes logic '0' at about 5 ns since both WL and WE signals are enabled and DI at this time is logic '0'. Similarly, the BL has been changed to a state of logic '1' at about 8 ns because both WL and WE signals are enabled (in the interval 7.50 – 8.00 ns) and DI in this time is logic '1'. This information (logic '1') is maintained by the SRAM cell till 12.5 ns because in the interval 8.00 – 10.00 ns only WE is enabled but WL is disabled, in the interval 10.00 – 12.00 ns both WE and WL are not enabled, and in the interval 12.00 – 12.50 ns only WL is enabled. Figure 5.5(b) and Figure 5.5(c) show simulation results emphasizing on BL and DI respectively. As shown in Figure 5.5(c), DI has a period of 10 ns and has a value of logic '0' from 0.00 – 5.00 ns and a value of logic '1' from 5.00 – 10.00 ns while BL is at logic '1' from 0.00 – 4.00 ns because WL and WE are not enabled at the same time in this interval. On Figure 5.5(d) writing logic '1' operation is zoomed to show the delay of the cell at about 8 ns. Figure 5.6(a) and (b) show reading logic '1' operation zoomed to show the delay of the cell at about 12 ns and 2.5 ns respectively.

V. CONCLUSION AND FUTURE WORKS

6.1 Conclusion

In this thesis a compact model of a type of CNFET known as enhancement-mode MOSFET-like SWCNT-CNFET was studied. The model includes the intrinsic channel
model, the doped source/drain extension regions model and multiple nanotubes transistor model. The thermionic and band-to-band tunneling currents from the semiconducting subbands are considered as the main current contributors for the transistor in this model. It takes into consideration elastic scattering, acoustic and optical phonon scattering, parasitic capacitances and resistances, SB-resistances and screening effects among multiple nanotubes. The model was described in hardware description language known as VHDLAMS. The VHDL-AMS code encompasses structural description of the equivalent circuit and behavioral code of the mathematical expressions in a separate package. The complete
VHDL-AMS code of the transistor was used to study the electrical characteristics of the CNFET. The influence of substrate biasing on the CNFET was simulated and the results confirm that the substrate (bulk) can be used as an alternative gate or additional terminal to control the transistor. Based on the CNFET, a new SRAM cell was developed. The proposed SRAM cell is composed of four CNFETs (two of which are

substrate-biased) and two load resistors. The SRAM was implemented in VHDL-AMS. The VHDL-AMS code was simulated to study the performance of the SRAM. The simulation results at 32 nm technology show that the proposed SRAM cell is faster than the present SRAMs but less noise tolerant than most
of the SRAMs. When compared with the most common six-transistors CMOS technology based SRAM cell, the proposed SRAM cell exhibits a number of advantages including reduced area occupation, faster reading and writing speeds, and more stability. In general, we can conclude that CNFETs can be used to produce high density and fast digital devices such as the SRAM beyond 32 nm channel length. We can also predict that CNFETs outperform MOSFETs under the same conditions such as at the same operating environment, equal channel lengths and overall dimensions.

6.2 Future Works

Other peripheral circuitry and signal pins used to implement special features such as spare cells management and low power hold mode can also be designed and added to the SRAM. Further studies can be done to develop optimum layout of the SRAM for fabrication and testing. More accurate simulation results can be obtained by using more accurate models such as the NEGF and Monte-Carlo simulations by the help of high speed computers.

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