Performance Parameters of 3 Value 8t Cntfet Based Sram Cell Design Using H-Spice

S.Tamil Selvan, M.Sundararajan

Abstract— this paper presents a design of a 3ValueLogic 9T memory cell using carbon nano-tube field-effect transistors (CNTFETs). The carbon nano tubes with their superior transport properties, excellent current capabilities ballistic transport operation, 3-value logic have been proposed for 8T SRAM cell implementation in CNTFET technology. The CNTFET design to achieves the different threshold voltages. And it also avoids the usage of additional power supplies. The channel length used here is 18nm wide. The power consumption is reduced, as there is absence of stand-by power dissipation. Second order effects are removed by using CNTFET. In a 3 Value Logic, it only takes log3 (2n) bits to represent an n-bit binary number. In 3Value logic 9T memory cell based CNTFET have been developed and extensive HSPICE simulations have been performed in realistic environments. CNTFET 9T based SRAM cell proves which is Dynamic power better than CNTFET, based 3value logic 8T SRAM cell as well as CMOS SRAM cell.

Index Terms—CNTFET, 3ValueLogic, HSPICE, Multi threshold value, FINFET, QDGFET, SNM, SWCNT

I. INTRODUCTION

With the advancement in technology, digital circuits play a very important role. Digital circuits are less susceptible to noise or degradation in quality than analog circuits. It is also easier to perform error detection and correction with digital signals. A computer system, either it be a large machine or be a microcomputer, needs memory for storing data and program instructions. In a computer system there are various types of memories using a variety of technologies and having different access times. The main memory is generally the most easily obtained memory. It is the one from which all instructions in programs are executed. The main memory is generally of the randomaccess type. A random-access memory (RAM) is defined as the memory in which the time required for storing/writing and accessing/reading data is independent of the location in which the information is stored. The read-write (R/W) memory circuits are designed to allow the change (writing) of data bits to be stored in the memory array, as well as their access (reading) on demand. The memory circuit is said to be static if the stored data can be retained indefinitely without any need for a periodic refresh

is the fastest memory in a computer. SRAMs alone possess a large area in the processor and as a result contribute an important part of total power dissipation of the system. Different SRAM topologies are 4T, 5T, 6T, 7T, 8T, 9T, etc. The performances of the SRAM cells are evaluated on the basis of its performance index comprising of parameters like, stability, power, delay, etc. The stability of the cell is measured through Static Noise Margin (SNM) which is obtained from the butterfly curves. Another method for the performance evaluation is the Noise-curves method, popularly known as the N-curves. These curves overcame the drawback of the SNM to measure the SNM through the automatic inline testers, because of the fact that after measuring the butterfly curve the Static Current Noise Margin (SINM) is still to be calculated mathematically Continuous scaling of the MOS devices has resulted to a tremendous improvement in the performance of MOS devices at the cost of increased threshold voltage, leakage current variation, short channel effects, reduced gate control, severe process variation and unmanageable power densities. This scaling has progressed rapidly for three decades, but may soon come to an end. Therefore, alternative technologies to bulk silicon transistors are being explored. A minimum sized SRAM cell is highly needed for increasing the memory integration density. As the integration of components increases, leakage power becomes a prime concern in today's memory chips. Lower voltages and smaller devices cause a significant degradation of data stability in cells. So the development of a memory technology with greater stability and lower power consumption characteristics is, highly desirable. Therefore, alternative technologies to bulk silicon transistors are being explored. Ultra thin body devices such as FinFETs have received increasing attention in recent years. However, it is also important to investigate new materials and devices to replace silicon in nano scaled transistors. Carbon nanotube transistors, for example, are especially promising because their unique one-dimensional band-structure suppresses backscattering and makes nearballistic operation a realistic possibility. As one of the promising new transistors, carbon-nanotube field-effect transistor (CNFET) avoids most of the fundamental limitations for traditional silicon MOSFETs. With ultralong (~1 μm) mean free path (MFP) for elastic scattering, a ballistic or nearballistic transport can be obtained with an intrinsic carbon nanotube (CNT) under low voltage bias to achieve the ultimate device performance. The quasi-1-D structure provides better electrostatic control over the channel region than 3-D device (e.g., bulk CMOS) and 2-D device (e.g., fully depleted SOI) structures. The MOSFET-like CNTFET model is reported to be scalable down to 10 nm channel length, a substantial improvement compared with the available MOSFET model

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(with a minimum channel length of 32 nm). Therefore, a SRAM design with CNTFET requires a significantly less area than its CMOS counterpart

The main objective of the work is to study the performance of different SRAMs with CMOS and CNTFET, then make a comparative analysis based on the performance metrics. Objectives:

• To study the different types of existing SRAM cells topologies.

• Simulate the CMOS based circuits in 32 nm CMOS Technology Node and CNTFET with Stanford University CNTFET Model.

• Make a one to one comparison of all the SRAM topologies in their individual technology node to that simulated in 32 nm CMOS technology node.

• Perform dual chirality in different CNTFET SRAM cells. Introduction

• Select the optimum chirality SRAM and compare it one to one with the CMOS based SRAMs counterpart.

• Now, from the 32 nm technology circuits select the best performance cell and simulate it again in 180 nm technology node and compare the duo.

• Calculate the "SPR" for 180 nm, 32 nm CMOS and CNTFET SRAMs

II. CARBON NANOTUBE FIELD-EFFECT TRANSISTOR

Carbon Nano-Tube Field Effect Transistor (CNTFET) is one of the advanced FET technologies in the VLSI industry. The remarkable electrical properties of carbon Nano-tubes arise from the unified electronic network structure of graphene itself that can binded up and form a excavated cylinder. The CNT is connected between source and drain regions act as the channel material as in the MOSFET device.. The way in which grapheme is rolled is expressed by (n,m)called chiral vector or chirality vector, depending on the dimemsion of the atomic alignment along the tube. In terms of the numbers (*n*,*m*), the nanotube diameter Dt Fig. 1 shows the CNTFET diagram of a CNTFET [9]–[11]. Its have same same function of MOSFET device, we have four terminals in CNTFET. As the gate potential increases, the device is electro statically turned ON or OFF, with the help of gate.

Fig.1 shows the schematic diagram of CNTFET. such as high density of on current and moderately high Ion/Ioff ratio that has many advantages changeable threshold voltage depending on carbon nanotube diameter which is an important characteristic of CNTFETs.

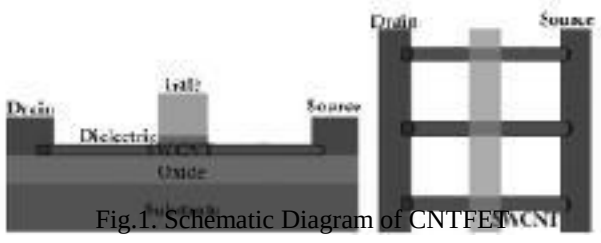

Fig.1. Schematic Diagram of CNTFET

The Voltage is required of transistor 0.6 to turn ON the transistor; the threshold voltage of the intrinsic CNT channel can be approximated to the first order as the half-band gap that is an inverse function of the diameter [9]–[11].

As the diameter of CNT changes, the threshold voltage of the CNTFET will also change. In the chirality voltages m voltage is always zero. then, the ratio of the threshold voltages of two CNTFETs with different chirality vectors .For example, the threshold voltage of the CNTFET having (19, 0) CNTs is 0.289 V because the DCNT of (19, 0) CNT is 1.49 nm. Simulation results have corrected this threshold voltage. the threshold voltage of NCNTFET with different chiral vectors. Extensive research has been reported on manufacturing well-controlled CNTs [13-14]. this paper, CNTFETs with different charity vectors are used and channel length of 18 nm is selected for area efficient 3 value logic CNTFET based SRAM design.

III THREE VALUE LOGIC DESIGN

As abstraction of the traditional binary logic. Three-value logic system has better characteristic compared to previous binary system such as increased bit handling capability per unit area, reduced number and complexity of interconnections, as well as reduced number of active FETs inside a chip. In the circuit the design base on three-valued logic, circuits will be simpler and more flexible also more easy. By using 3VL speed and less dynamic power.will be achieved [13] [14]. To obtain 3value logic system we need three values, in conventional binary system we have two logics values '0' and '1', these logics represented by 0V and Vdd respectively. supplementing one state between these two logics of conventional binary system ternary logic system can be achieved. In 3value logic system values represented by 0V, 0.5v and 1v which denote '0', '1' and '2' respectively.

In principle, 3VL can provide a means of increasing data processing capability per unit chip area. The serial and serial-parallel arithmetic operation can be carried out faster if the 3value logic is employed.

One of the main merits of 3value logic is that it reduces the number of required computation steps. As each input can have three different values, the number of digits required in a three value logic family is log32 times less than that required in binary logic. It is assumed that 3value logic elements can operate at a speed approaching that of the corresponding binary-logic elements. Thus, three value design technique combined with the binary logic design technique also provides an excellent speed and power consumption characteristics in memory circuits.

Here, 0, 1, and 2 denote the 3 logic values to represent true, intermediate, and false, respectively. Any n-variable {X1 ,. . .,Xn} 3 value logic function f(X) is defined as a logic function mapping {0,1,2}n to {0,1,2}, where X = {X1 ,. . .,Xn}. The basic operations of three value logic can be defined as follows, where Xi,Xj $\in$ {0,1,2}

$$Xi \mid Xj = \max\{Xi,Xj\}$$
$$Xi \,\&\, Xj = \min\{Xi,Xj\}$$
$$Xi = 2 - Xi$$

where "–" denotes the arithmetic subtraction, the operations "|," " &," and "–" are referred to as the OR, AND, and NOT in 3value logic, respectively. The 3 value logic gates are designed according to defined in above equation. Here work the set {0, 1, 2} is used, where 0 = false, 1= intermediate, and 2 = true.. The choice of these values leads in a more natural way the adaptation of the ideas from the binary logic

III. 3VL 8T & 9T SRAM CELL DESIGN

A . 8T SRAM Cell Design

Proposed a 8T cell to reduce the activity factor α for reduction of dynamic power. The 8-transistor SRAM cell based on CNTFETs has been designed to improve the read cycle and reduce dynamic power. The transistor level schematic of this cell appears in Figure 3. It adds a transistor N8 in the feedback loop and a separate read line 'Read Bit' from the word line 'Write Bit' of the 6-transistor cell.

The four transistors N1, N2 and N3, N4 in the centre form two cross-coupled inverters INV1 and INV2. Due to the feedback structure, a low input value on the first inverter INV1 will generate a high value on the second inverter INV2, which amplifies and stores the low value on the second inverter INV2. Similarly, a high input value on the first inverter INV1 will generate a low input value on the second inverter INV2, which feeds back the high input value onto the first inverter INV1. The two inverters INV1 and INV2 will store their current logical value, whatever value that is. But in this circuit feedback connection is established through an extra nMOS transistor M7. The circuit stores data at a node 'Q' and its complement at a node 'Q bar'. This circuit uses two separate transistors M5 and M6 to write and read data from memory cell. To write data into cell 'Write Select' signal is used. To read data from the cell 'Read Select' signal is used.

The 8T CNTFET SRAM cell depends on switch off the feedback connection between the two inverters, INV1 and INV2, before a write operation. The feedback connection and disconnection is performed through an extra nMOS transistor N8. During write operation N8 is OFF and during read operation it is ON.

The cell depends only on 'Write Bit' to perform a write operation as shown in Figure

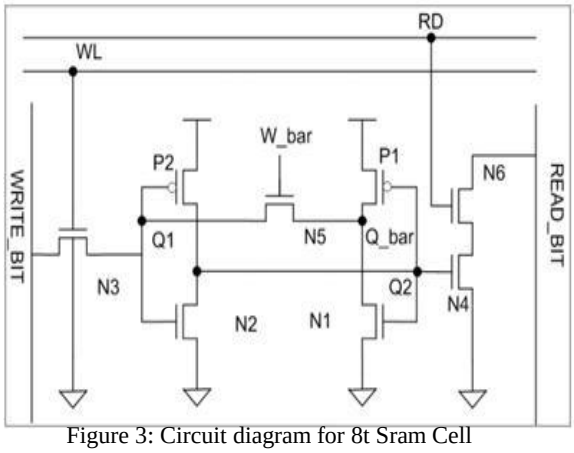

Figure 3: Circuit diagram for 8t Sram Cell

Read Operation

Read operation starts by turning on a transistor N8 using a signal 'Read Select' and turning off the transistor N7. During this operation turning on 'Write Bar' signal connects feedback path. Then the stored data at a node 'Q' can be read at 'Read Bit'. The read cycle is improved based on two aspects of the cell operation namely the ability to pre-charge the read bit line 'Read Bit' irrespective of the activity of the write bit line 'Write Bit' and device sizing of the read zero path with the pull-down transistor N5 of the second inverter made 8 times larger than the N7 to provide a fast path to ground.

Write operation

The write operation working principal is transistor N8 off to switch off the connection, thereby allowing for a fast transfer of the logic value from the write bit line 'Write Bit' into the memory cell. Using a signal 'Write Select', while M6 is kept off as shown in Figure 3 turns on 'Write Bit' carries the input data, N6. The 7T SRAM cell looks like two inverters, INV1 followed by INV2. N6 transistor transfers the data from 'Write Bit' to Q1, which drives INV1, N1 and N2, to develop 'Q bar'. Same, 'Q bar' drives INV2, N4 and N5, to develop 'Q', the cell data.Then, N6 is turned off and N8 is turned on to reconnect the feedback link between the two inverters to stably store the new data. Dynamic power reduction would result from the reduced switching activity during memory accesses. The 'Write Bit' line does not have to be pre-charged in preparation for the read operation and a write operation affects only a single bit line of the cell compared to both for the 6-transistor memory cell.

A . 9T SRAM Cell Design

The need of 8T-SRAM has originated from the fact that the 6T SRAM has more power consumption and less immunity to noise voltage during read operation as a small noise voltage is enough to flip the data. Designing an efficient cache system with 8 transistors in basic SRAM cell provides increased stability and good effective memory speed. Figure 4 shows the 9T SRAM cell configuration based on CNTFETs, where the write and read bits are separated to improve read cycle. In 8T SRAM only the Write bit is used to write for both "0" and "1"data, while BIT and BIT lines are utilized for writing data in the conventional 6T SRAM.

The writing operation starts by breaking the feedback loop of the cross-coupled inverter. During read operation, the feedback loop is maintained. The feedback loop is disconnected by setting Write bit to"1".In this case, SRAM memory cell has just two cascaded inverters. The Wbit line voltage decides the data that is going to be written into SRAM cell. The Wbit line transfers the inversion of the input data to Q2 (cell data), which drives the other cascaded inverter to get Q_bar. The Wbit line has to be pre-charged before and after each write operation. When writing "0" data, there is no. Discharging at WBit line so negligible power is consumed. But writing '1' data at Q2, the dynamic power consumption is same as 6T SRAM cell because the WBit line has to be discharged to ground level. The proposed 8T SRAM cell is more power efficient in comparison with conventional ones because during write operation, the circuit does not require discharging for every write operation but discharges only when writing "1" data, and the discharging activity factor of the WBit line is less than 1.

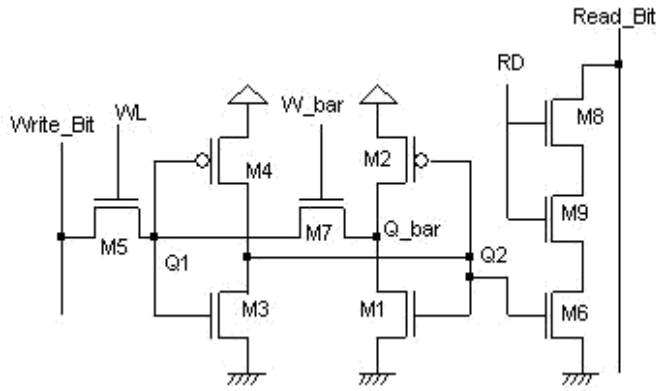

Figure 4: Circuit diagram for 9t Sram Cell

The Rbit line has to be pre-charged before any read operation. During read operation, Read bit is "high" and Write bit is low, which set turning ON condition for M6 & 7. When Q2="0", the transistor M4 is OFF maintaining the Rbit line at the pre-charged value, which shows the cell data Q2 holds "0". On the other side, when cell data Q2= "1", both the transistors M6 and M8 are ON which makes the Rbit line to be dropped at few millivolts, which is quite enough for detection in the sense amplifier. In the proposed 8T SRAM cell design, the device sizing of the read zero path with pull down transistor M5 and M7 is made 8 and 6 times larger to get a quicker discharge path to ground. In this design, two PCNTFET (P1,N5) with one tube, two NCNTFETs (N2,N3) with two tubes, one P-type CNTFET (P2) with two tube, one NCNTFET (N1) with one tube, are utilized for proper functionality and shorter delay at the minimal cost of the chip area overhead. Compared to CMOS SRAM cell with a transistor length of 32nm, a CNTFET SRAM cell offers a significant saving in chip area.

IV SIMULATION RESULT

THE 9T SRAM CELL BASED ON CNTFET IS DESIGNED AT 18NM TECHNOLOGY. ANOTHER 8T SRAM CELL AT 18NMNM TECHNOLOGY
IS ALSO DESIGNED FOR COMPARISON. THIS CIRCUIT IS SIMULATED IN HSPICE MODEL AT 18NM FEATURE SIZE WITH SUPPLY VOLTAGE VDD OF 1.0V

Simulation setup of 8T and 9T SRAM cells using CNTFET Technology

Physical channel length (L_channel) = 18.0nm The thickness of high-k top gate dielectric material (Tox) = 4.0nm Chirality of tube (m, n) = (19, 0)

CNT Pitch = 10nm The path of the p+/n+ doped CNT = 10.0nm

The working function of Source/Drain metal contact = 4.6eV CNT work function = 4.5eV

The sizing of a CNFET is same as to adjusting the number of tubes. In this 8T CNTFET SRAM Cell Circuit design we have chosen 3 tubes for M1, M2 and M5 transistors, 1 tube for M4 and M7 transistors, 8 tubes for M3 transistor and 6 tubes for M6 transistor for proper functionality of the cell. Because of the asymmetry of the proposed 8T cell, the read path when Q ="1", represents the worst case read delay. The read cycle improvement is based on two aspects of the memory cell operation. First to pre-charge 'Read Bit' line irrespective of the activity of the 'Write Bit' line and secondly device sizing of the read zero path containing transistors M3 and M6, with the transistor M3 of the second inverter INV2 made 8 times mores to provide a fast path to ground.

For a write operation, the write delay is defined as the time between the activation 50% of 'Write Select' to when 'Q' is 90% of its full swing. The write delay is approximately equals the propagation delay of INV1 and INV2.
the write Dynamic power for a conventional 8T cell is independent of the input data, the activity factor of discharging the bit line α is equal to 1, because for any input data one of the bit lines is discharges. But this 9T CNTFET SRAM cell design uses only one bit line for writing and the discharging of the bit line 'Write data' depends on the stored data, so the activity factor α is definitely less than 1. Dynamic power reduction would result from the reduced switching activity during memory accesses. The 'Write Bit' line does not have to be pre-charged in preparation for the read operation and a write operation affects only a single bit line of the cell compared to both for the 8T CNTFET SRAM cell.

The 9T CNTFET SRAM circuit is successfully simulated using HSPICE and simulation waveforms are measured using the Avan waves. The Simulation waveforms for successive Writes and Reads are shown in Figure 5 and the simulation results of Dynamic Power and propagation delay are table 2. This circuit is verified by successfully writing the data "1010101" into the cell using 'Write Select' and 'Write Bit' signals, as shown by the waveform Q and correspond successfully reading of the data using the signal 'Read Select' as shown by the signal 'Read Bit' in Figure 5. The Dynamic Power and propagation delay pared to 7T

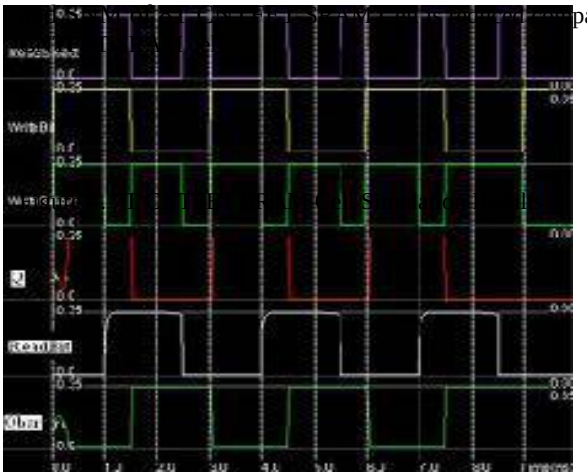

Figure 5. 9T CNTFET SRAM Cell Simulation Results
The simulation results of eight transistor cell of figure 3.11(a) shown in figures 5.1, 5.2 and 5.3 explain about the stability of the SRAM cell. The butterfly curve has shown that the square fitted inside the curves is very small, therefore the SNM is small.

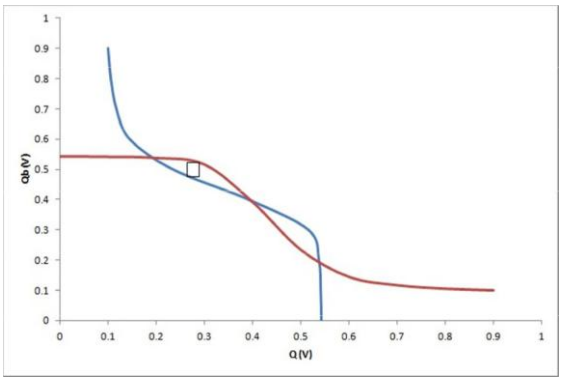

Figure 5.1: Eight transistor CMOS SRAM cell Read Static Noise Margin (SNM)

The plot of write Static Noise Margin depicts larger value of write SNM, as the size of the square is very large. So the write stability imparted by the curve is very high.

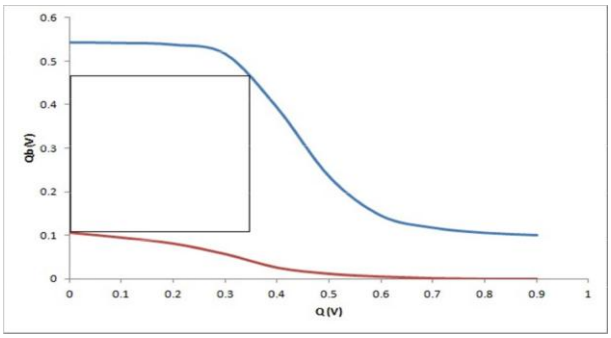

Figure 5.2: Eight transistor CMOS SRAM cell Write Static Noise Margin (WSNM)

The positive current peak value is small, means lower SINM and the negative peak value is also a small value indicating better write trip current.

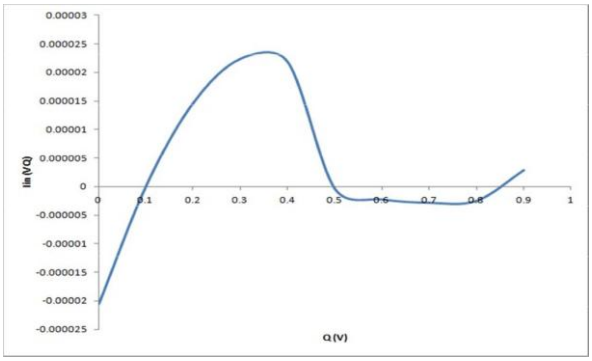

Figure 5.3: Eight transistor CMOS SRAM cell N-curve

Table 6.1: Eight transistor CMOS SRAM cell at 16 nm [17] and simulated 32 nm

16 nm Technology node at 0.4V power supply [17]		**Simulated 32 nm Technology node at 0.9V power supply**	
Parameters	**Values**	**Parameters**	**Values**
		SNM	45 mV
		SINM	23.5 µA
SNM	28 mV	WSNM	345 mV
WSNM	121 mV	WTI	3 µA
I_{READ}	974 nA	WTV	400 mV
Write delay	1.27 nsec	Write Delay	13.5 psec
		Write Power	150 µW

The 16 nm node and simulated 32 nm technology node parameters having supply voltage 0.4V and 0.9V have been compared in table 6.1.

Stability of the 9 Transistor CMOS SRAM cell shown in figure 5.4(a) is shown in figure 5.5.This graph obtained for read SNM is identical in shape with the other topologies but the size of the square in scibed inside it varies giving unique values of SNM for different topologies. Hence the noise tolerance for each topology is different.

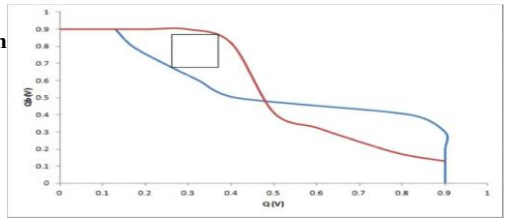

Figure 5.4: Nine transistor CMOS SRAM cell Read Static Noise Margin (SNM)

Writing into the cell takee more time than read, the inscribed square size for 9 transistor write SNM is very large so the data can easily be written into the cell. The internal node voltage 'Q' plotted in the X-axis and node voltage of 'Qb' node obtained in Y-axis.

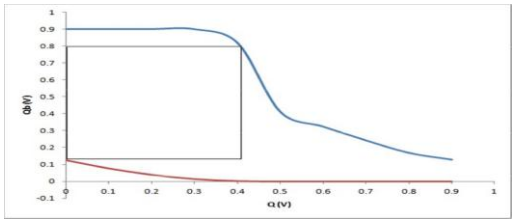

Figure 5.5: Nine transistor CMOS SRAM cell Write Static Noise Margin (WSNM)

The current peak obtained is high, so the SINM increases for 9 transistor cell.

The X-axis plots the voltage node 'Q' and Y-axis plots the current Iine across it.

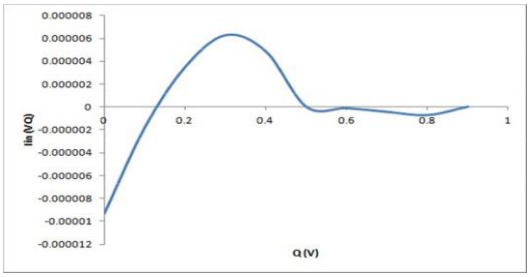

Figure 5.6: Nine transistor CMOS SRAM cell N-curve

Table 6.2: Nine transistor CMOS SRAM cell at 16 nm [22] and simulated 32 nm

65 nm Technology node at 1.0V power supply [22]		**Simulated 32 nm Technology node at 0.9V power supply**	
Parameters	**Value**	**Parameters**	**Values**
		SNM	163 mV
		SINM	6.3 µA
		WSNM	600 mV
SNM	270 mV	WTI	0.7 µA
		WTV.	400 mV
Write Power	35.1n W	Write Delay	9 psec
		Write Power	255 µW

The 65nm node standard results show high SNM and low write power to the simulated 32 nm node parameters.

V. CONCLUSION AND FUTURE WORK

The 3VL 8T STI is designed with 16 nm technology and their parameters are analysed. One bit memory cell is designed using 3VL 8T CNTFET SRAM and parameters are compared with 16nm 3VL 9T CNTFET SRAM,. It is found that the power consumed by 16nm CNTFET 3VL 9T memory is 12.02µW, which is much less than that of 3 VL 8T STI CNTFET SRAM and other memory cell. All this simulation results shows the most power efficient technology among the CMOS SRAM Cell. Thus as the channel length reduces the power consumption is also reduced. The later work consists of designing the memory with 14nm CNTFET technology, Cross bar memories with 14nm CNTFET has interesting applications. Carbon-based devices to replace silicon based MOSFETs in the future. In this paper 3VL 9T SRAM Cell is designed using CNTFETs at 16nm Technology to reduce power dissipation and to reduce the propagation delay. This 3VL 9T CNTFET SRAM Cell circuit uses extra one transistor compared to \conventional 3VL 8T SRAM Cell to reduce power dissipation. This circuit is designed and simulated.

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