FIR Filter Design Using Floating point Column Bypassing Technique

Jency Rubia J, Sathish Kumar G.A

Abstract*: This paper presents the design of floating point fixed-width multiplier using column bypassing technique for signal processing applications. The designed fixed-width multiplier provides less power consumption due to the reduction of switching activity in the operands of the partial products. This is the key element of the Multiply-accumulate (MAC) unit for enhancing its performance. The proposed MAC can be implemented in a FIR filter for DSP applications. To improve the accuracy of the FIR filter, various rounding methods have been used to solve the truncation error in the product. The power consumption is 10% lesser than conventional fixed-width multiplier and the accuracy also have been improved. The output response of the proposed filter will be simulated in the virtual software and hardware environment with the MATLAB software.

Index Terms*: Column bypassing technique, error reduction algorithms, FIR filter, Fixed-width multiplier, nearest rounding, wrap overflow.

I. INTRODUCTION

A Multiplier is the core of any digital signal processor unit. So the performance of the multiplier circuit will impact on the digital signal processor. Previously, the conventional multiplier was used in the signal processing applications. Nowadays the conventional multiplier can be replaced with various multipliers such as array multiplier, tree multiplier, booth multiplier, etc. since it requires much area and power. The traditional multiplier needs area and power for accumulating partial product bits. And also the processing speed will be less. To improve the performance of the DSP system, the fixed-width multiplier can be used. The theory of the fixed-width multiplier defines the number of bits of product is the same as that of the input. To achieve that the less significant bits (LSB) of the partial product bits will be truncated. So the area consumption and processing speed will be improved. Since the area got reduced, power consumption will be less in some manner.

In the last decades, many researchers were found various effective ways to enhance the performance of fixed-width multiplier and other multipliers. In paper [1], considered only the most significant partial products and the error can be rectifying by using correction constant. the choosing of correction constant can be calculated by rounding and reduction error [2]. In 1996, the area of the multiplier circuit can be reduced as in [3]. In [4] Jou proposed an extended work of kidambi and got 50% better result than previous. The multiplier is proposed with variable correction constant and error approximation is done by exhaustive approximation in [5]. The scientist Nicola was proposed optimal compensation function for reducing the error and also he suggested sub-optimal compensation function [6-8]. The previous work was extended in [9] and found an effective way to improve the multiplier accuracy namely uniform quantization and non-uniform quantization.

The proposed work involves the designing of floating point fixed-width multiplier using column bypassing technique for power consumption. The proposed MAC unit can be implemented in FIR filter for signal processing applications. The accuracy of the filter can be enhancing with the various error approximation methods. This paper organized as follows, section II clarifies the background knowledge of the basic concepts, section III describes the proposed work and section IV shows the simulation waveforms and the results. Finally, the conclusion and the future enhancement have been explained in section V.

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II. BACKGROUND

A. Fixed-width Multiplier

The fixed-width multiplier has the fixed number of output product bits as the input. The fig1 shows the general architecture of the fixed-width multiplier. From the architecture, we understood that the partial products are classified into various sections.

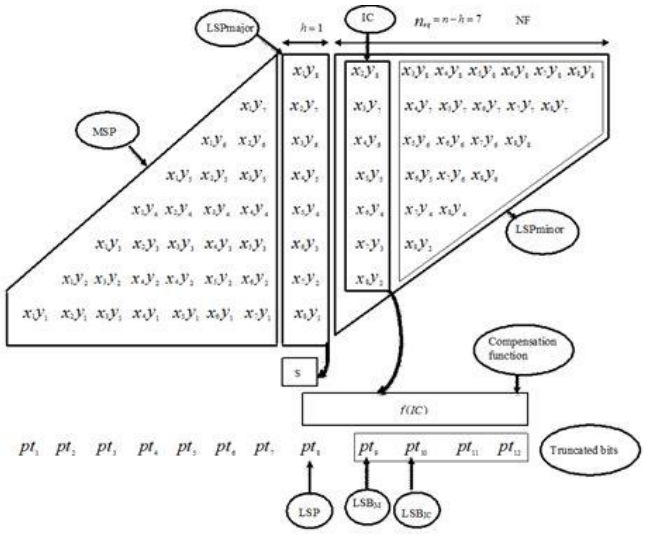

Fig 1. Architecture of Fixed-width multiplier for 8×8 matrix

The leftmost columns represent as Most Significant Part (MSP). And the rightmost

column refers to the Least Significant Part (LSP). The LSP part is further distributed as LSP_{major} and LSP_{minor} for the convenient computation of correction constant. The LSP_{major} considered the leftmost 'h' columns and the rest ($n_{eq} = n - h$) of the column denoted as Input Correction (IC). The Not Formed (NF) section is the truncated part of the multiplier for the fixed width of output same as the input. So there is a slight error in the result. To resolve the error many error approximation schemes were enabled[10-11].

B. Floating point Representation

The floating point number can be represented by IEEE 754 and IEEE 854 format in signal processing applications. The radix point in a floating point can vary its position relative to the significant digit of the number. IEEE 754 representation can be used widely in digital electronics. The features of using floating point representation are the usage of a wide range of numbers. It allows a large amount of numerical value to process than fixed-point and integer number representation. To maximize the speed and efficiency of the processor used the binary floating point format. This floating point representation used for computing real numbers[12]. The radix point in the floating point representation can be a float as the name indicates but in the case of fixed-point representation the radix point is fixed. The main advantage of using floating point will be the usage of a wide range of numbers and the design time of an algorithm will be less. The simplicity of the usage is better in floating point than fixed-point number format[13]. The IEEE 754 format for the single precision number is illustrated as in the table 1 below.

Sign bit (single bit)	Exponent (8-bit)	Mantissa (23-bit)
31	30 23	22 0

Table 1. IEEE 754 Format for Single Precision Number

C. Column Bypassing Technique

Low power consumption is the most inevitable factor in the digital signal processing world. The multiplier circuit is the most power consuming element in the DSP processors. If we minimize the power consumption of the multiplier, the power consumption of the DSP processors and communication system also get reduced.

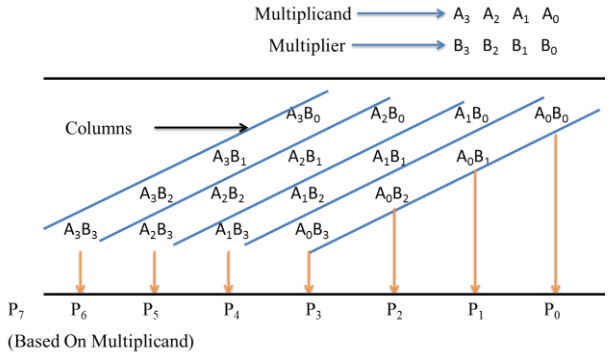

Fig 2. Architecture of Column Bypassing

This can be achieved by reducing the switching activity by area optimization. This can be attained by reducing the switching activity in the circuit design. This column bypassing technique reduces the switching activity by eliminating some of the columns of the multiplicand if zero. In the parallel array structure, the redundant signal switching causes the power dissipation. The general architecture of the column bypassing technique as shown in fig 2.

D. FIR Filter Design

FIR filter is a digital filter as it operates on discrete signals. FIR filter is used to implement any type of digital frequency response. Generally, this filter can be designed using a series of adders, multipliers, and delays[14]. The other name of the FIR filter is the recursive filter as they do not have feedback. In digital signal processing, the term FIR filter represent their impulse response has a finite time period. That means, the FIR filter settles to zero at a finite time period [15]. FIR filter involves higher order to realize the filter characteristics than IIR filter. But it has the advantage of better stability and assurance of the easy implementation of a linear phase filter. FIR filter has some specific properties that appropriate for multi-rate signal processing applications. The difference equation for the FIR filter is given by,

$$y[n] = h_0x[n] + h_1x[n-1] + h_2x[n-2] + \cdots + h_Mx[n-M] \quad (1)$$

where 'x' is the input digital signal and 'y' refers to the desired output signal. İnbetween the term 'h' denotes the filter coefficients for 'n' number of samples[16]. This equation can be explained in terms of graphical representation below as shown in figure 3. İt consists of a series of adders, multiplier, and delays.

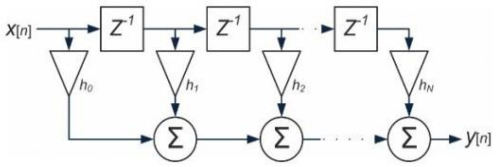

Fig 3. Block diagram of the FIR filter

III. PROPOSED WORK

A. Block Diagram

Any type of signal is fed to the FIR filter for processing. It can be an audio signal, image signal or video signal. In this research work, the input floating and fixed point input signal is superimposed with the white noise. The combined signal is given to the FIR filter for computation. Here, bypassing technique has been employed in the filtration process. The block diagram of this proposed work is depicted in fig 4.

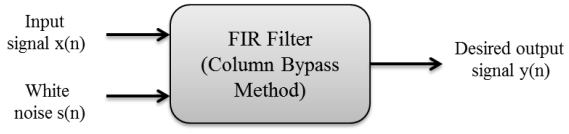

Fig. 4. Block Diagram of the FIR filter process

From the above figure, the complex input signal ($x(n)$) and the white noise ($s(n)$) added and forms superimposed signal ($b(m)$) and the desired

output is ($y(n)$)

B. Flow Chart

This work can be separated into three modules namely floating point analysis, fixed-point analysis, and real-time environment. Figure 5 gives the entire workflow of the proposed work. The floating point signal analysis involves the complex input signal which has the real and imaginary parts. The input signal requires quantization for the signal conversion. The proposed system follows 14-bit quantization and the general representation is as follows.

$$\varphi_t = \frac{(\text{input signal}) \times 2^{14}}{2^{14}} \quad (2)$$

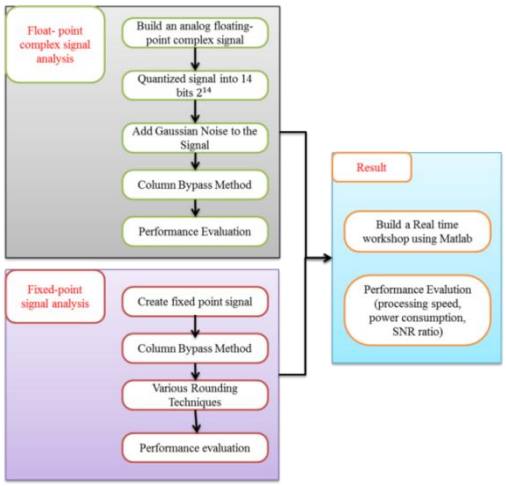

Fig. 5 Workflow of the proposed system

The fixed point signal used to store a particular number. To modify the signal into fixed width, it divided the given signal into 16-bit integer part and 15- bit fractional part. For quantization, nearest rounding method was very efficient. The overflow type is selected as wrap because of its reliability and security. In the fixed point toolbox active the product mode and sum mode to 'keep MSB'. The real-time environment is built by using Matlab toolbox. The parameters such as error, power, SNR, and speed of processing FIR filter has been measured in the software environment (non-compiled code) as well as in a real-time environment (compiled code).

C. Column Bypassing Technique

Column bypassing is the efficient method for area optimization technique thereby reducing the power consumption. In conventional parallel multiplier, the number of components is double the time of the number of inputs. For example, the m×n multiplier requires m×(n-1) adders and m×n gates[17-18]. Such that, the conventional multiplier compute zero component also. But it is an area and power consuming operation. It will lead to the unnecessary switching activity in the circuit. The key idea of the column bypassing is to disable the column of the partial products when there is a zero occurs in the multiplicand. Whenever the output bit is known, the elimination of the column will happen. Hence, mute some of the columns in the partial products when the multiplicand is zero. Column bypassing technique does not need the extra correcting circuit. The design of a modified full adder circuit is simple compared to the row bypassing. The general equation for the product of the multiplier is,

$$P = \sum_{i=0}^{n-1} \sum_{j=0}^{n-1} (a_i, b_j) 2i + j \quad (3)$$

Let us consider the multiplicand 'A' is 1 0 1 0 and multiplier 'B' is 1 1 1 1. Apply these numbers to the column bypassing architecture as in figure 2. The first partial product comes as it is. Then the second partial product bit forms using two full adder circuits. It performs $a_1 b_0$ and $a_0 b_1$. Here $a_0 = 0$, so need not to compute the second element b_1. Thereby eliminates one full adder circuit. Then, the third column represents $a_2 b_0$, $a_1 b_1$, and $a_0 b_2$. In this product bits, other than $a_1 b_1$, all are disabled. So it can save two full adders. The element $a_2 b_1$ and $a_0 b_3$ are inactive in the fourth column. But the carry bit is extended to the fifth column and here $a_2 b_2$ is disabling. The carry bit is fed to the sixth column and so on. If we noticed the structure of the internal architecture of this example as shown in figure 6, there is a diagonal arrangement in the partial product matrix.

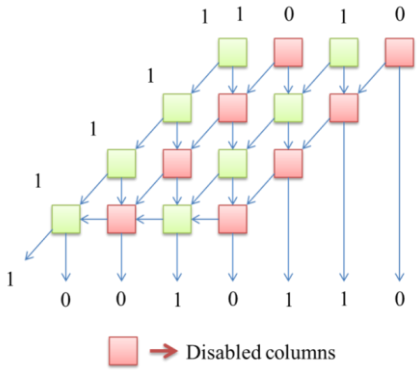

Fig. 6. The Internal architecture of the column bypassing

For better understanding, the dashed line in figure 4 represents the column of the partial product matrix. So called the technique column bypassing. The diagonals in the partial product matrix are denoted as columns of the matrix. So we can simply eliminate the diagonals. So that we can save eight number of full adders. Thereby saving a lot of area of the multiplier. The computation also takes a small amount of time. Most importantly we can reduce the switching activity of the components hence is leads to the less power dissipation.

IV. Simulation Results and Discussion

In this section explained the spectrum waveforms and the graphical representation of the signal analysis. The input filter coefficients of single precision were obtained from the Matlab toolbox. These filter coefficients (fixed and floating) was computed in the FIR filter by using column bypassing technique. The following section will clarify the simulated waveforms and the performance evaluation with the graphical demonstration.

A. Spectrum analysis for floating-point signal

The below figures 6 and 7 represent the spectrum diagram of the floating-point single precision signal in software and hardware environment or real-time environment. The software environment created by simulation of the circuit and the hardware environment made of virtual real-time environment created by the

microprocessor. In this waveform x-axis denotes frequency in hertz and y-axis denotes the scale.

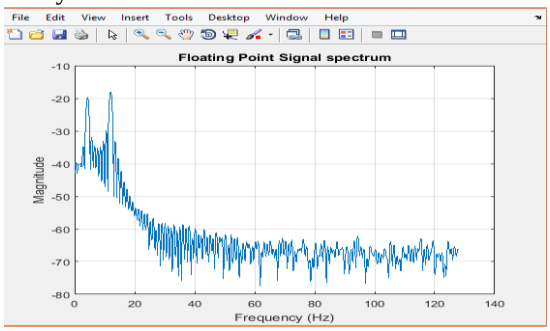

Fig. 6. Floating point signal spectrum (software)

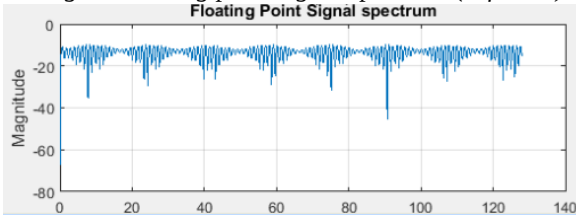

Fig. 7. Floating point signal spectrum (real-time)

B. Spectrum analysis for fixed-point

The below figures 8 and 9 represent the spectrum diagram of the fixed-point single precision signal in software and hardware environment or real-time environment. In this waveform x-axis denotes frequency in hertz and y-axis denotes the scale.

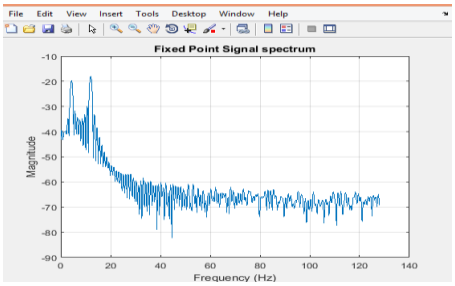

Fig .8. Fixed-point signal spectrum (software)

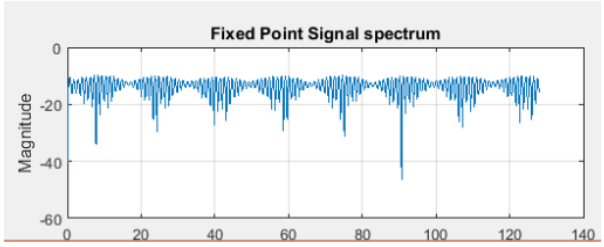

Fig. 9. Fixed-point signal spectrum (real-time)

C. Performance estimation Graph

The performance of the proposed filter can be improved by using different rounding method with the suitable selection of the overflow method. There are some parameters such as power, SNR, error, and speed which are influence the characteristics of the filter design. We analyzed such factors with respect to the column bypassing technique. The filter designed with the nearest rounding and the saturation type overflow gives better result in terms of power consumption. The accuracy of the filter is good when used rounding method with wrap overflow. The ceiling rounding offers the best signal to noise ratio. The computation speed of the filter process is better when used floor rounding with saturation overflow. Figure 10-14 shows the graphical representation of the performance of the proposed filter design.

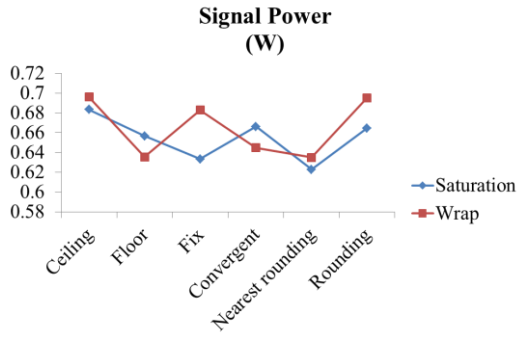

Fig. 10. Graph for signal power

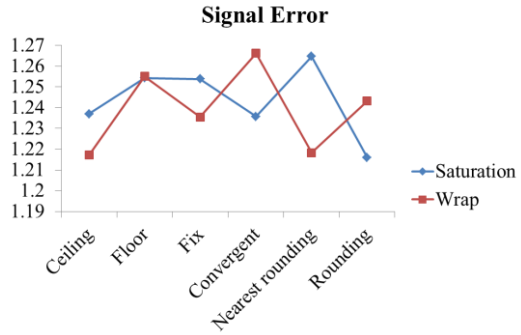

Fig. 11. Graph of Signal Error

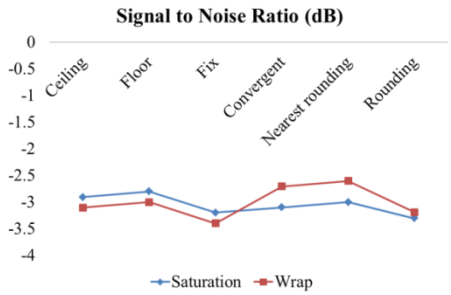

Fig .12. Graph for SNR ratio

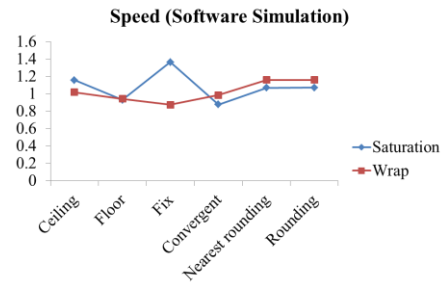

Fig .13 .Graph for software simulation speed

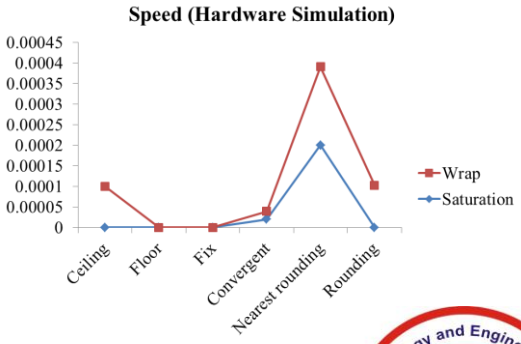

Fig .14. Graph for hardware simulation speed

V. CONCLUSION AND FUTURE WORK

The FIR filter is designed using bypassing technique and analyzed in both software and hardware environment. The overall power consumption of the designed filter can be minimized by the proposed algorithm. Since it optimized the area of the circuit. For performance evaluation, various rounding methods were employed. Finally, the nearest rounding method with saturation overflow provides the best result in terms of speed and error. The simulation waveforms are created by Matlab software. In the future, this work can be extended to implement the designed filter in FPGA for VLSI signal processing applications.

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