Quantum Dot Gate FET Based Multi-Value Logic Sequential Circuits

A. Phani Kumar, E. John Alex

Abstract— The design of multi value logic sequential circuits based on QG-FET (Quantum dot Gate Field Effect Transistor) is discussed here. The QG-FET produces an intermediate state in between the two stable states(i.e.) ON & OFF, this is happening due to change in the threshold voltage over this range. The design of various sequential circuits using QDGFET which includes ternary D-flipflop and ternary right shift register is discussed. The proposed design of sequential circuits using QDGFET results an improved circuit parameter and less circuit elements in the implantation. The three state QG-FET will increase the bit handling capability of the device due to increase in number of states. So that, with less circuit elements at a time we can handle more number of bits.

Keywords: -- QG-FET or QDGFET(Quantum Dot Gate Field Effect Transistor), MVL (multi value logic), Ternary D-flip flop, Ternary right shift register.

1. INTRODUCTION

The present digital logic exploits binary logic for computation. The Digital equipment designed based on binary logic have the advantages of being low cost, consuming less power and are very easy to implement. But currently, the designs with binary logic have reached saturation [1]. Hence multi valued logic (MVL) systems came into picture. These systems having radix more than 2 (i. e. binary system). The main advantage of MVL systems are that more information can be passed over channels and interconnection problems on the chip can be reduced [1].

The importance of ternary logic has been noted by many researchers [2]. Using CMOS technology, implementation of MVL has two main types: current-mode and voltage-mode. There are advantages of current-mode circuits but the disadvantage is high power consumption is occurred due to constant current flow. The advantage of voltage mode of M.V.L. circuits is low power dissipation. Because of reduced interconnections, electronic circuit implementation is simple and cost estimation ternary logic is more attractive than other types of MVL.

In QG-FET (Quantum Dot Gate Field Effect) Transistor, quantum dots are present on top of gate region which produces an intermediate level in between two standard levels. The resonant tunneling of charge carriers from inversion channel to quantum dots on the top of gate region can explains the generation of this intermediate state. On the gate region the quantum dots are cladded, due to this charge leakage is very small for this device, and giving stability to the intermediate state which is generated between its LOW and HIGH states. The QDGFET can be fabricated using existing process also.

Quantum dot layers and gate insulator thickness which are present on the top of gate governs the threshold voltage of QDGFET. The main circuit element used in this work is a QDGFET which generates 3 levels in its transfer characteristics as given in [2]. Ternary logic circuits can be designed using QDGFET in the same way as they are with CMOS, reducing complexity of design to develop the ternary circuits.

Based on the design, a ternary system has significant advantages such as a decrease in the number of inter-connections demanded in the implementation of logic circuits reducing chip area, lower memory requirement and higher data throughput.

The most common memory element used in today's world is binary D - Flip Flop and we want same popularity in the case of ternary D - Flip Flips in near future.

II. QUANTUM DOT GATE- FIELD EFFECT TRANSISTOR

A QG-FET exhibits transfer characteristics of three states, unlike from a conventional F.E.T. In QG-FET, on the top of thin insulator SiOx cladded Si or (GeOx cladded Ge) quantum dots are self-assembled [7, 9]. Like normal FET the source and drain regions in QG-FET are also formed. A lattice matched epitaxial layer of high-κ dielectric or HfO2 or SiO2 can be used as layer of gate tunnel insulator. Unlike floating gate Quantum dot non-volatile memories, three-state QDGFET devices do not have a layer of thick outer control gate insulator and the charge is permitted to escape the dot via tunneling through very thin SiO2 cladding layer around the silicon. In add to that, QG-FETs have minimum of two cladded quantum dot layers separated by a thin barrier which permits the tunneling of electrons. QDGFET structures exhibits the tri state behavior without an outer control gate insulator.

We know that QG-FET produce an intermediate state in its transfer characteristics because of presence of quantum dots in the gate region. The occurrence of this intermediate state can be explained by the transfer of the channel electrons to one of two quantum dot layers which

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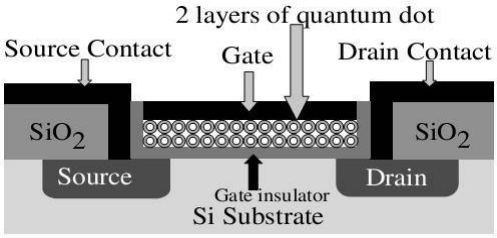
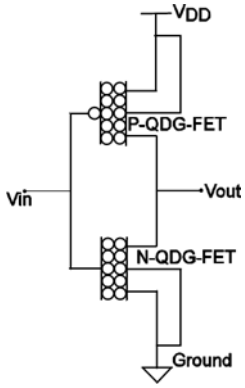
increases threshold voltage.

This increase in threshold voltage (VTh) compensates the raise in the gate voltage (Vg), thereby keeping the Drain Current approximately constant. The rate of electron transfer from inversion channel to quantum dots & resonant tunneling across quantum dot layers determines the range of gate voltage over which the behavior is observed. Below Diag: -1 shows the cross sectional schematic of a QG-FET.



Diag-1: Cross sectional Schematic of QG-FET

The QG-FET's effective threshold voltage is divided into 3 regions, ON state, Intermediate state and OFF state corresponding to the transfer characteristics. Initially as the gate voltage increases, the QDGFET's threshold voltage is same as a normal FET's threshold voltage, represented with VTh. Later when the gate voltage increases through a range of voltages Vg1 to Vg2, the threshold voltage varies linearly with respect to gate voltage. This change is controlled by the parameter 'α'. The model works like a conventional FET with α=0 and with α= 1 the model expresses the characteristics of QG-FET. The parameter α depends on the size and number of quantum dots which can be controlled at fabrication time, and as a result change the quantum dot gate's charge. The gate voltages Vg1 and Vg2 are also determined at fabrication time. The below diagram-2 shows the circuit diagram of a standard test inverter using QDGFET.



Diag-2: - circuit diagram of STI using QDGFET

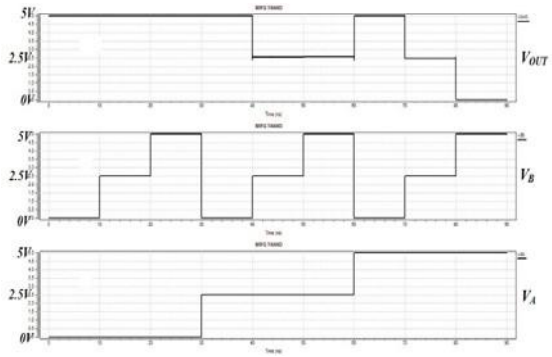
III. TERNARY D-FLIP FLOP

In digital systems, Ternary D-flip flops using QDGFET are used instead of binary D- f/f The binary D f/f operation & logic diagram can be easily observed in the literature. The ternary D - Flip Flops are produced by replacing the binary NAND gates with ternary NAND gates and the binary NOT gates with simple Standard Test Inverter (STI). The ternary logic operation of binary logic gates is presented in [1]. The truth tables and output waveforms for both the ternary NAND and ternary STI (Standard Test Inverter) are shown in Table I, Diag: - 3 and Table II, Diagram: - 4 respectively.

For ternary D - Flip Flop using QDGFET, the information is in ternary form. The low and high logic levels are represented by 0logic(0V) and 2logic (5V) respectively. The intermediate logic is 1logic (2.5V).

INPUT A	INPUT B	OUTPUT
0	0	2
0	1	2
0	2	2
1	0	2
1	1	1
1	2	1
2	0	2
2	1	1
2	2	0

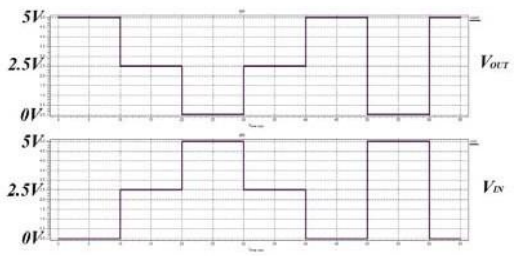
TABLE-I: Truth Table for Ternary NAND with Two Inputs



Diag:-3: Ternary NAND Gate Input-Output Waveforms

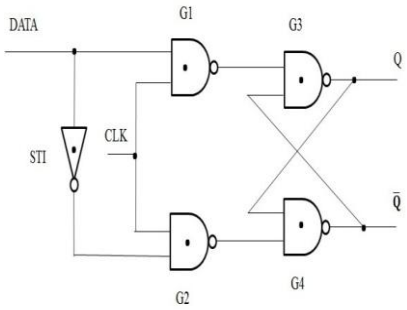
INPUT	OUTPUT
0	2
1	1
2	0

TABLE:-II: Truth Table of Ternary STI

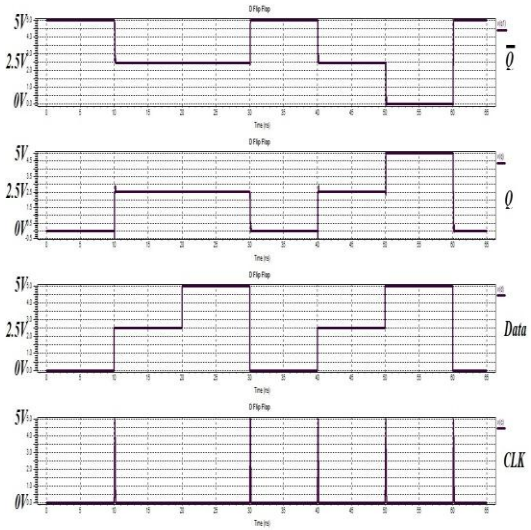


Diag: -4: STI Input-Output waveforms

The ternary D – Flip Flop with a clock spike pulse can transfer the information whenever the clock pulse goes from low to high (i.e., +ve edge). The circuit is formed with ternary NAND gates which replaces the binary D- f/fs & the binary NOT gates with STI as shown in Diag: -5. The input to ternary D - Flip Flop are clock(CLK) input and data input, whereas the outputs are Q & . The CLK signal is in binary clock spikes form and logic levels are represented with 0V and 5V. The ternary D - Flip Flop triggered on raising edge of the binary clk spike circuit's truth table is shown in Table III and the results of simulation are presented in the Diag: -6.



Diag-5: Ternary D – Flip Flop



Diag: -6: Input and Output Waveform of a Ternary D – F/F Using QDGFET

CLK	D	Q	$\bar{Q}$
0	X	No Change	
0-2	0	0	2
0-2	1	1	1
0-2	2	2	0

TABLE-III: Truth Table of Ternary D – F/F.

The performance parameters of multi valued D-f/f using QG-FET are shown below table-IV. It shows the critical delays for ternary D-flip flop from input to Q, input to $\bar{Q}$, the average power dissipated (µW) and Power Delay Product (J).

Delay (psec)		Average Power Dissipated (µW)	Power Delay Product (PDP) (J)
Input to Q	Input to $\bar{Q}$		
70.864	75.57	22.24	1.57601×10^{-15}

TABLE – IV: Performance Parameters of Ternary D – F/F

The power dissipation of ternary D-f/f is maximum when the input is 2.5 because the current is at its peak value here. The average power dissipated in Ternary D – Flip Flop is 22.24 µW which is lesser when compared with reported circuits in the literature. The Power Delay Product (PDP) for Ternary D – Flip Flop is 1.57601×10^{-15} J.

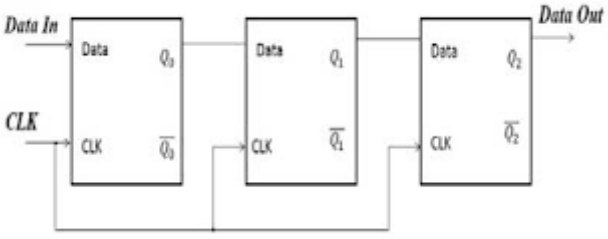
Input Capacitance (ff)	Output Capacitance (ff)	
	across Q	across $\bar{Q}$
660.83	279.77	276.24

TABLE-V: Input and Output Capacitance of Ternary D – F/F

The input capacitance of Ternary D – Flip Flop is found out to be 660.83 ff whereas the output capacitance is 279.77 ff and 276.24 ff across Q and $\bar{Q}$ respectively.

IV. TERNARY RIGHT SHIFT REGISTER

One of the applications of Ternary D – F/F is Ternary Right Shift Register. The Ternary Right Shift Register is formed by substituting the binary D – F/Fs with ternary D – F/F, as shown in Diag: -7. The inputs to Ternary RSR (Right Shift Register) are clock and data, whereas the outputs are Q & $\bar{Q}$. The CLK signal is in binary clock spikes form and the logic levels are represented with 0V and 5V.



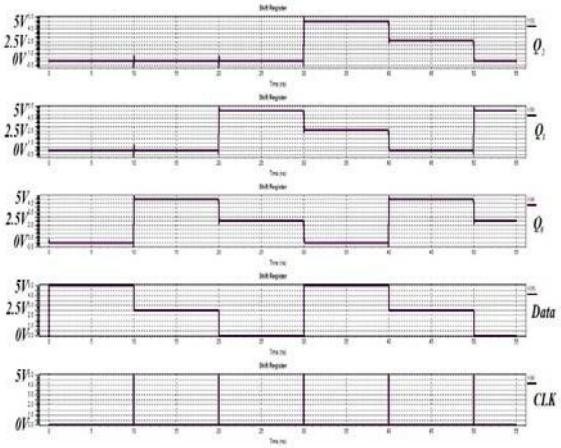
Diag: -7: Ternary Right Shift Register Using QDGFET Based on Ternary D-F/F.

The working of this Ternary Right Shift Register is described in the next paragraph. The RSR (Right shift registers) with binary clk pulse and right shift register with ternary clk pulse can be

designed based on the type of clock signal.

Initially, all outputs of Flip Flops are reset (i.e., made 0's). On first rising edge of CLK, the first D – f/f transfers the input data (5V) to the i/p of the second D – f/f whereas, the o/p of other D – F/Fs will be in their previous state. On the second positive edge of the clk pulse, the first D – F/F transfer the input data (2.5V) to the input of second D – f/f which transfers previous data (5V) to the i/p of third D – F/F whereas, the o/p of the third D- F/F will be 0V. For third positive edge of clock spike pulse the first D – F/F transfer the i/p data 0V to input of the second D – f/f which transfer previous data (i.e. 2.5V) to the i/p of third D – f/f and finally the o/p of the third D- f/f become 5V.

In this way, each Flip- Flop transfers the data towards the o/p on the successive raising edge of the clk signal. This is verified using truth table as shown in Table VI. Thus, input data is transferred to the output serially on successive rising clock spike pulses. The Ternary RSR (Right Shift Register) is shown in Table VI and the results of simulation are presented in Diag-8.



Diag:-8: Input and Output Waveform of a Ternary Right Shift Register Using QDGFET Based on Ternary D – Flip Flop

CLOCK	DATA	Q_0	Q_1	Q_2
Initially	5	0	0	0
0 – 5	2.5	5	0	0
0 – 5	0	2.5	5	0
0 – 5	5	0	2.5	5
0 – 5	2.5	5	0	2.5

TABLE VI Truth Table for Ternary Right Shift Register

The performance characteristics of Ternary Right Shift Register using QDGFET are shown in table VII. It shows the critical delays for Ternary Right Shift Register from Inputs to Q0, Q1 and Q2 are 28.14 psec, 28.52 psec and 28.55 psec respectively. Thus, the total delay across Input and output is 28.55 psec. Average power dissipated in Ternary Right Shift Register is 15.17468 µW which is very less when compared with other devices. The Power Delay Product (PDP) for this Ternary Right Shift Register is 4.3324×10^{-16} J.

Delay (psec)			Average Power Dissipated (µW)	Power Delay Product (PDP) (J)
Input to Q_0	Input to Q_1	Input to Q_2		
28.14	28.52	28.55	15.17468	4.3324×10^{-16}

TABLE-VII: Performance Parameters of Ternary Right Shift Register

Input Capacitance (ff)	Output Capacitance across Q_2 (ff)
219.55	84.256

TABLE-VIII: Input and Output Capacitance of Ternary Right Shift Register

Input capacitance of Ternary RSR is found out to be 219.55 ff whereas the output capacitance is 84.256 ff acrossQ2.

V. RESULTS AND DISSCUSSION

Here, the comparison for sequential circuits is done in terms of number of MOSFETs required. The comparison is done for the circuits of ternary D – flip flop and 3 – bit ternary right shift register. The circuits used to design a ternary sequential circuit are same as given in previous work. But the circuit with QDG-FET was found to be operating with less number of MOSFETs.

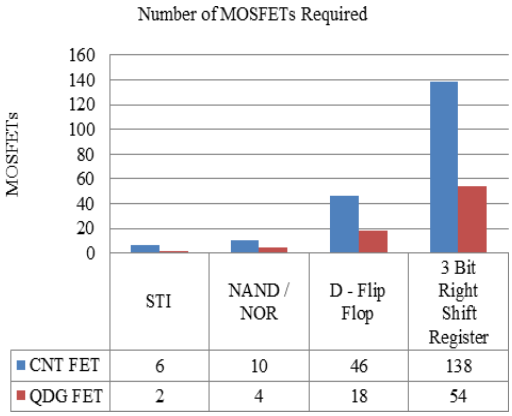


Fig. 9 Comparison Chart for Number of MOSFETs required

Thus, the number of MOSFETs required for each universal gate based on QDG-FETs are reduced by 60% and the number of MOSFETs required for designing ternary D – flip flop and 3 – bit ternary right shift register using ternary D– flip flop based on QDG-FETs are reduced by 60.86%.

VI. CONCLUSION

Design of Ternary D -F/F implemented with QG-FET, triggered on positive edges of a binary clock is presented here. The truth table, logic diagram & simulation results of this circuit are validated. For the QDG-FET based ternary D-flip flop with binary clock spike, the logic gates are need to be replaced with corresponding ternary gates and it is sufficient to obtain the correct operation of circuit.

Ternary Right Shift Register, which is an application of Ternary D - Flip Flop using QDG-FET with binary spike clock, is demonstrated here. The TT (truth table), logic diagram & simulation results of the Ternary Right Shift Register are also corroborated. The simulation results validate the proposed solution to obtain Ternary D – F/F and 3-bit Ternary Right Shift Register using Ternary D – F/F with triggered edge control. The designed Ternary Sequential Circuits using QDGFET successfully achieves low power consumption, less propagation delay and low Power delay product in the circuits such as Ternary D – F/F and Ternary RSR (Right Shift Register) using QG-FET.

Future work can be aimed at obtaining all other types of ternary Flip Flops with triggered edge control (such as T, SR, JK, and MS) Ternary Counters and Ternary Registers.

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