Research on Single Input and Regulated Multiple Output Isolated Dc-Dc Soft Deviceing Converter

J.Sivavara Prasad, K.R.L.Prasad, G.Nageswara Rao

Abstract— In this paper, in order to reduce the space occupied by individual DC-DC converter systems, the two-level single input multiple output isolated DC-DC converter is proposed for generating (2n-1) outputs where 'n' is number of legs. The first and second output voltages are controlled based on the control of duty cycles of two half bridge asymmetrical topologies and third output voltage is controlled based on phase shift control of two half bridge asymmetrical topologies. The efficiency of the proposed single input multiple output two-level isolated DC-DC converter has been compared with existing single input multiple output two-level DC-DC converter to realize the proposed work.

Keywords: Pulse width modulation, switching losses, Zero voltage switching dc-dc converter, controlled multiple output.

1. INTRODUCTION

The two-level single input multiple output isolated DC-DC topologies were proposed in order to reduce the space occupied by individual DC-DC converter systems. The dc–dc multiple-output topologies are mainly used in electronic equipments such as PC appliance, military and industrial applications. For designing the conventional dc–dc multiple output topologies, how to regulate multiple outputs is the main issue. In order to regulate all the output voltages against load and line variation in dc–dc multiple-output topologies, post regulation has been mainly used in [1]-[4]. There are various ways to make post regulation. In low output current applications, the linear voltage regulation is used. In high output current applications, the magamp post regulation proposed in [1]-[4], which makes the advantage of ability of handling high current and high efficiency. However, the large size and high cost of magamp post regulation has limited its application. Later, the synchronous-device post regulator has been developed in [5]-[9] is other way need for high output current applications, which utilizes the device as the post regulation. The synchronous-device post regulator has many features over magamp post regulation, such as easier remote on/off control implementation, easier over current protection, and smaller size.

DC–DC Multiple output topologies by pulse width and frequency modulations control were proposed in [10], in which the auxiliary output is controlled through the switching frequency and the main output is PWM controlled. The PWM frequency modulation control method is suitable to two-output applications only and due to variable-frequency control, the magnetic component is not easy to optimize. The other method used in dc–dc multiple-output topologies is parallel regulation in [11], it adds a adjustable voltage source in auxiliary circuit. By tuning the voltage of the adjustable voltage source, the auxiliary output is controlled. However, this method is very costly and precisely controlled. The PWM-pulse delay control technique was implemented to the dc–dc multiple-output topologies in [12]. It has been proved to have the feature of ability to produce controlled outputs but the structure is complicated and it require more number of control devices for multiple outputs.

In this research work, to overcome the limitations in the existing multi level outputs, the single input controlled two-level multiple output isolated DC-DC converter is proposed for generating (2n-1) outputs, here 'n' is number of legs. This topology is very simple and attractive due to less number of control devices.

This research paper is divided into three sections. The introduction is discussed in section 1. The characteristics of DC-DC multiple output converter, operating modes, realization of soft mechanism, design equations and results of two-level single input controlled multiple output isolated DC-DC converter are presented in section 2. The results and conclusion of the work are discussed in section 3 and 4.

2. ZVS MULTIPLE OUTPUT ISOLATED DC-DC CONVERTER:

The circuit diagram of single input controlled three output isolated DC-DC converter is shown in Figure 1. The second output is used for low voltage and high current mode of applications. The three output voltages are controlled based on the control devices in the primary side of inverter. The voltages V_{AB} & V_{CD} are the voltage across transformers T_1 & T_2 and the voltage V_{AC} is the voltage of transformer 3 & blocking capacitor C_b respectively. The output voltage V_{01} is controlled by the duty cycle control of asymmetrical half ridge converter S_1&S_4 and capacitors C_1& C_2. The output voltage V_{02} is controlled by the duty cycle control of other asymmetrical half bridge converter S_3&S_2 and capacitors C_3&C_4. The output voltage V_{03} is controlled based on phase shift of two asymmetrical half bridge topologies. All the control devices in the converter are operating under ZVS, hence this converter topology is suitable for high efficiency and high frequency applications.

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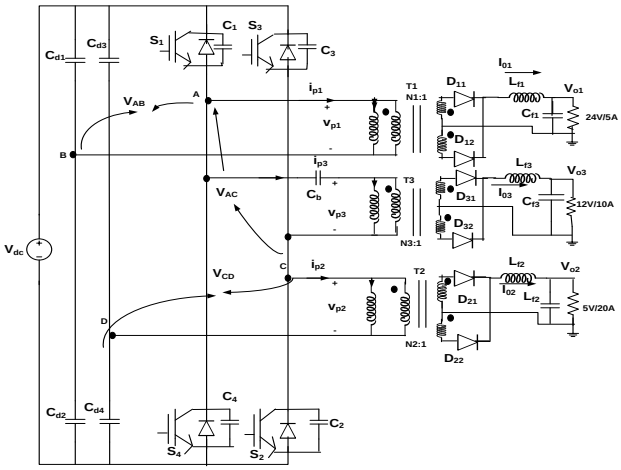

Figure 1: Controlled Three terminal outputs of ZVS isolated DC–DC converter

The Figure 2 shows the control signals of the multiple output converter. The three output ZVS DC-DC converter consists of two asymmetrical half bridge topologies connected to three single phase transformers.

Table 1 shows the comparison of proposed single input controlled three output isolated DC-DC converter with the conventional single input three output isolated DC-DC converter [5]. From table 1, it is clear that, the no. of control devices used in the proposed converter is less as compared to the existing converter and design of transformer is simpler in the proposed one. Hence, the deviceing losses are reduced and efficiency of the conversion system has been improved.

Table 1: Comparison of Proposed converter with other multiple output converter

Type of Element	Single input three output DC-DC converter topology [5]	Proposed single input three output DC-DC Converter Topology
Control devices	2n+1	n+1
Diodes	3n-1	3n+1
Gate-Amp	2n+1	n+1
Transformer Design	Complex	Simple
Deviceing Losses	High	Low
	Where "**n** "is the number of output voltages, n=3	

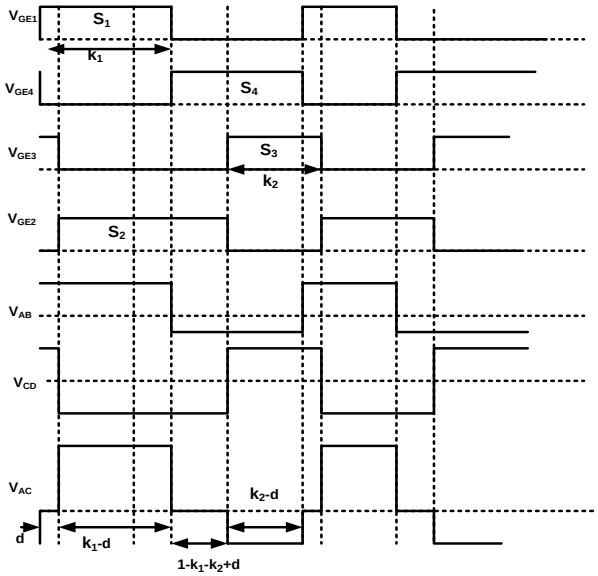

Figure 2: Control signals of the three output isolated DC–DC converter

2.1.Characteristics of the multiple output topologies:

The output voltage of the converter has been derived based on volt-second balance of output inductor.

The 1st output voltage V_{01} is

$$V_{01} = 2.V_{dc}.\mathrm{k}_1.(1-\mathrm{k}_1).\frac{1}{N_{\mathrm{T1}}} \quad (1)$$

Where V_{dc} is the input voltage, k_1 is the first asymmetrical converter duty cycle and N_{T1} is the turns ratio of transformer T_1.

The voltage gain of 1st output voltage to the input dc voltage is,

$$G_{01} = \frac{V_{01}}{V_{\mathrm{dc}}}.\mathrm{N}_{\mathrm{T1}} = 2\,\mathrm{k}_1(1-\mathrm{k}_1) \quad (2)$$

From the above equation it is clear that the voltage gain G_{01} is maximum at k_1=0.5.

The 2nd output voltage V_{02} is

$$V_{02} = 2.V_{dc}.\mathrm{k}_2.(1-\mathrm{k}_2).\frac{1}{N_{\mathrm{T2}}} \quad (3)$$

Where k_2 the second asymmetrical converter duty cycle and N_{T2} is the turn's ratio of transformer T_2.

The voltage gain of 2nd output voltage to the input dc voltage is,

$$\mathrm{G}_{02} = \frac{\mathrm{V}_{02}}{\mathrm{V}_{\mathrm{dc}}}.\mathrm{N}_{\mathrm{T2}} = 2\,\mathrm{k}_2(1-\mathrm{k}_2) \quad (4)$$

From the above equation, it is clear that the voltage gain G_{02} is maximum at k_2=0.5.

The third output voltage V_{03} depends on the duty cycles of two asymmetrical half bridge topologies k_1 and k_2. If k_1 is greater than k_2,

$$V_{03} = V_{dc}.(\mathrm{k}_1+\mathrm{k}_2-2.d).\frac{1}{N_{\mathrm{T3}}} + V_{dc}.(\mathrm{k}_1 - \mathrm{k}_2).(1-2.\mathrm{k}_1+2.d)\frac{1}{N_{\mathrm{T3}}} \quad (5)$$

If k_1 is less than k_2 then V_{03} becomes

$$V_{03} = V_{dc}.(k_1 + k_2 - 2.d).\frac{1}{N_{T3}} + V_{dc}.(k_2 - k_1).(1 - 2.k_2 + 2.d)\frac{1}{N_{T3}} \quad (6)$$

Where d *is* the phase shift of devices S_1 to device S_4 and N_{T3} is the turns ratio of transformer T_3.

Both the terms in equations (5) and (6) are the coefficients of $V_{dc}.\frac{1}{N_{T3}}$. Now for the given V_{dc} and turns ratios N_{T1}=4, N_{T2}=38 and N_{T3}=25, the term $(k_1 - k_2).(1 - 2.k_1 + 2.d)$ is very small compared to $(k_1 + k_2 - 2.d)$ term and hence it is neglected. So, the 3rd output voltage becomes,

$$V_{03} = V_{dc}.(k_1 + k_2 - 2.d).\frac{1}{N_{T3}} \quad (7)$$

2.2 Operating modes of the proposed converter:

The following assumptions are considered in the operation of the proposed converter.

- The duty cycles k_1 and k_2 are both near 0.5, so the voltage across C_b is $(k_1 - k_2).V_{dc}$ (when duty cycle k_1 is more than k_2) or $(k_2 - k_1).V_{dc}$ (when duty cycle k_2 is more than k_1) and is small compared to V_{dc} and therefore will be ignored.
- The control devices S_1& S_4 are operating under ZVS based on the usage of energy stored in output inductor of 3rd output. The control devices S_2 & S_3 are operating under ZVS based on the energy stored in leakage inductance of transformers T_2 and T_3.
- The voltage across capacitors C_{d1}-C_{d4} and C_b are constant by selecting large values of capacitances.
- The output inductors are large enough to make the output as constant current sources.

The voltage and current operational waveforms of proposed three output isolated DC-DC converter is shown in Figure 3.

Mode 1 (t0–t1):

Before mode 1, the transformers 1 and 2 are transmitting power to load through the devices S_1 and S_3, whereas the secondary output voltage of transformer 3 is freewheels. At the time t=t_0, the device S_3 is turned off under ZVS. The primary current i_{p2} and i_{p3} will charge the capacitor C_3 and discharge capacitor C_2. The primary voltage V_{AC} comes to positive, then the current in the diode D_{31} starts rising from zero value. The voltage across transformer T_3 is clamped to zero due to the conduction of diodes D_{31} and D_{32} simultaneously, as shown in the Figure 4.

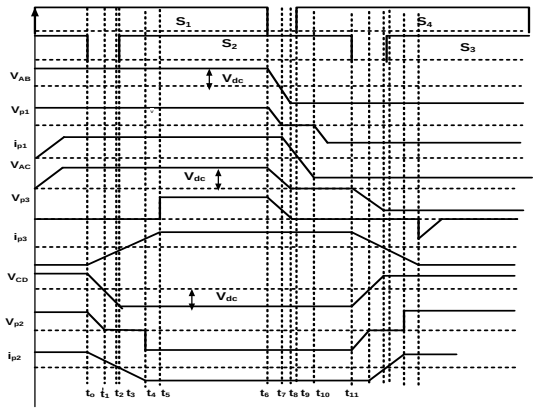

Figure 3: Voltage and current waveforms of three output isolated DC–DC converter

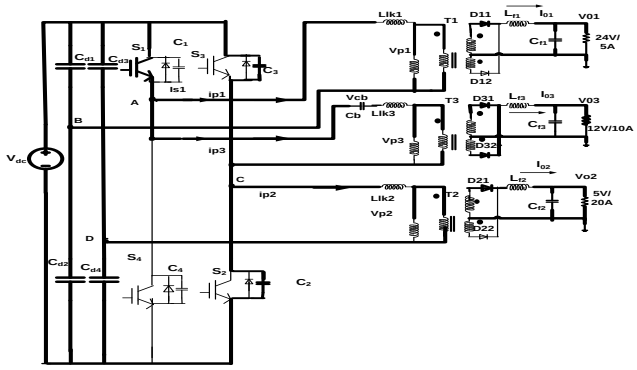

Figure 4: Mode '1' operation

Mode 2 (t1–t2):

At time t=t_1, the capacitor C_2 is discharged to $[k_2.V_{dc}]$. The voltage V_{CD} becomes zero if the voltage across capacitor C_2 is $[k_2.(V_{dc})]$. The current through diode D_{21} starts decrease and therefore diodes D_{21} and D_{22} turned on simultaneously and hence the 2nd transformer output voltage is clamped to zero as shown in Figure 5.

Mode 3 (t2–t3):

From figure 6, at time t=t_2, the capacitor C_2 is completely discharged to zero. So, the body diode of S_2 is on. Therefore the device S_2 is ready to function under ZVS at the ending of time t=t_2.

Mode 4 (t3–t4):

From figure 7, the device S_2 is turned on under ZVS at time t=t_3. The sum of primary currents i_{p2} and i_{p3} are flows through the device S_2.

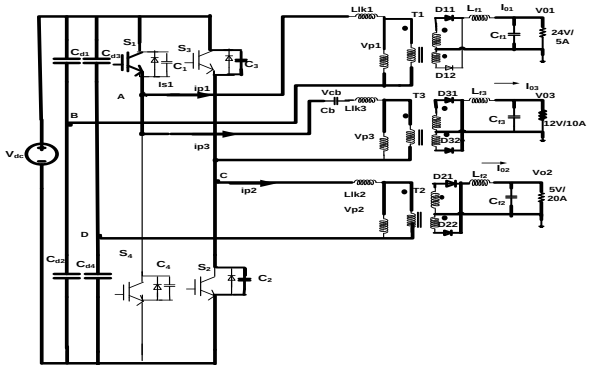

Figure 5: Mode '2' operation

Mode 5 (t4–t5):

From figure 8, during this mode, the current flowing through diode D_{21} rises to the second output current and current flowing through diode D_{22} falls to zero at time t=t_4.

Mode 6 (t5–t6):

From figure 9, during this mode, the current flowing through diode D_{31} rises to third output current and current flowing through D_{32} falls to zero at time t=t_5.

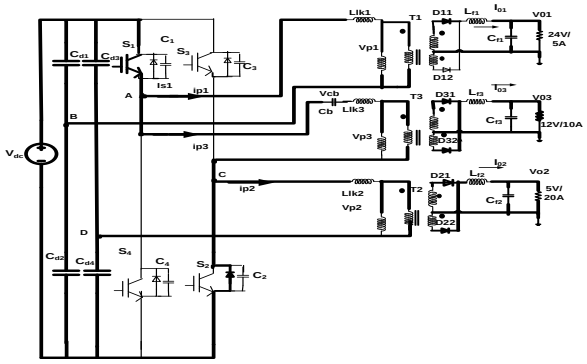

Figure 6: Mode '3' operation

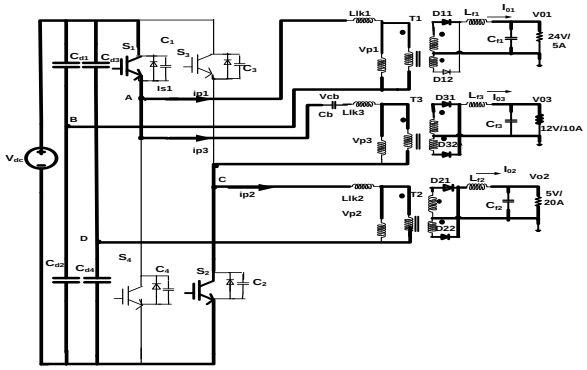

Figure 7: Mode '4' operation

Mode 7 (t6–t7):

From figure 10, the device S_1 is turned off under ZVS at time $t=t_6$. The sum of currents i_{P1} and i_{P3} will charge thecapacitor C_1 and discharge capacitor C_4.

Mode 8 (t7–t8):

The voltage across capacitor C_4 is discharged to $[k_1.V_{dc}]$ at time $t=t_7$. The voltage V_{AB} becomes zero due to voltage $[k_1.V_{dc}]$ across capacitor C_4. Thereby, the current flowing through diode D_{12} starts rising from zero value, whereas the current flowing through D_{11} starts falling. Hence the diodes D_{11} and D_{12} are conducting simultaneously and voltage of transformer 1 is clamped to zero, as shown in Figure 11.

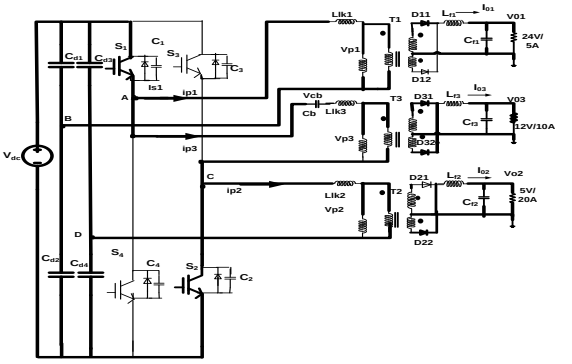

Figure 8: Mode '5' operation

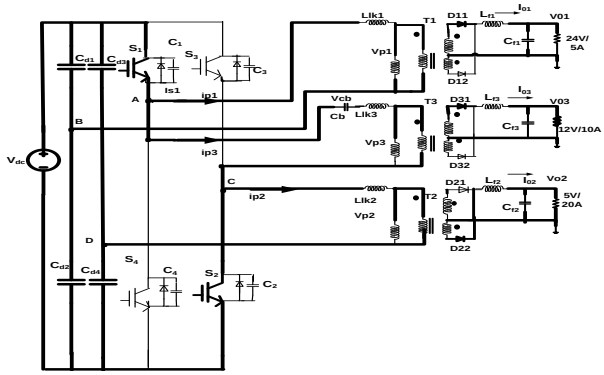

Figure 9: Mode '6' operation

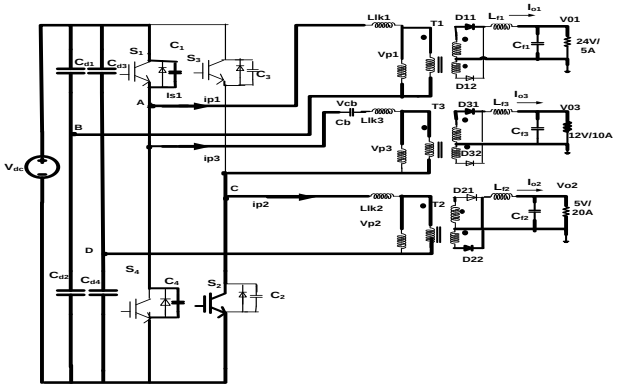

Figure 10: Mode '7' operation

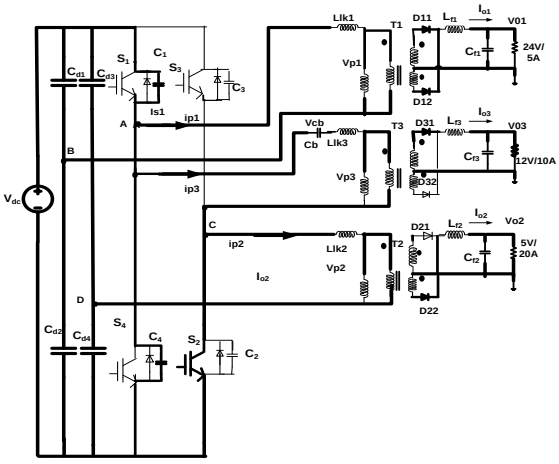

Figure 11: Mode '8' operation

2.3 Realization of soft switching:

The devices S_1 & S_4 are operating under ZVS based on the energy in the output inductance of third output. The control devices S_3 and S_2 are operating under ZVS based on energy stored in leakage inductances of transformers 2 and 3.

The following ZVS condition must satisfy

$$\left[\frac{1}{2}L_{lk2}.\left\{\frac{(2.I_{o2}.k_2)}{N_{T2}}\right\}.\left\{\frac{(2.I_{o2}.k_2)}{N_{T2}}\right\}+\frac{1}{2}L_{lk3}.\left\{\frac{I_{o3}}{N_{T3}}\right\}.\left\{\frac{I_{o3}}{N_{T3}}\right\}\right] > C_r.\{1-k_2\}.\{1-k_2\}\{V_{dc}^2\} \quad (8)$$

Where C_r is the parasitic capacitance, $C_1=C_2=C_3=C_4=C_r$.

2.4 Design equations:

The converter design indicates the design of values for C_{d1}, C_{d2}, C_{d3}, C_{d4}, C_1, C_2, C_3, C_4, C_b, L_{lk}, L_f and C_f. The output inductor should be large enough to make the output current

should be continuous throughout the switching period and leakage inductance of transformer must be small enough to make the less reset time.

The capacitors C_{d1}, C_{d2}, C_{d3} and C_{d4} must be large enough to make the voltage division must be maintained as constant even when the change of input voltage and voltage spikes produced by the device capacitances.

The resonant capacitor C_r ($=C_1=C_2=C_3=C_4$) must be selected in such a way that the minimum requirement for ZVS operation of control device during turn-off. The large capacitance is required to hold the device voltage closed to zero at time t_{fi}. The value of t_{fi} can be taken from the data sheet. The value of C_r can e calculated as,

$$C_r = \frac{t_{fi} * I_p}{V_{dc}} \quad (9)$$

The dc output filter elements are designed based on the following equations:

$$\Delta I_O = \frac{V_O * (1-k) * T_s}{L_f} \quad (10)$$

$$\frac{\Delta V_O}{V_O} = \frac{\pi^2 * (1-k) * f_r^2}{f_{sw}^2} \quad (11)$$

$$f_r = \frac{1}{2 * \pi * \sqrt{L_f * C_f}} \quad (12)$$

Where ΔV_O & ΔI_O are the acceptable ripple contents in the dc output voltage and current waveforms, V_O is the required dc output voltage, f_r is the resonant frequency, $f_{sw}=(1/T_s)$ is the switching frequency and k is the duty cycle of device.

3. RESULTS AND DISCUSSION

Figure 12 show the gate voltage, voltage across and current through device S_1 for the device transition period from off state to on state. When the gate pulse is given to S_1, then the device S_1 is turned on and current passes through the device from time t=7.3085ms, it is observed that the voltage across device is still zero, so no device power loss during transient instant from off state to on state and therefore ZVS is achieved for S_1. The ZVS is developed across S_1 due to clamped to zero by the body diode D_1. Hence, the device S_1 is turning on under ZVS during off to on transient period. The device is completely turned on at time t=7.3095ms, then the collector current of S_1 is starts rising from zero to 1.3A and the collector to emitter voltage of S_1 is clamped to zero due to its intrinsic capacitors C_1.

Figure 13 show the gate voltage, voltage across and current through device S_1 during on state to off state transition period. The gate pulse is given to S_1 at time 7.3475ms, but the collector current of S_1 starts falling from 6A to zero from the instant 7.348ms to 7.3485ms and the collector to emitter voltage of S_1 is still clamped to zero due to its intrinsic capacitors C_1. Therefore, the device S_1 is operating under ZVS during on to off transition instant. The device S_1 is completely turned off at time t=7.35ms, then the collector-emitter voltage of S_1 is starts rising from zero to rated input voltage due to charging of its intrinsic capacitor C_1. Thus, the device power loss becomes zero in on state to off state transition instant.

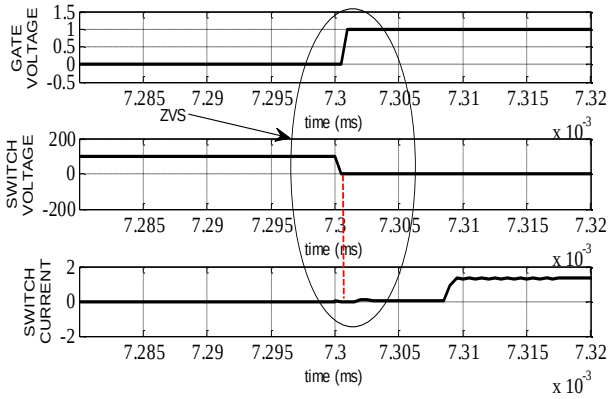

Figure 12: Gate voltage, voltage across and current through S_1 during OFF to ON

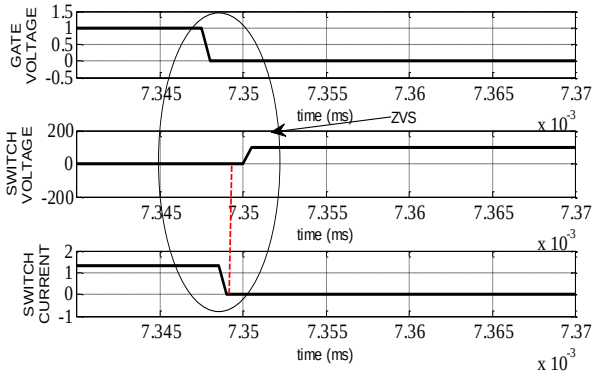

Figure 13: Gate voltage, voltage across and current through S_1 during ON to OFF

Figure 14 show the filtered three dc output voltage waveforms of the proposed converter. The dc filter values are designed in such a way that the ripple content present in dc output voltage waveforms become less than 3%. This converter converts input dc voltage of 100V into 24V, 12V and 5V respectively and these output voltages are reached to their steady state settling values at time t=0.45s.

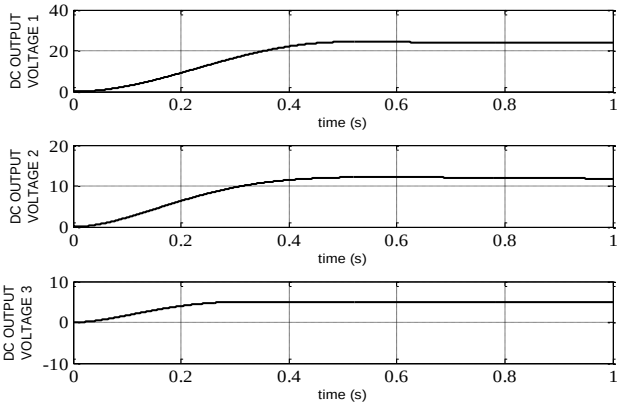

Figure 14: Three controlled dc output voltages with filter

Table 2 shows the % efficiencies of the proposed single input three output two level DC-DC converter for different load currents at the second load output with V_{o2}=5V.

Table 2: Comparison of efficiencies of proposed converter for various load currents at the second load output

S. NO	LOAD CURRENT (Amps)	OUTPUT POWER (Watts)	INPUT POWER (Watts)	EFFICIENCY (%)
1	5	25.7	33.16	77.5
2	7	35.2	44.38	79.3
3	9	44.7	53.21	84
4	11	54.2	62.87	86.2
5	13	64.1	73.25	87.5
6	15	73.9	82.75	89.3

4. CONCLUSION

In this paper, the two-level single input multiple output isolated DC-DC converter was implemented for generating three multiple controlled dc output voltages from single dc voltage source. This topology generates (2n-1) outputs, where 'n' is the number of legs. Due to soft switching mechanism, the proposed multiple output DC-DC converter gives higher efficiency even at high switching frequency. The operational modes, design equations and realization of soft switching of the proposed converter were discussed. The performance of the proposed was analyzed and results are quite satisfied.

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