

Design of Low Power and High Speed 4X4 Multiplier using Modified Column Bypassing Scheme for DSP Applications

E.Srinivas, N.Sharath Babu, G.Sreenivasa Raju

ABSTRACT--- In this paper a low power and high speed 4X4 multiplier is designed using CMOS Technology. The important factors in VLSI Design are power, area, speed and design time. Now-a-days, power and speed has become a crucial factor in Digital Signal Processor (DSP) Applications. However, different optimization techniques are available in the digital electronic world. The proposed approach a Low power and high speed Multiplier Design based on Modified Column bypassing technique mainly used to reduce the switching power activity. While this technique offers great dynamic power savings, due to their interconnection. In this work, a low power and high speed multiplier with Hybridization scheme is presented. This scheme is combination of booth encoder algorithm and column bypass technique is called modified column bypassing scheme. The simulations are performed in 0.18µm CMOS Technology in Cadence Virtuoso tools with operating voltage ±1.8v.

Keywords: Multiplier, CMOS, Column Bypassing, Digital Signal Applications (DSP), Row Bypassing, Booth encoder

I. INTRODUCTION

Multiplication is one of the basic building block in all digital processors ,digital filters ...etc. the basic operation of two number multiplication is first number is multiplicand and second number is multiplier; both can called factors [1]. In VLSI Integrated Circuit Design have two approaches, First is Analog IC Design and second one is Digital IC Design but digital IC design somewhat more accuracy compared to analog IC design. So most of the digital integrated circuits are popular as compared to Analog design [2]. Generally different types of multiplier architectures are available in the electronic world. The types of multiplier architectures are booth multiplier, Braun multiplier, Row bypassing multiplier and column bypassing multiplier,.etc. among all the multipliers column bypassing architecture are designed in this paper.

II. MULTIPLIERS:

The multiplier architecture can be generally classified in to the following categories: series, parallel and series-parallel. The series multiplier uses a successive addition algorithm. Parallel Array Multiplier Consider the multiplication of two unsigned n-bit numbers, where $A=A_{n-1}, A_{n-2}, A_{n-3}, \dots, A_0$ is the multiplicand and $B=B_{n-1}, B_{n-2}, B_{n-3}, \dots, B_0$ is the multiplier.

The product $P=P_{n-1}, P_{n-2}, P_{n-3}, \dots, P_0$ [5]. Array multiplier is close to regular architecture[3]. Multiplier circuit based on add and shifts algorithms. In digital electronic world Bypassing multipliers very much needed to save the power consumption of architecture.

III. BYPASS MULTIPLIERS:

The main motivation behind the realization of the Bypass Multipliers reduced area and fast speed [6]. While coming in to operation Types of Bypassing schemes are Row Bypassing schemes and Column bypassing schemes. Row bypassing technique is based on number of zeros in the multiplier bits. In this multiplier operation, some rows of adders in the basic multiplier array are disabling during operation to save the power [8]. The internal structure of the row bypassing adder cell is shown below Fig. 1. Row Bypassing Multiplier shown in Fig. 2. In this architecture contains 4-bit two numbers and 8 partial products. The inputs are $A_0, B_0, A_1, B_1, A_2, B_2, A_3, B_3$ and A_4, B_4 and partial products are $P_0, P_1, P_2, P_3, P_4, P_5, P_6$ and P_7 .

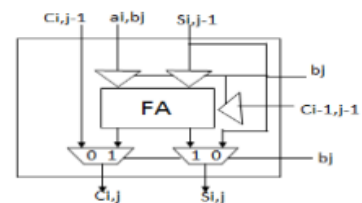


Fig:1 Structure of Row bypassing

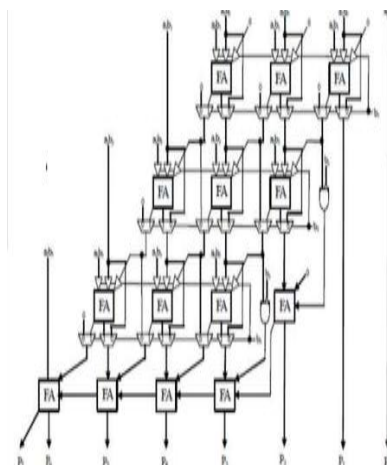


Fig: 2 Row bypassing Multiplier

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Fig. 3 shows the Column bypassing Multiplier Products architecture. It contains input 4-bit Two numbers and output have 8 partial product such as P0,P1,P2,P3,P4,P5,P6 and P7[9,10]. Hybrid bypassing multipliers can be verified by the number of zeros in either the multiplicand or multiplier to predict. Whether the operation completed in one cycle or two cycle.

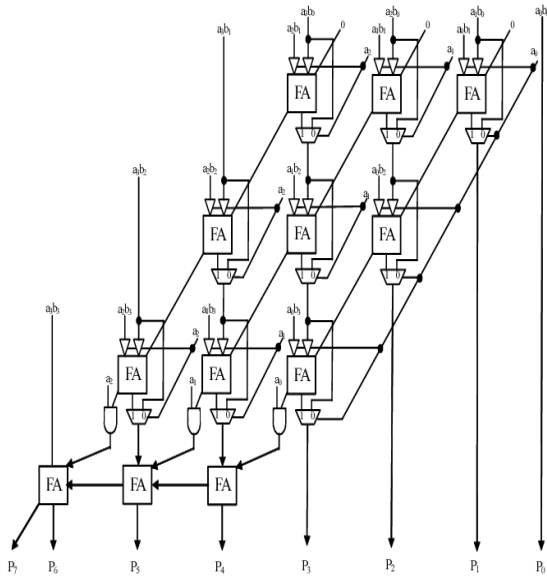


Fig: 3 Column bypassing Multiplier Products

A proposed architecture for implementing the 4-bit multiplier using modified column bypassing multiplier with is shown in Fig. 4. The modified column bypassing multiplier proposed the hybridization of booth encoding algorithm and

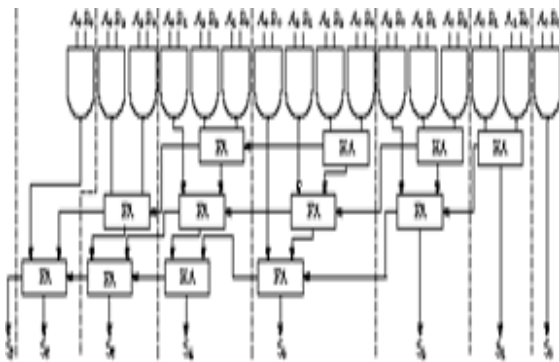


Fig: 4 a proposed circuit for implementing the 4-bit multiplier

Fig 4 shows the proposed 4-bit multiplier architecture. The sum and carry out is bottom architecture. The Partial products are accumulated (i.e. multiply and accumulate). Once the circuit first sum (S1) is the direct sum of two partial products, A1B0 and A0.B1. Second sum (S2) contains three partial product are added with this two adders and carry out from first sum (S1) Column is required. Third sum (S3) is a little bit complex. Why because two different carryout from previous column. Here three cascaded adders, two full adders and one Half adders required [11]. S4 requires three products and carry outs from S3. Similar

analysis applied to reaming sums such as S5, S6 and S7 in the multiplier architecture.

IV. SIMULATION RESULTS

The proposed multiplier and conventional multiplier comparison is made in terms of power consumption, power dissipation and delay. The designed circuits are drawn in cadence virtuoso schematic diagram and simulation are done in cadence analog Design Environment. The Results of proposed multiplier are compared with conventional design. This architecture useful to design multipliers such as 16-bit and 8-bit multiplication. The comparison of power consumption at different operating frequencies ranging from 1 MHz to 333.3 MHz is shown in Table 1.

Fig. 5 shows the schematic diagram of 2X1 Multiplexer. The basic operations of 2X1 multiplexer have two inputs, one selection line and one output. The schematic diagram drawn in analog design environment schematic editor.

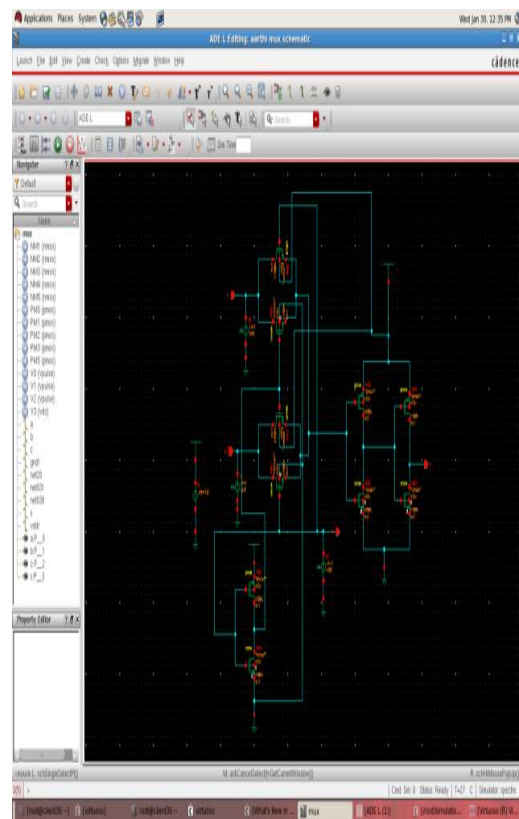


Fig.5 Schematic Diagram of 2x1 MUX

Fig .6 shows the 2x1 multiplexer output waveforms are simulated in cadence tools. The output wave forms are two input's, four combinations, two selection lines and one output are presented. The combination that is two inputs are zero and selection line is zero, the output becomes zero. If two inputs are one, the output is one. If input A becomes 1 and B Becomes 0, the selection line is zero the output is 1 and the selection line is 1 the output is 0. Generally multiplexer is also called as data selector. Why because the data selecting based on the selection lines. Multiplexer blocks are used in many digital design circuits.



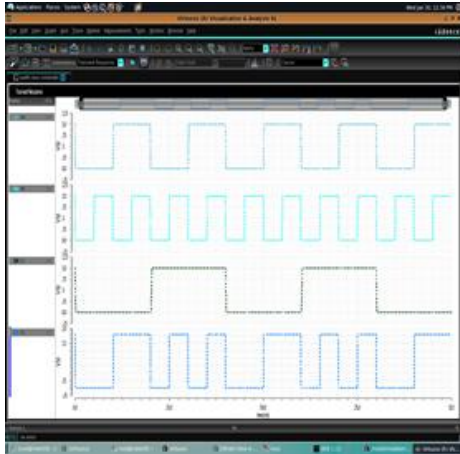


Fig 6. Output Put Waveform of 2x1 MUX

Fig. 7 Shows the Schematic Diagram of AND Gate, The basic operation of AND carries multiplication and one output.

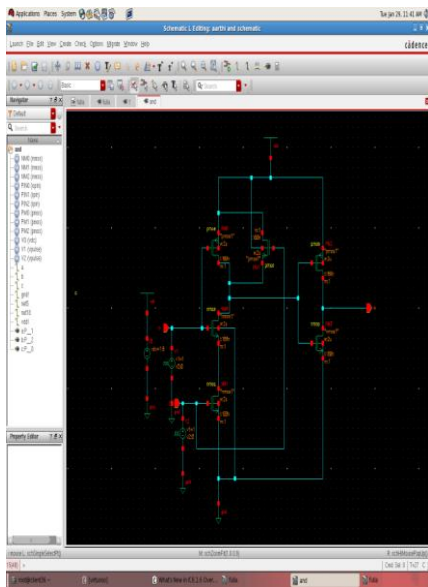


Fig.7: Schematic Diagram of AND Gate

Fig. 8 Shows the Output Waveform of AND gate, The gate contains two inputs and one output. For Example if input A and B are becomes zero the output becomes zero. If A and B becomes are one, the output becomes one. If any one of the input is zero the output becomes zero.

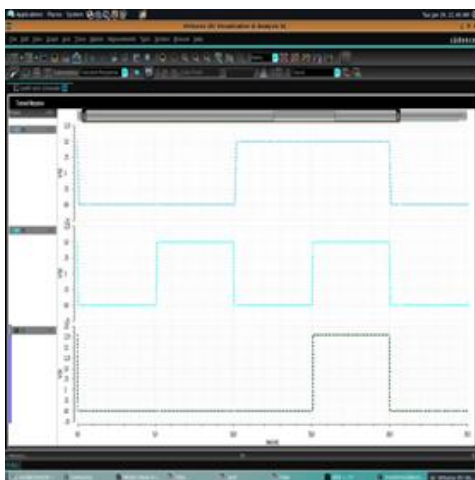


Fig 8: Output Wave form AND Gate

Fig. 9 Shows the Schematic diagram of OR gate, The OR Gate drawn in Analog design Environment In cadence tools. OR Gate contains two inputs and one output.

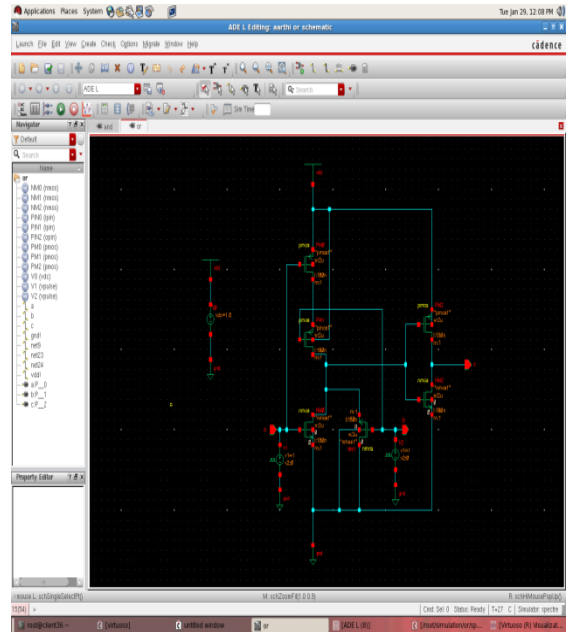


Fig 9: Schematic diagram of OR gate

Fig. 10 Shows the Output waveform of OR Gate. This Output window contains two input waveform and one output waveform. If Inputs A and B are zero, the output is zero. Otherwise the output becomes one.

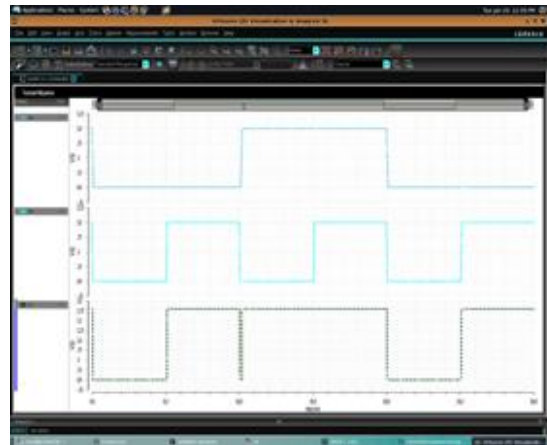


Fig 10: output waveform of OR Gate

Fig. 11 Shows the Schematic Diagram of XOR gate. The basic operation of XOR Gate is any one input is high the output is high. Schematic Diagram of XOR Gate is drawn and simulated in cadence tool.

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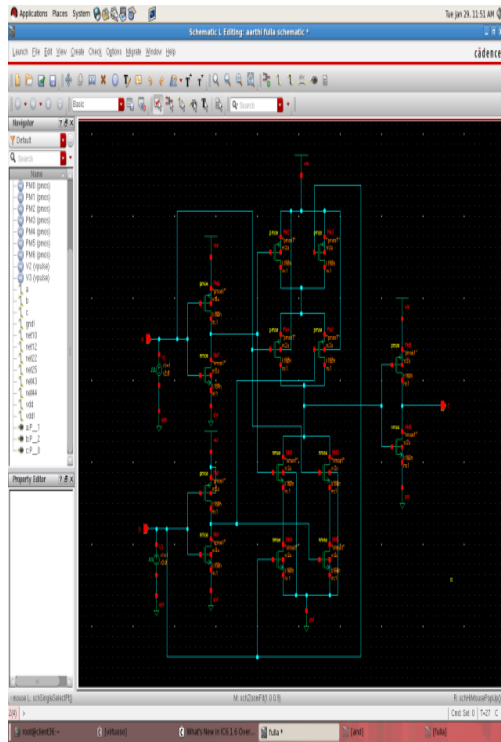


Fig 11: Schematic Diagram of XOR Gate

Fig. 12 shows the Output Waveform of XOR gate. The output waveforms have two inputs and one output.

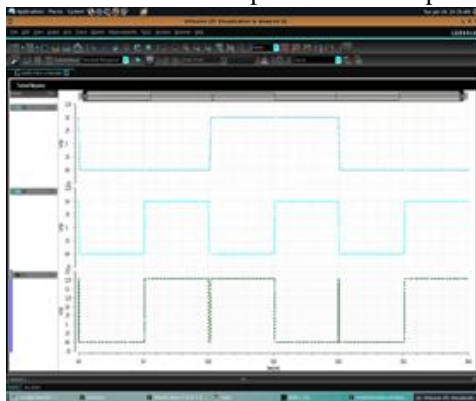


Fig 12: Output Waveform of XOR Gate

Fig. 13 Shows the Schematic Diagram of Proposed 4X4 Multiplier. The Schematic diagram drawn in analog schematic editor in cadence tools

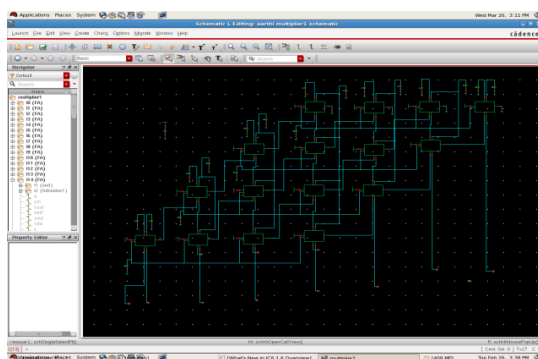


Fig 13: Proposed Schematic Diagram of 4x4 Multiplier

Fig. 14 Shows the Proposed output waveform of 4X4 Multiplier. The output window contains the waveforms of 4X4 multiplier.

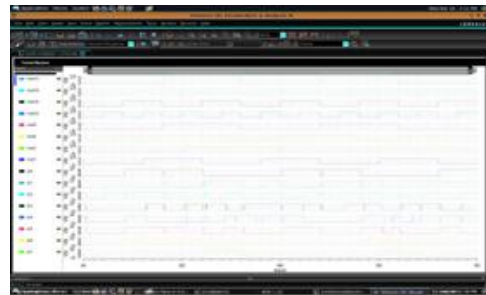


Fig 14: Output Wave form of Proposed 4x4 Multiplier

Fig 15: Power Consumption of Proposed Multiplier circuit. The proposed multiplier have power consumption is 3.4µwatts.

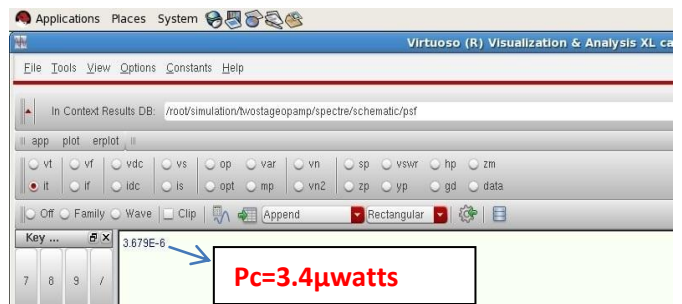


Fig 15: Power Consumption of Proposed Multiplier circuit

Table 1: shows the Comparison of Multiplier.

In Conventional Design, the power dissipation is 11.34nawatts, the power consumption is 94µwatts and delay is 23ns. While proposed design the power dissipation is 2.4nawatts ,power consumption is 3.5µwatts and delay is 10ns. Finally proposed design have superior results compared to Conventional design.

Table 1: Comparison Table of Multiplier Circuit

Parameters	Conventional design	Proposed design
Power Supply	1.8v	1.8v
Power Dissipation	11.34nawatts	2.4nawatts
Power Consumption	94µwatts	3.5µwatts
Delay	23ns	10ns

V. CONCLUSION

A low power, high speed 4x4 multiplier using a modified column bypassing Architecture is designed. This architecture achieved better results like reduces the power consumption and propagation delay. The Simulation results show that proposed multiplier facilitates reduction of power and area occupancy compared to conventional design. This method is valid for both signed and unsigned operands.



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