TIQ Flash ADC Design using a Low Power Multiplier Based Encoder

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Abstract: ***Threshold Inverter Quantization (TIQ) for applications of system-on-chip (SoC) depending on CMOS flash analog-to-digital converter (ADC). The TIQ technique which uses two cascaded CMOS inverters as a voltage comparator. However, this TIQ method must be created to meet the latest SoC trends, which force ADCs to be integrated with another electronic circuit on the chip and focus on low-power and low-voltage applications. TIQ comparator reduced the impact of variations in the process, temperature, and power supply voltage. Therefore, we obtained a higher TIQ flash ADC speed and resolution. TIQ flash ADC reduced / managed power dissipation. We obtain large power savings by managing the power dissipation in the comparator. Furthermore, the new comparator has a huge benefit in power dissipation and noise rejection comparative to the TIQ comparator [1]. The findings indicate that the TIQ flash ADC based on Modied mux attain heavy-speed transformation and has a tiny size, low-power dissipation and operation of low-voltage compared to another flash ADCs.***

Keywords: ***Encoder, Flash ADC, Threshold Inverter Quantization***

I. INTRODUCTION

According to the semiconductor roadmap [45], the minimum channel length of the transistor will be scaled down to 0.007 micro meters in 2018. In Furthermore to this downscaling, the current trend of system-on-chip (SoC) compels analog and digital integrated circuits (ICs) to be integrated on a individual chip called the complete SoC. There are currently several requirements on the full SoC in wireless and broadband communications – wireless networking (WLAN, voice / data communication), wired communication (WAN and LAN), and consumer electronics (DVD, MP3, digital cameras, video games, and so on). Therefore, as one of the blended-signal ICs, analog-to-digital converters (ADCs) must follow this full SoC trend. This section presents the challenges of developing ADCs and potential solid-state techniques for the full SoC trend.

A common encoding approach for thermometer code is the utilization of a full adder-based encoder [3]. It comprises of a full adder only. This full adder consists of low power based design and less area consume to chip level of the design full adder based and tiq based comparator will reduce noise linearity as effective way to reduced the leakage power.

The subthreshold voltage declines in successive nanometer technologies and has an associated effect of increased leakage current. High level integrated semiconductor solutions such as system-on-chip calls for data converters to be designed in the same technology the rest of the chip uses. At the same time, applications drive data converter development in such a way that while their linearity requirements are maintained, the power consumption has to be lowered, or their bandwidth needs to be wider. In an era of fast growing smart phone usage with ever faster communication speed, and of the emerging of wearable electronics and portable health care products, the world calls for lower power data converters designed in modern technologies. The proposed flash adc design architecture will reduce noise linearity, power and area of the design.

II. TIQ FLASH ADC

A Flash ADC comparator array analyzes the input voltage with a group of growing remark voltages. The outcome of the comparators shows the binary output code which is input for the encoder. The encoder is produce digital output based on the inputs.

The differentiate between TIQ method and standard flash ADC implementation method arises from how the remark voltage is set. A resistor array structure is used in the resistive flash ADC to create the remark voltage and a comparator cell array is utilized to evaluate the incoming voltage source along with the remark voltage to achieve the thermometer code. All comparator is intended to place the remark voltage with the ratio (W/L) internally in the TIQ technique. The TIQ technique uses as a comparator two pairs of cascaded CMOS inverters. This proposed technique must be developed in order to be better implemented in Soc functions. The TIQ method decreases the ADC power consumption and chip region compared to conventional flash ADCs. The Flash ADC design is faster compared to all flash adc and is also called parallel adc.

TIQ Comparator

The comparator is the most significant element of ADC design. Its role is to transform a Vin input voltage into a '1' or '0' logic by equating a Vref remark voltage to the Vin. If the Vin is higher than Vref, the comparator's output is '1' otherwise '0'. For comparison [1], CMOS switching voltage is replaced as a remark voltage.

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It comprises of two end to end CMOS inverters and are linked in a series connection with the similar width of channel ratio (Wn=Wp) in Figure 1. In the switching threshold point of a CMOS inverter, the output voltage is equivalent to the input voltage (Vin= Vout) and at this stage both nMOS & pMOS transistor always perform in a saturation region. By equating the equations we can obtain comparator threshold voltage Figure 3.

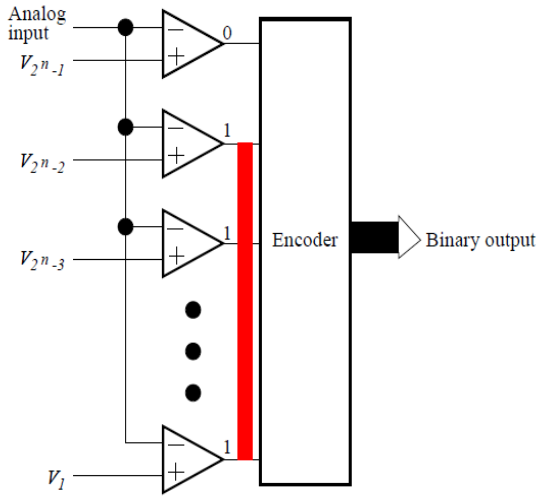

Fig. 1 Flash ADC

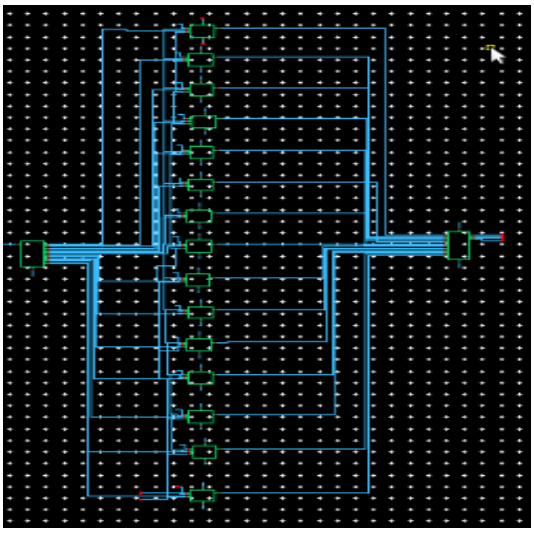

Fig. 2 TIQ Flash ADC

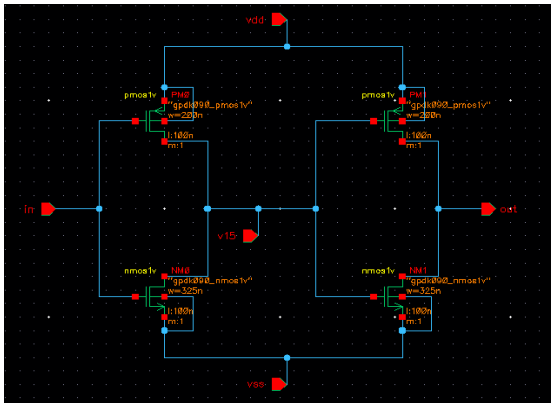

Fig. 3 TIQ Comparator

III. ENCODERS

We have several encoders to transform thermometer code to gray code.

A. Fat tree encoder

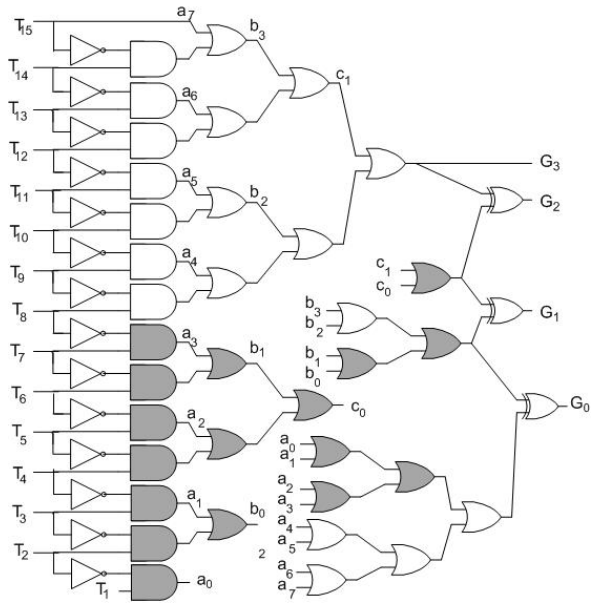

Fig. 4 Fat tree encoder

The Fat tree-based encoder considered as an effective method of renovating Thermometer code into Gray code. It acquires less region & delay when compared to the Wallace tree-based encoder. This encoder also shows a self-configured property Figure. 4 Indicates a fat tree encoder for 15-bit thermometer input code.

B. Full adder based encoder

In full adder based encoder we are using ADC with transmission gate and opamps to reduce the delay and power [2]. In flash ADC using opamps to make the power low and also to reduce the delay we are using as shown in the figure 5.

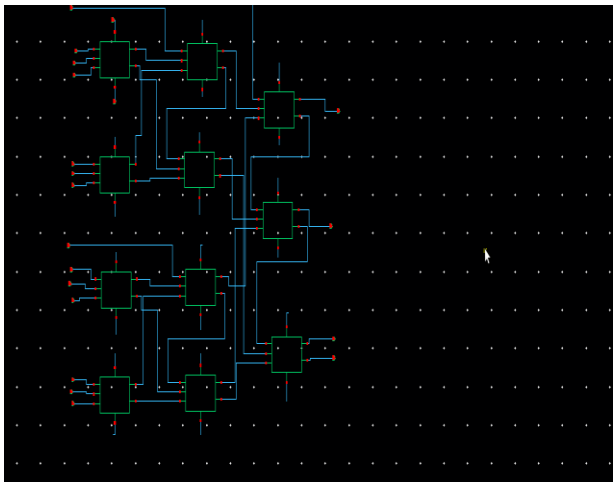

Fig. 5 Encoder using full adder transmission gates

C. Mux based encoder

A mux-based thermometer code for the encoder Gray code is suggested in [2]. This has high speed and small region compared to wallace and Fat tree based encoders. The realization of the 15-bit thermometer code input MUX based encoder is shown in Fig. 5

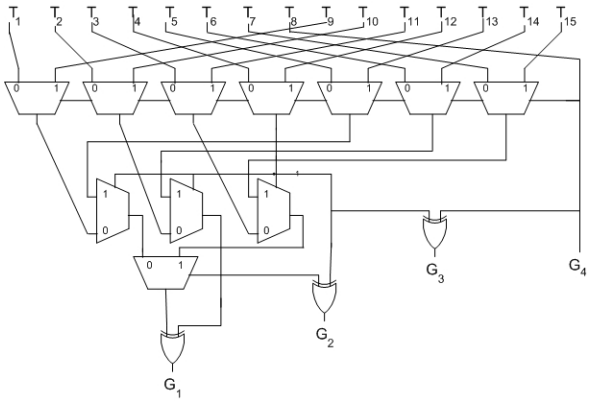

Fig. 6 Mux based encoder

Proposed 4 bit Mux based encoder

G4 = T8
G3 = T4T12

The suggested design for the 4-bit encoder architecture is shown in Figure 7 2:1, 2- XOR gate and MUX input form the fundamental components for the projected design. Gray code outcomes are applied using 2:1 MUX and 2-input XOR gates and also used to achieve the respective binary code. Here the input line '1' of a few of the MUXs is related to the ground end to diminish the number of Multiplexers and stop the additional inverters requirement compared to the present MUX-based design. The 2:1 MUX and 2 XOR input gates are implemented to achieve low power consumption in the transmission gate logic style.

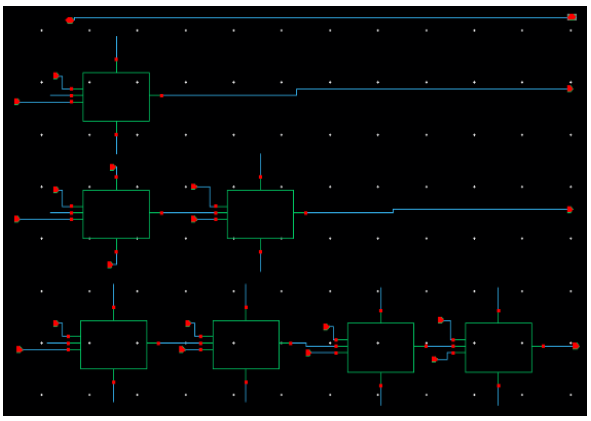

Fig. 7 Encoder using Proposed Mux based design

The gray code output G4 is equal to the thermometer code input T8. Therefore G3 is straightly linked to T8 and the G3 output code is acquired from the input codes T12 and T4. The input codes T4, T12 are used to achieve the corresponding gray code G1. T12 is used as the line of choice and T4 as the input to MUX 1. To attain the respective G2 gray code, T6, T2, T14, and T10 input codes are used. T14, T6 are often used as choice lines and T10, respectively T2 are used as inputs for MUX 2, 3. Using MUX 5,5,6,7, the G1-output code is obtained from the input codes T13, T15, T9, T11, T5, T7, T1 and T3. Using the entry of 2 XOR gates, the output binary code is acquired from the gray code. So you can use the same encoder.

The suggested design also benefits from self-configurable property. The 4-bit encoder can be transformed into a 3-bit encoder by allocating to '0' the larger order inputs T8-T15. Likewise, it can be transformed to a 2-bit encoder by allocating the T4-T15 inputs to '0'. For the lower resolution flash ADC, it is therefore possible to use the same encoder.

The design method enhanced the ADC's linearity over differences in the CMOS method, temperature, and power supply voltage. The modified mux based encoder overcame the speed limitation all type of encoders which is the potential bottleneck of high speed ADCs. In addition to improving the performance of the TIQ flash ADCs, this thesis proposed two modifications to the TIQ technique to achieve low-power dissipation and low-voltage operation. Because parallel voltage comparison is used in the flash ADC, the power dissipation is much larger as we increase the resolution of the ADC. We have both introduced the Power and delayed the management technique in the TIQ flash ADC. Substantial decrease in power dissipation at reduced resolution will prolong the battery-powered operation. The fresh power management technique can handle power dissipation by controlling its on-demand sampling interval. The TIQ flash ADC was introduced with CMOS technology to verify characteristics for low voltage operation at low power supply voltage. Without any additional circuits, the TIQ flash ADC worked correctly at high speeds and with small linearity errors. This comparison with other ADCs shows a smaller size, higher speed, and lower power dissipation of the TIQ flash ADCs. Therefore, we can conclude that the TIQ flash ADC is preferable for SoC implementation.

IV. SIMULATION AND RESULTS

Table. 1 Results of different flash ADC

	Conventional flash ADC	Mux based tiq flash ADC	Proposed mux based tiq flash ADC
Technology	90nm	90nm	90nm
Resolution	4bit	4 bit	4 bit
Supply voltage	1.2 V	1.2 V	1.2 V
Delay	232ns	198ns	170ns
Power dissipation	22.6mw	10.23mw	6.78mw

The table above demonstrates that the proposed flash ADC is enhanced in efficiency as well as less power dissipation. The present flash ADC is less region relative to other flash ADC.

The bar charts for delaying distinct flash ADC as shown in Figure 8 and the bar graphs for energy dissipation of distinct flash ADC as seen in Figure 9

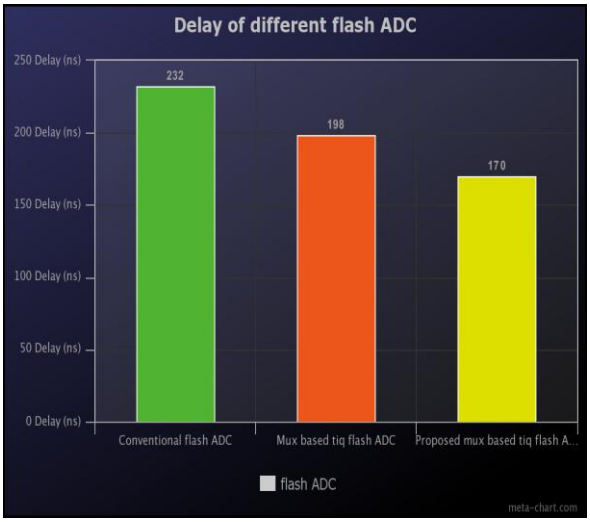

Fig. 8 Delay comparison of flash ADC

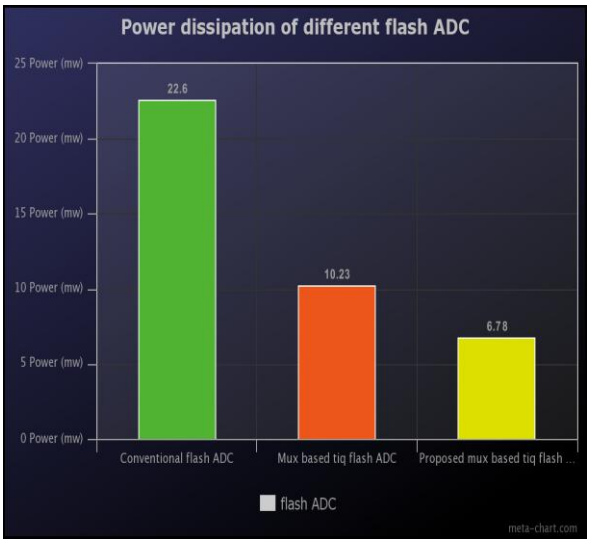

Fig. 9 Power dissipation of different flash ADC

Fig. 10 Simulation of tiq flash ADC

The flash ADC Waveform's 4 bit architecture as shown in Figure 4.3 The Vin is analog signal input and the corresponding digital outputs are D0, D1, D2, D3.

V. CONCLUSION

A fresh flash ADC based on TIQ is introduced that removes the resistive array presence and it's used to create 4 bit ADC that provides Gray code as an output. A new modified mux-based encoder is suggested which also reduces electricity expenditure. So, this strategy of the proposed TIQ ADC is appropriate for SoC apps where the main requirements are decreased area and power with immense speed conversion. In these applications, the proposed ADC can be used. The suggested converter could be modified as future steps by decreasing the scaling of technology.

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