Experimental Research on Performance Analysis of a UPFC Damping Controller

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Abstract—The unified power quality conditioner is equipment used for regulated voltage distortion and voltage unbalance in a power system. This device gives unique control on the power flow and voltage stability in the transmission line within their limits and enhancing the power to flow through the preferred path. This paper presents a control scheme and Theoretical derivation of the unified power flow conditioner and the simulation results are compared and contrasted in detail. UPFC is a combination of shunt Active and series active power filters. UPFC contains a DC link capacitor in a single phase voltage source inverter with two back to back connected, three-phase three-wire and three-phase four-wire are arranged. The objective of the study is to introduce a scheme which improves the quality of power in the flexible AC transmission systems on the aspects of voltage sag and harmonic distortion apart from enhancing power transfer capability and stability limit using unified power flow conditioner In this, the power system simulation models are made on MATLAB version. The results obtained show that the UPFC controller had better performance to damp LFO compared to the other UPFC damping controllers.

Keywords: Unified Power Flow Controller (UPFC), Fuzzy Logic Power System Stabilizer (FLPSS), Flexible AC Transmission Systems (FACTS), Static Synchronous Compensator (STATCOM), Static Synchronous Series Compensator, (SSSC), Low-Frequency Oscillations (LFO), Total Harmonic Distortion (THD)..

I. INTRODUCTION

Numerous increasing demands of electrical power for different types of load are degrading the quality of power in the system. So to improve the power quality, different Flexible AC transmission system (FACTS) devices are used to maintain controllability and capability of the electrical power system. One of the numerous arrangements is the utilization of a jointed mechanism of the shunt and dynamic arrangement channels like Unified Power Flow Conditioner (UPFC). This device consolidates a functioning shunt and series channel with an arrangement dynamic channel in setup, to all the while repay the supply voltage and the heap current or to moderate any voltage and current changes and power calculate amendment a power dispersion organize. The performance of UPFC Transformative with Intrinsic Algorithm (TIA) transmission system is improved.

In the past several decades, linear and nonlinear control techniques, modern and the traditional planning principles based on successfully proposed in the literature have been applied to control the Transmission system.

Unified power Flow conditioner (UPFC) is equipment in flexible AC transmission system capable of improving the

stability of a power transmission system with a suitable design. In this chapter, a general introduction to the basic operating principle of UPFC and UPFC Power Oscillation Damping Controller and their tuning has been discussed. The fundamental target of this work needs to enhance the power quality of a transmission line by improving the real and reactive power flow, mitigation of voltage sag and swell, and reduction in THD using Unified Power Flow Controller (UPFC) for based on Transformative Intrinsic Algorithm (TIA) control algorithms. The performance analysis of the proposed technique is carried out by using Matlab Simulink software.

II. WORKING PRINCIPLES OF UNIFIED POWER FLOW CONTROLLER

The UPFC has the ability to control all the parameters affecting power flow in a transmission line, i.e. the bus voltage, the line impedance, and the power angle. It realizes the function by injecting a voltage between the sending and receiving end buses. Figure 2.1 depicts a typical three-phase UPFC configuration.

As can be seen in Figure 2.1, if the series converter is disconnected, the shunt converter works as a STATCOM along with the DC capacitor and the shunt 25 transformers. In this situation, the STATCOM generates or absorbs reactive power to or from the Point of Connection (POC).
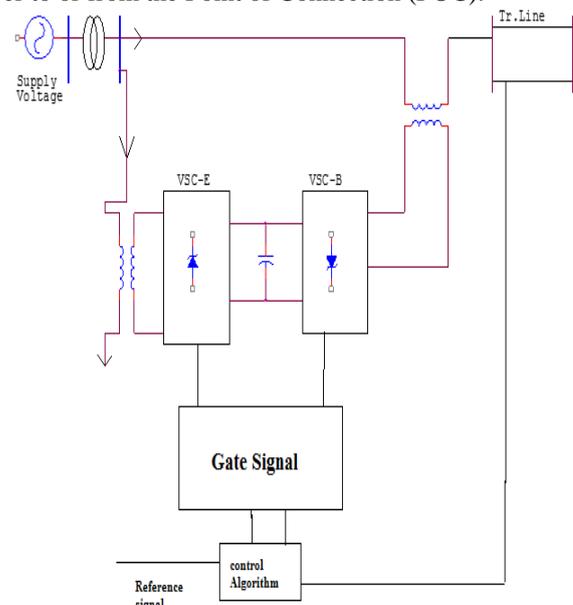

Figure 2.1 UPFC structure

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If the shunt converter is disconnected, the series converter will function as a Static Synchronous Series Compensator (SSSC) along with the DC capacitor and the series transformer. The SSSC works as a voltage source injecting a voltage Vc into the transmission line through the series transformer. The Magnitude of Vc is independent of the line current. The Phase angle between Vc and the line current is either 900 or -900. In the two above described situations, the shunt and series converter generates/absorbs reactive power independently. Thus, the UPFC can be modeled as a dependent voltage source (the SSSC) and a dependent current source (the STATCOM).

When the two converters exchange real power, the series converter of the UPFC can change the bus voltage in other patterns. The series converter can inject a voltageVc, which is in phase with the bus voltage. The effect is equivalent to the tap-changing transformer. However, the magnitude of the injected voltage can be continuously controlled in the range of voltage level allowable for the series converter. The series converter can also inject a voltage which is in quadrature to the bus voltage. In this mode, the series converter works to change the effective inductance of the transmission line. The series converter can also be used to change the power angle without change of the bus voltage magnitude. In the last mode, the UPFC injected a voltage which changes all the transmission line parameters: the bus voltage magnitude, the line inductance, and the phase angle.

In practice, the series converter injected voltage is limited by several factors. One of them is the voltage rating of the inverter. The voltages on the DC capacitor, the switching devices, and the related transformer cannot exceed the designed voltage rating of each component. Due to the ability to exchange both reactive and real power with the transmission line, the series converter injected voltage is shown in Figure 2.2(b)can be at any phase angle as in Figure 2.2(c) when the voltage magnitude Figure 2.2(a) is lower than the rated 30 value of the converter. Thus, the achievable Vs + Vc will be in a circle. Moreover, the voltage drop at the series transformer inductance also needs to be taken into account. The effect is that the available series converter injected voltage range shifted as the dotted line circle illustrates Figure 2.2 (d) series compensation. The voltage drop is related to the line current. At heavy loaded transmission line, the series transformer inductance can cause an additional voltage drop.
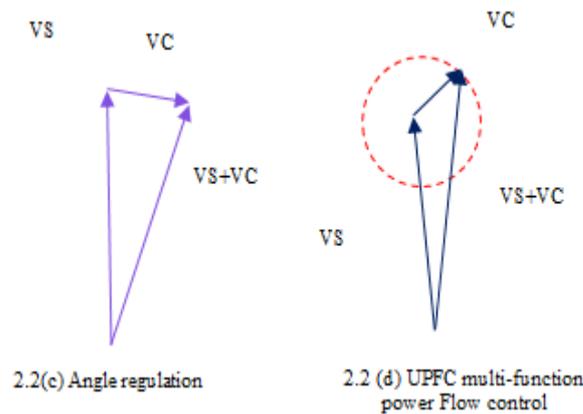

2.2 (a) Voltage regulation   2.2 (b) Series compensation

Figure 2.2 Phasor diagram when UPFC working in different modes

The other constraint is the bus voltage Vs'. The Vs' is limited in the range from a certain minimum value to a maximum value. The constraint is shown as two curves. The result of all the constraints is that the achievable and available voltage Vs' is in the shaded area of voltage constraints of a UPFC system is shown in Figure 2.3
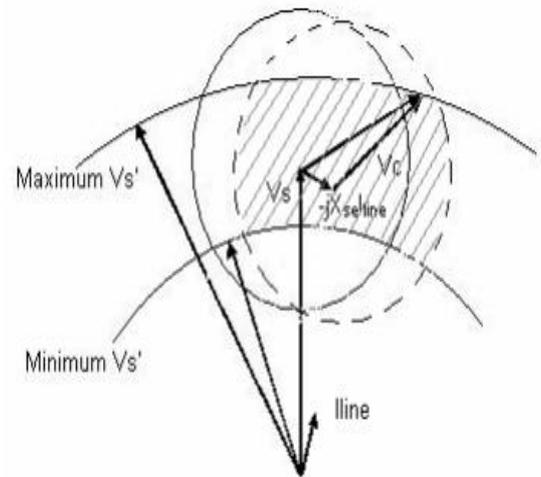

Figure 2.3 Voltage constraints of UPFC series device

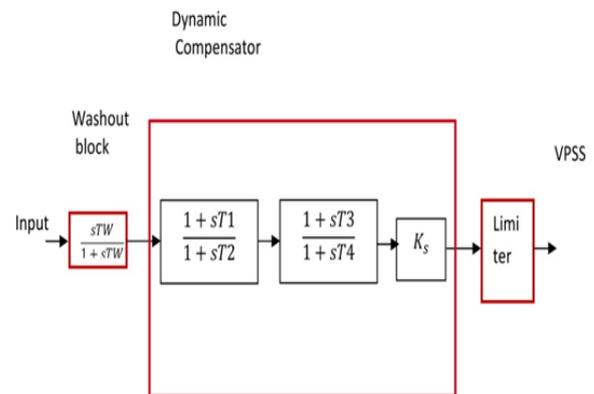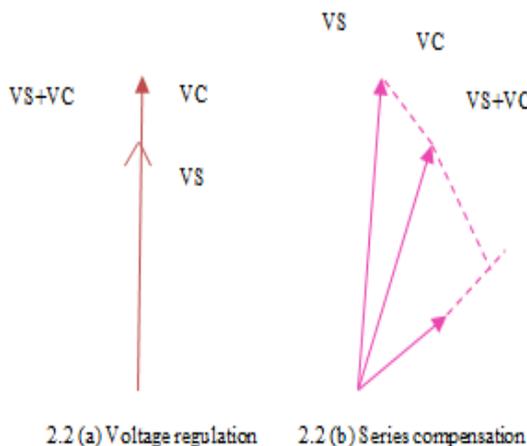**III. DESIGN OF DAMPING CONTROLLERS POWER SYSTEM STABILIZER**

Figure 3.1 Damping Controllers Power System Stabilizer

Block diagram of the damping controller is shown in Figure 3.1. Power System Stabilizer consists of Washout block, Dynamic compensator block, and Limiter. The Fundamental function of a Power system stabilizer is to provide sufficient damping to the generator rotor oscillations by controlling its excitation using an auxiliary stabilizing signal(s). To provide damping, stator and rotor speed deviations from the hierarchy should be a component of the electrical winding.

Wash out Block: Serves as a high-pass filter, with the time constant associated with TW high enough to allow signals to pass unchanged or in the oscillations. Without it, the speed in the steady state would modify the terminal voltage changes. It only allows the PSS to respond to changes in the range of 1 to 20seconds in the speed may be.

The Dynamic Compensator: It is used in lead-lag industries have two stages, and it is shown in Figure 3.1 Where the PSS Ks introduce the amount of damping. Ideally, the gain should be set at a value corresponding to maximum damping it is however often limited by other considerations. Time T1 to T4 are constants chosen to provide the input signal for a phase lead in the range of frequencies that are interested.

Limiter: It is designed to pass the signal frequency while allowing swing mode from system conditions from any variation in this frequency. It rejects frequencies associated with non-power swing modes, such as modes relating to sub synchronous torsional oscillations and noise signals that override the auxiliary control signals. In some cases, this may be noise frequencies within the bandwidth of the power swing.

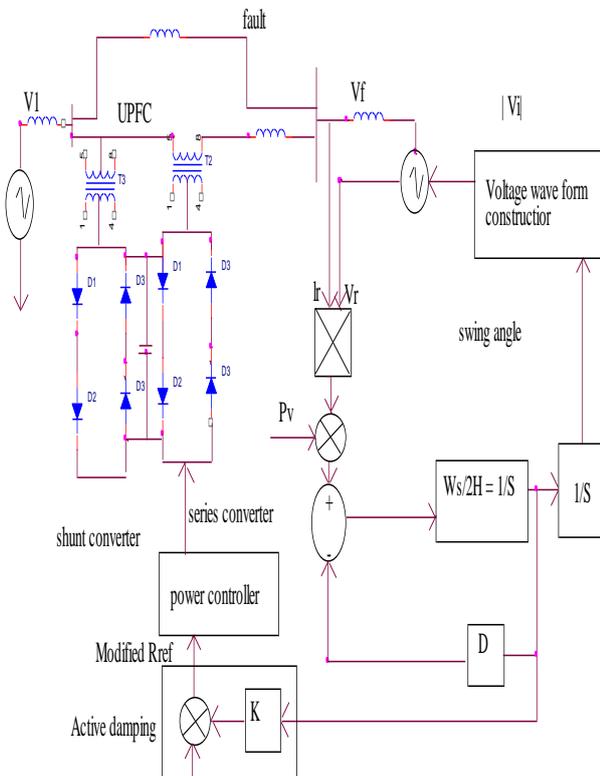## IV. ANALYSIS AND DESIGN OF UPFC DAMPING CONTROLLER

Figure4.1. Block diagram showing the "swing bus" &control algorithm for power oscillation damping

For designing, we are using the swing equation. By using the swing equation, a block is designed which results in the output as Active power command. This Pref controller output is compared and given feedback to the UPFC as input. The UPFC controller system is primarily designed to pass dominant swing mode frequency. High operating point and a specific magnitude of the system damping has been chosen for the entire layout of the heavy power transfer function. A maximum level of interaction with sub synchronous modes is ensured, and noise amplification beyond an acceptably small limit is not permitted. The efficiency of the controller must be established for both forward and reverse power flow in the tie-line. The below Figure 4.1.shows the schematic diagram of the UPFC damping controller.

According to the swing equation,

$$M\frac{d^2\delta}{dt^2} = P_M - P_e \quad ....(4.1)$$

Where M=Inertia constant Pm=Mechanical power Pe=Electrical power

Providing active damping where the rate of change of the differential phase angle between the sending-end and receiving-end buses d_δ/d_t is sensed and fed into the real power command, Pref, with the correct polarity and an appropriate gain for the UPFC can control which helps in generating the power flow through the line from source to relieve sudden loads and reduces system oscillations.

A. Series Converter Reference

By d-q transformation, the transmitted real and reactive power to the receiving end bus is controlled independently. In the d-q axis for the three-phase system, $p = v_{rd}i_d$, $q = v_{rd}i_q$, where vrd is the d axis component of the receiving end voltage. id and iq are real and reactive components of the line current respectively. So, the d-axis and q-axis reference current in the transmission line is calculated as equation (4.2). The computation process is depicted as Figure 4.2

$$\begin{cases} i^*_{d=\frac{p^*}{v_{rd}}} \\ i^*_q = \frac{q^*}{v_{rd}} \end{cases} \quad ....(4.2)$$
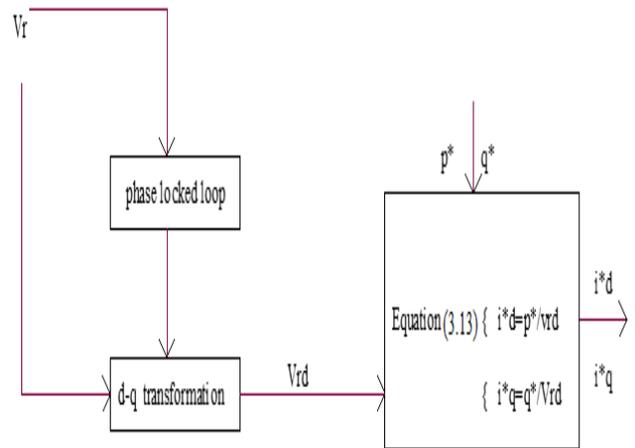

Figure 4.2 Series current reference
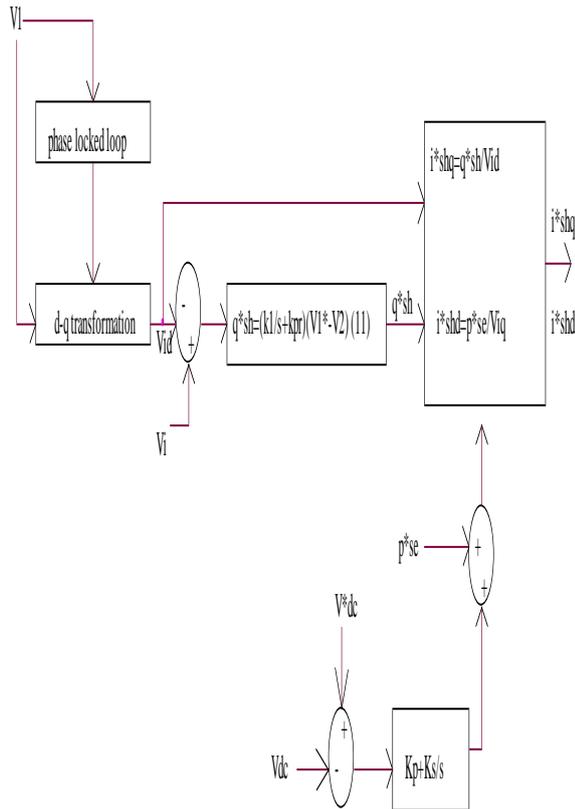
B. Shunt current reference computation

Figure 4.3 Shunt current reference computations

The magnitude of the sending end bus voltage v1 is controlled by shunt device reactive power injection. So, the reactive injection power qsh can be controlled by a PI controller. The Reference value of qsh is:

$$q^*_{sh} = \left(\frac{k_{iv}}{s} + k_{pv}\right)(|V_1|^* - |V_1|) \qquad (4.3)$$

Where * v1 is the sending end voltage magnitude reference and v1 the real-time voltage magnitude. Kiv and Kpv are the integral and the proportional gain for the PI controller. If the rotating axis is synchronous with the sending end voltage, the d axis component of the voltage is the instant magnitude of the voltage. So, $v_1 = v_1d$.

Then, the q-axis reference current in the shunt branch should be:

$$i^*_{shq} = q^* \frac{se}{vid} \quad \dots\dots\dots\dots\dots\dots\dots\dots\dots \qquad (4.4)$$

The d-axis reference current for the shunt branch is decided by the active power Pse drawn by the series device. At the same time, the real component of the shunt converter current is responsible for providing power losses in the switching devices and the DC capacitor. This is reflected by keeping the DC capacitor voltage constant.

$$i^*_{shq} = p^* \frac{se}{vid} + \left(\frac{k_{iv}}{s} + k_{pv}\right)(V^*DC - VDC). \quad (4.5)$$

Where, v_1d is the d axis component of the voltage at the point of connection. $pse* = vsed + vseq_{ishq}$ is the instantaneous real power injected into the transmission line by the series converter, vsed is the real component of the injected voltage. ised and iseq are the real and reactive components of the line current respectively. KiDC is the stability region of the power in the transmission line, the kpDC power Variation in the transmission line is the integral and the proportional gain for the PI controller. The real power

drawn by the series converter is supplied by the shunt converter through the DC capacitor.

The shunt current reference computation process is illustrated in Figure 4.3. Here, the DC capacitor bank is assumed to be an ideal capacitor. In practice, the capacitor has an Equivalent Series Resistance (ESR). The power loss due to ESR is also compensated by the shunt device

V. RESULTS AND DISCUSSION

A. Simulation Model of the UPFC System Using Proposed TIA

The proposed UPFC and Transformative Intrinsic algorithm based developed by Matlab Simulink software and a simulation model were shown in the following figure to 5.1. In this simulation, a Transformative intrinsic controller algorithm will be needed to balance the power and maintain the direct voltage constant; especially when the system is running under various conditions. The experimental results are compared with the methods of the improved algorithm. MATLAB 2017a operating software is the most common manipulation.
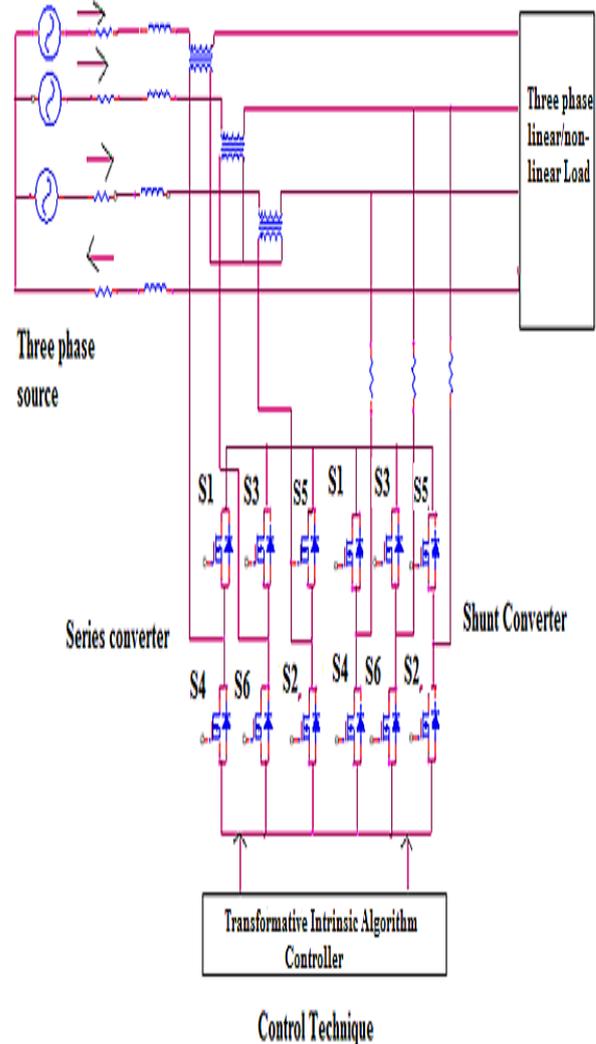

Figure 5.1 Simulink Model of Proposed system

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B. Simulation Result and Analysis

This section presents the simulation results. A comparison is made with that of the standard previous controller to test and analyze the proposed controllers.

The simulation environment is common to all the simulations. The accompanying parameters were embraced to assess the performance of the proposed controllers.

- THD analysis
- Voltage balancing system
- Steady-state Error
- Filter Performance

Table 5.1 Performance analysis for UPFC Features of the proposed and existing system

Parameters	PI	ANFIS	TIA
Steady state error (%)	1.2	0.9	0.3
Switching loss (%)	0.928	0.9	0.8
With UPFC THD (%)	10.1	7.3	4.85
Injected voltage	48.3	49.4	50.1
Peak overshoot (%)	13.1	9.7	4.9
Damping ratio (%)	0.064	0.053	0.036
Settling Time(sec)	1.3	1.26	1.086

Table 5.1 shows the comparison for the proposed Unified Power Flow Control (UPFC) which are considered for the operating features like the steady-state error 0.3 (%), switching loss 0.8 (%), With UPFC THD 4.85 (%), injected voltage is 50.1(V), peak overshoot (4.9)%, damping ratio (0.036)%, Settling Time(sec)(1.086). Of the existing system like PI Proportional Integral, Adaptive Neuro-Fuzzy (ANFIS) and Transformative Intrinsic Algorithm (TIA) proposed a system provides a better result.
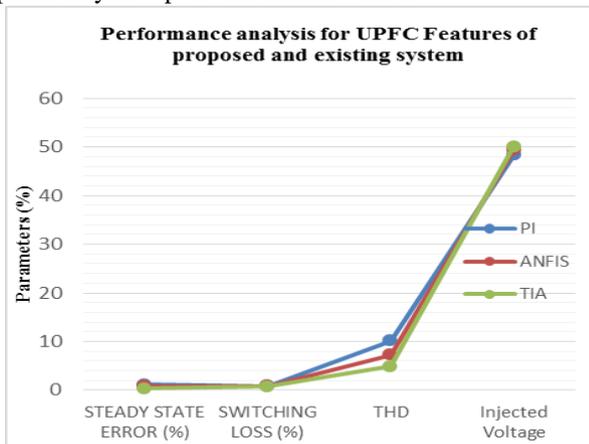

Figure 5.2 Performance Analysis of the UPFC system

Figure 5.2 performance analysis of the unified power flow control which compares various parameters like the steady-state error, switching loss and THD with conventional system .the proposed Transformative intrinsic algorithm (TIA) produce an effective result
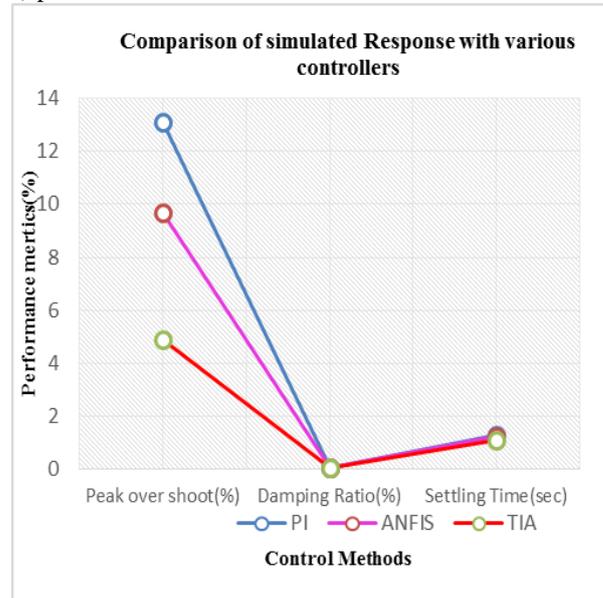

Figure 5.3 Comparison for simulated Response with various controllers

The above **Figure 5.3** shows performance analysis with various parameters such as peak overshoot (4.9) %, damping ratio (0.036) %, Settling Time (sec) (1.086).etc, are taken from the simulation results, the comparison was mentioned in Table 5.1. The results prove that the TIA based controller provides the response overshoot

Table 5.2 THD analysis for the proposed system Transformative intrinsic algorithm with and Without UPFC

Parameters	Value
THD value without UPFC	8.47%
With UPFC THD (%)	4.85%

Table 5.2 shows the Total harmonics distortion for the proposed model with and Without UPFC and the controller system which produce THD value up to 8.47% For without UPFC for with THD system it provides the THD range is 4.85(%).
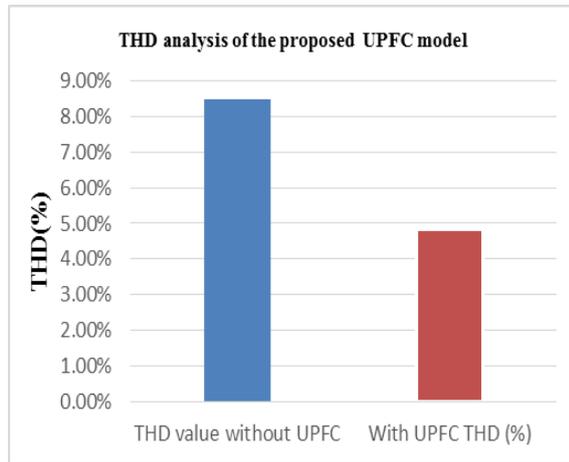
Figure 5.4 THD analysis of the proposed UPFC model

Figure 5.4shows the Total harmonics distortion for the proposed model without UPFC system is 8.47 % and With the applied UPFC and optimized transformative intrinsic algorithm reduce the value from 4.85 %.

V. CONCLUSION

The voltage stability analysis is carried out by using modal analysis and stability indices which are capable in determining the critical line with respect to the bus. The parameters of the power system stabilization and input control parameters of UPFC are tuned by Transformative Intrinsic Algorithm by minimizing problem function. The proposed controller has been examined with changing with different load conditions. On comparing the results obtained from each optimization techniques such as PI, ANFIS, and TIA it can be said that the use of UPFC controller at the line will be the better feasible solution and will have maximum power transmission in the power system. For the Proposed Transformative Intrinsic Algorithm (TIA) produce a better result in the simulation which is like steady-state error 0.3 (%), switching loss 0.8 (%), With UPFC THD 4.85 (%), injected voltage is 50.1(V). All these parameters describe the Effectiveness of the Proposed TIA algorithm while comparing with the conventional methods.

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