Multi-stage Interconnection networks CLOS/BENES Parallel Routing Algorithms For circuit switching system

B. Swapna Rani , C.Chitra

Abstract— This article approaches the design of parallel routing Clos and Benes switching networks in Communication Technology. In communication, the transmission of data with less traffic and low latency are the biggest challenges. The conventional packet switching circuits takes the more power and high area to overcome this problem parallel routing algorithms are proposed. Clos and Benes networks are designed for the circuit switching systems where the switching configuration will be rearranged and it's relatively low speed. Most of the existing parallel routing algorithms are not practical those are fail to interconnects the inputs with the matched outputs with less traffic. In this article, we designed Clos and Benes network. Clos and Benes networks are the Non-blocking switching Networks. Clos Switching network provides the better results like low area and less delay when compare with the Benes Switching Network. Clos and Benes non-blocking switching circuits are designed by Verilog HDL, Synthesized and simulated by XILINX 12.1 tool.

Keywords: Clos Network, Benes Network, Non-blocking switching networks, Parallel Routing Algorithm, Cross bar switch.

I. INTRODUCTION

In the past few years, communication technologies were growing up rapidly because of their demands in communication systems. Local area networks, metro Politian area networks and wide area computer networks are enormously deployed to interconnect computers throughout the world. In the transmission, switching circuits plays a very important role in the communication networks because switching circuits changes the terminals of connections to increase the utilization of more resources. Circuit switching has the facility that directly connects the sender and receiver in an unbroken path. In this technique, when connection is fixed a dedicated path it's exists in between the both ends users sender and receiver until the connection is closed. The Routing decisions must be taken when the connection is started first but there are no decisions made after that connection is fixed. Switching circuit is a method of designing a communication network. In switching circuit, during a connection the delay will be constant, , where packet streams may changing and probably which provide the long packet transfer delay. In which two network nodes create a circuit through the network earlier than the nodes communicate. The switching circuit arrangement with the packet switching, the data is divided into packets and independently transmitted through the network. Packet switching is the procedure of dividing the data and that data to be transmitted into the smaller packets. Every packet is arranged with the destination & series of the ordering related packets and which needs a dedicated path to help the packet and find its way to its destination. Every packet is independently dispatched & each packet routed via a different path. . For example, N users are there in communication system, instead of using fully connected structure, a switching circuit facility will be sufficient for any connection as per request, as shown in Figure1.

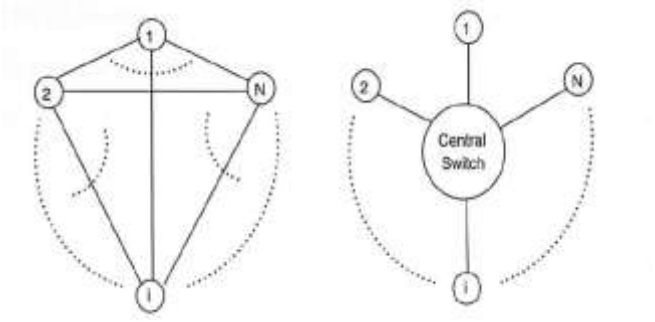


Figure1: Request path through a switch

II. MULTI STAGE INTERCONNECTION NETWORKS

Multi stage interconnection networks (MSIN) are high speed computer networks. MSIN's are mainly designed with the three elements those are processing elements (PE's), Memory elements (ME's) and Switching Elements (SE's). MSIN's are provide the high performance and low latency interconnections. Multi stage inter connection networks are mainly used for the high speed routing process and it can be used as co-processor to the main processor those are cycle shifting and sorting in a perfect shuffle network. The interconnection networks are mainly used to connect the codes in the connection or circuit. The interconnections are change according to the topologies. There are two types of topologies those are static and dynamic topologies. Static interconnect is used in small networks and dynamic interconnects are mainly used in the large networks. Multi stage interconnection networks are formed by the multi single stage connection networks. A single stage 8x8 connection network is shown in below figure2.

Revised Version Manuscript Received on 10 September, 2019.

B. Swapna Rani , Associate Professor, TKRCET, Medbowli, SAROOR NAGAR, Hyderabad, Telangana, India.(Email: swapnaharshith@gmail.com)

Dr. C.Chitra, Professor, SSSUTMS, Sehore, Bhopal, M.P, India.

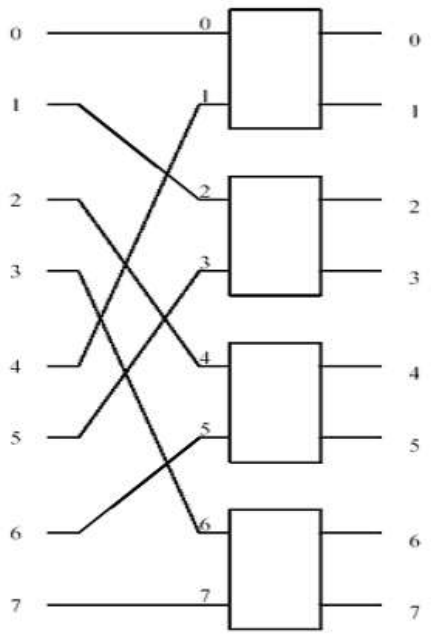


Figure2: Single stage 8x8 Network

To complete interconnection network in MIN, either the switches are controlled by the router or switches can use their own routing algorithm.

Multistage interconnection networks are derived into three types those are

1. BLOCKING
2. NON BLOCKING
3. REARRANGABLE NON BLOCKING

III. BLOCKING NETWORK

Generally, communication networks are designed with the switching circuit networks. The circuit or connection is established in between the two end users. When the request is come to the network according to the request the data will be processed via path. A connection request is to be "BLOCKED", In the network resources are not available to set up the connection to satisfy the request. This type of network is called as a Blocking Switching Network. The blocking may occur inside the switching circuit when the number of connections is provided via transmission lines. To overcome this problem the non blocking switching circuits are proposed.

IV. NON BLOCKING NETWORK

These non blocking switching circuits are implemented with the using of cross bar switches. The crossbar switch connects the multiple inputs to the multiple outputs. All the switches or cross points in the crossbar switches are arranged like a matrix.

Generally, Crossbar switches are providing the path between the input and outputs. These crossbar switches are mainly used in the telephony and circuit switch. These cross bar switches are avoiding the internal blocking in the network and which provides the better connection paths between the input and outputs. If the crossbar switch have the M inputs and N outputs nothing but which creates the MxN Matrix.

NxN cross bar switch is shown in below figure 3. Here N number of inputs and N number of outputs are there in the network and which creates the NxN matrix. Crossbar will be occurred in the network according to the request path.

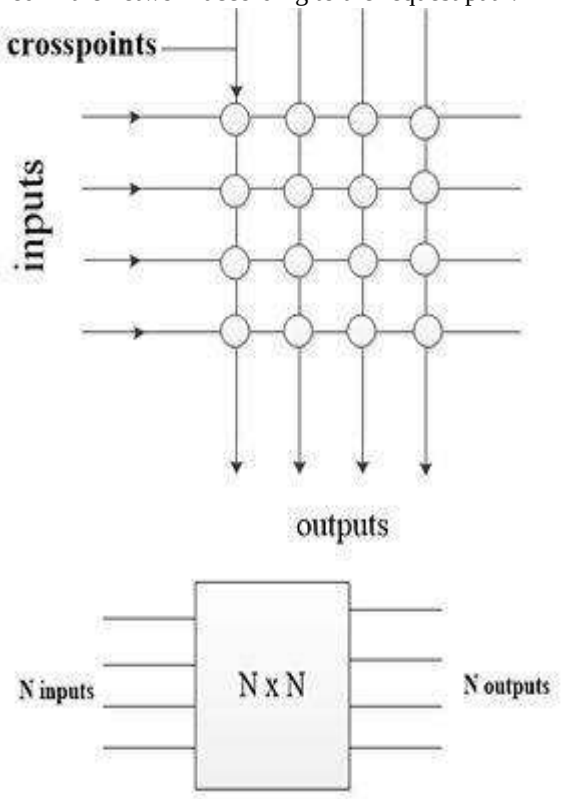


Figure 3: NxN Crossbar switch

In the Non Blocking Network, the idle input can be connected to the any idle output. The connection is already established through the network according to the right path. The non Blocking network has the N inputs and N outputs and which creates the NxN connections. The term Non Blocking it's not defective it's always have the connection. Clos and Benes switching networks are the examples of Non Blocking Switching Network.

V. REARRANGABLE NON BLOCKING NETWORK

The rearrangable non blocking network can provides the all possible connections in between the inputs and outputs by rearranging its previous connections. Benes Network is the rearrangable non blocking network because which can route any permutation if rearranging previously established connections is allowed. A permutation network also called as rearrangable in a network with some number of input terminals and equal number of output terminals and some number of switches and those are interconnected by wires.

VI. IDESIGN OF CLOS & BENES NETWORKS

Clos networks are universal multi stage interconnection networks and which realize all permutations and Benes network connect their inputs to the outputs according to the N! Permutations. This both Clos and Benes multi stage interconnection networks are used in parallel communication systems for interprocessor or memory processor

communications.

Benes Network:

Benes Network taken by his name from Benes, who was first implemented this network in 1962. Benes network is the rearrangably non blocking network. An NxN benes network have the N number of inputs and N number of outputs and its denoted by B(N). This Benes network has been proposed for used in tele communications, multiprocessors and parallel computers.

If $N=2^n$, the Benes network is constructed with the using of three stages. The 2x2 switching elements are placed in the first and last stage of network. In the middle stage we are having the N/2 x N/2 sub networks which are decomposed to smaller networks in the form of recursive manner. The three stages 8x8 Benes network structure and complete structure of 8x8 Benes networks designs are shown in below figure4.

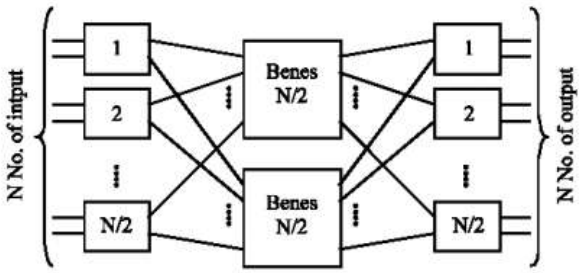
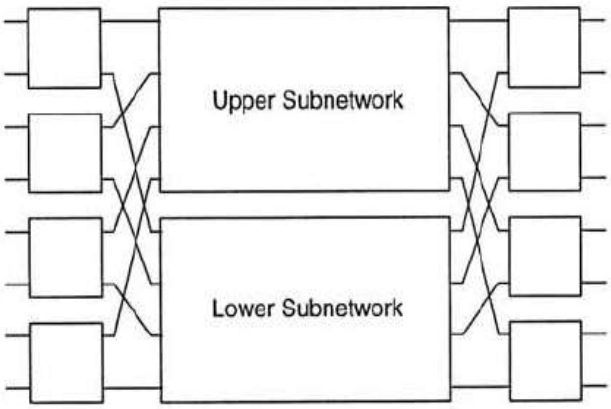
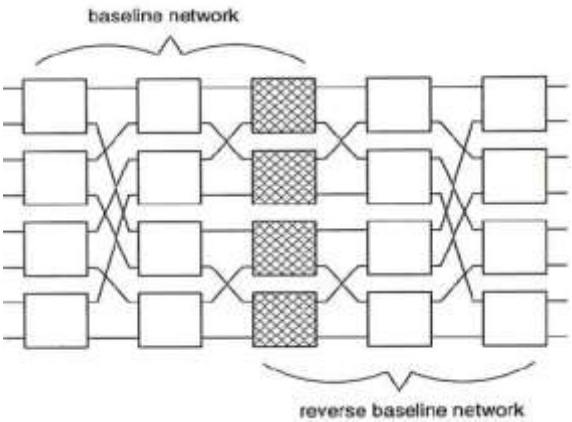


Figure A: Non Blocking Benes network with N inputs and N outputs



B. Three Stage Design



C. complete design of 8x8 Benes Network
Figure3: 8x8 Benes Network.

The Benes network has the $2\log_2 (N-1)$ stages. In this Benes Network each stage contains the N/2 switching elements. For example, 8x8 Benes network has the 5 stages of switching elements. In these 5 stages each stage contains the 4 switching elements. The middle 3 stages has the two 4x4 Benes network. The 4x4 Benes network can connect the any input to the any output recursively. The 16x16 Benes network design is shown in figure4.

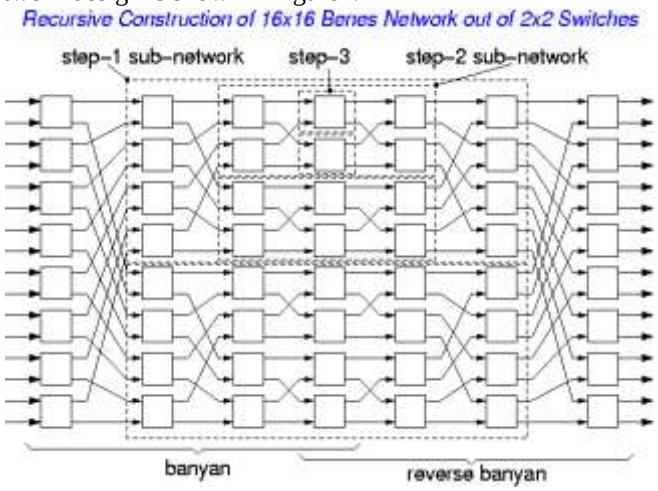


Figure4: 16x16 Benes Network

In this article we designed the 2x2, 4x4, 8x8, 16x16 Benes networks respectively. The various designs of Benes networks are done by Verilog HDL and Synthesized by Xilinx Tool. The important factors Area, delay and memory for 2x2, 4x4, 8x8, 16x16 are shown in below table.

	No. of slices	No. of LUT	Delay in ns	Memory in kb
Benes 2x2	1	2	5.906ns	131360kb
Benes 4x4	2	4	5.906ns	131360kb
Benes 8x8	16	28	8.218ns	132384kb
Benes 16x16	51	88	10.418ns	133408kb

Table1: Area, Delay and Memory parameters in Various Benes Networks

Clos Network:

In communication systems, Clos network is the multi stage interconnection network which represents the theoretical idealization of multi stage switching network. The Clos network is invented by Charles Clos in 1952. Clos Network reduces the number of stages in the network. Clos network has the three stages of cross bar switches those are input stage, middle stage and output stage. A Clos network is characterized by three integers (r,n,m) where m represents the no. of switches at middle stage, n represents the no. of

inputs at each switch , r is the no.of switches at the each stage. In this article we designed the 2x2, 4x4, 8x8 and 16x16 clos networks. The clos network reduces the number of stages when compare with the Benes network. Clos network provides the better results low are and less delay.

The relation between the number of stages of a Clos network and the network size is shown in the below equation.

$S(N)= 2 (\log_4^N)-1$

The three stage clos network is shown in below figure5.

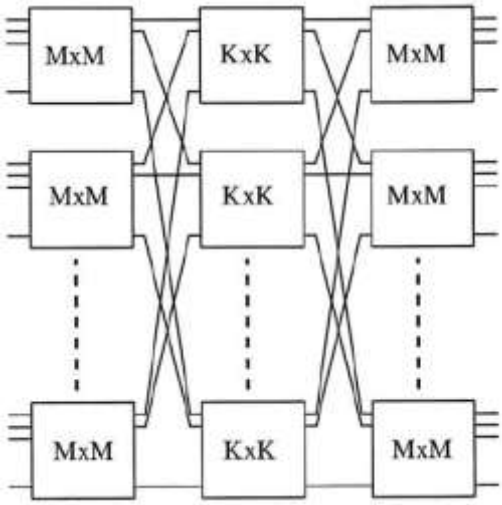


Figure5a: Three stage Clos Network

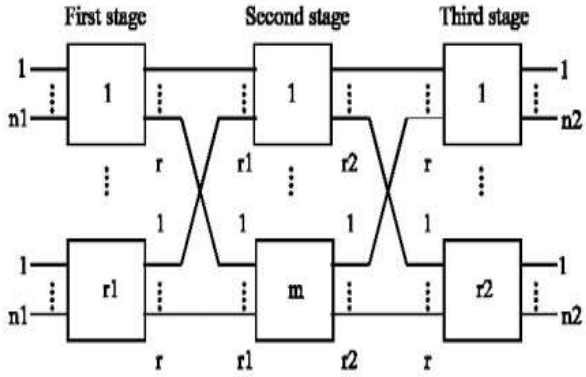


Figure5b: Three stage CLOS interconnection network

The 8x8 CLOS network is designed with the using of four 2x2 cross bar switches and four 4x4 cross bar switches. The Design of 8x8 clos network with the using of 2x2 and 4x4 circuits is shown in below figure6.

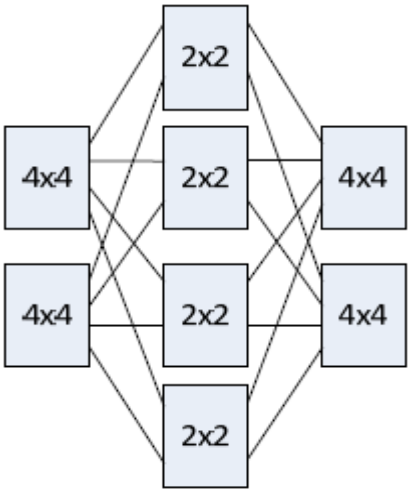


Figure6: 8x8 Clos Network

The 16x16 Clos network is shown in below figure7. The 16x16 Clos network is designed with the using of 4x4 Clos networks. It's have the three stages in each stage we have the four 4x4 Clos networks. The 16x16 clos network have the 16 inputs and 16 outputs. The 16x16 Clos network provides the better results when compare with the Benes 16x16 network.

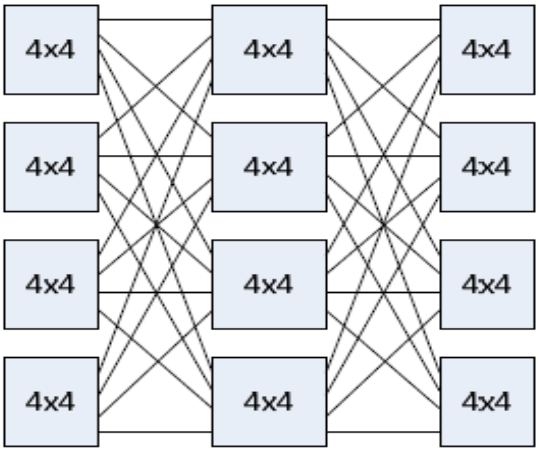


Figure7: 16x16 CLOS NETWORK

In this article we designed the 2x2, 4x4, 8x8, 16x16 Clos networks respectively. The various designs of Clos networks are done by Verilog HDL and Synthesized by Xilinx Tool. The important factors Area, delay and memory for 2x2, 4x4, 8x8, 16x16 are shown in below table

	No. of slices	No. of LUT	Delay in ns	Memory in kb
Clos 2x2	1	2	5.906ns	131360kb
Clos 4x4	2	4	5.906ns	131360kb
Clos 8x8	14	24	8.162ns	132384kb
Clos 16x16	28	48	8.162ns	132384kb

Table2: Area, Delay and Memory parameters in Various CLOS Networks

Clos Network reduces the number of stages when compare with the Benes network. The number of stages will be taken by each network is shown in below table.

SIZE	CLOS	BENES
4x4	1	3
8x8	3	7
16x16	3	9

Table 3: Number of stages in CLOS/BENES network

VII. RESULTS

In this article, we designed the Benes and CLOS networks. Those designs are simulated and synthesized by Xilinx 12.1 tool. The Benes network takes the more area and delay when compare with the clos network. The simulation results of 8x8, 16x16 CLOS network, 16x16 Benes network, area and delay parameters are shown in below figures.

4x4 CLOS NETWORK:

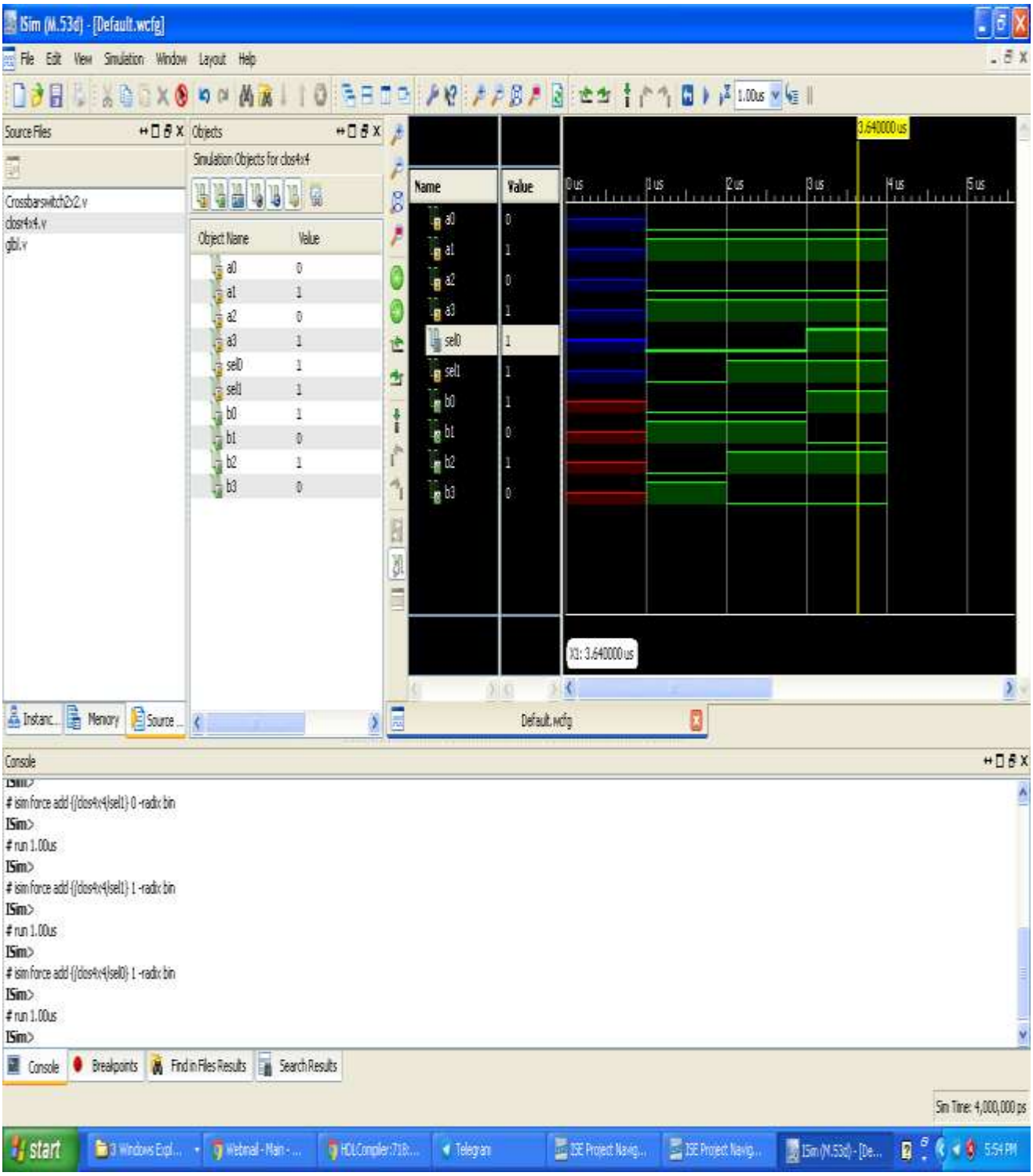


Figure 8: Simulation Result of 4x4 Clos Network

8x8 CLOS NETWORK:

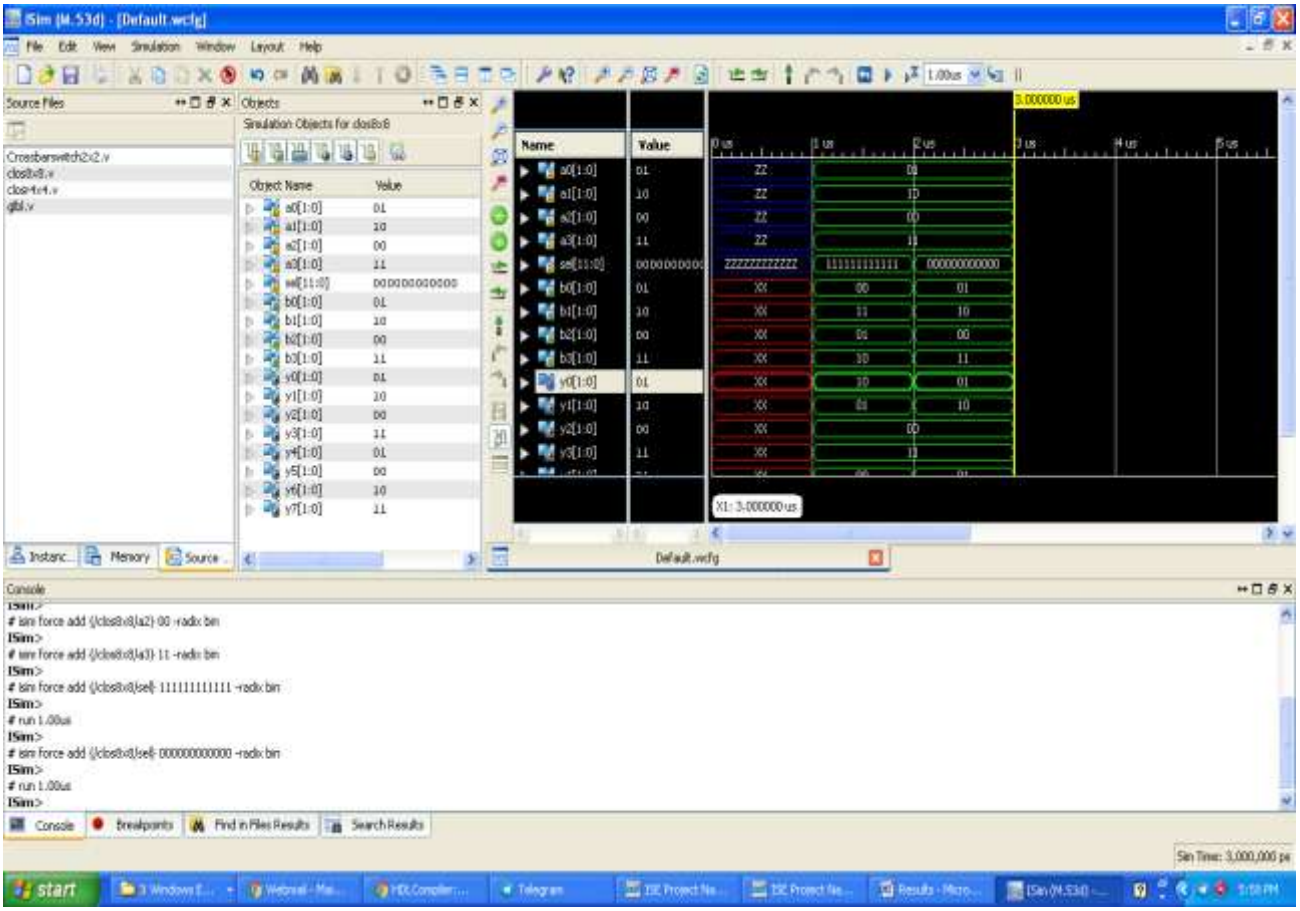


Figure9: Simulation Result of 8x8 Clos Network

CLOS 16x16

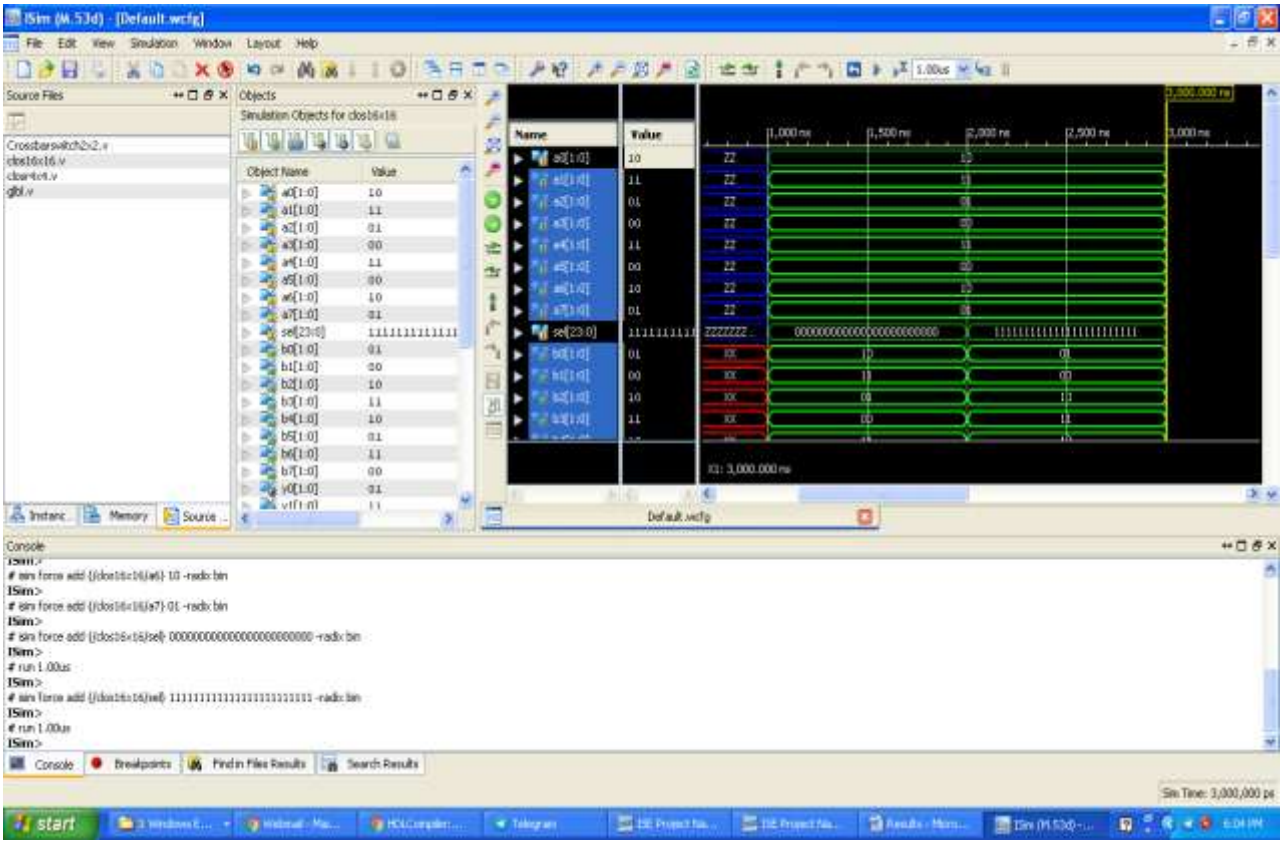


Figure 10: Simulation Result of 16x16 Clos Network

Design Summary:

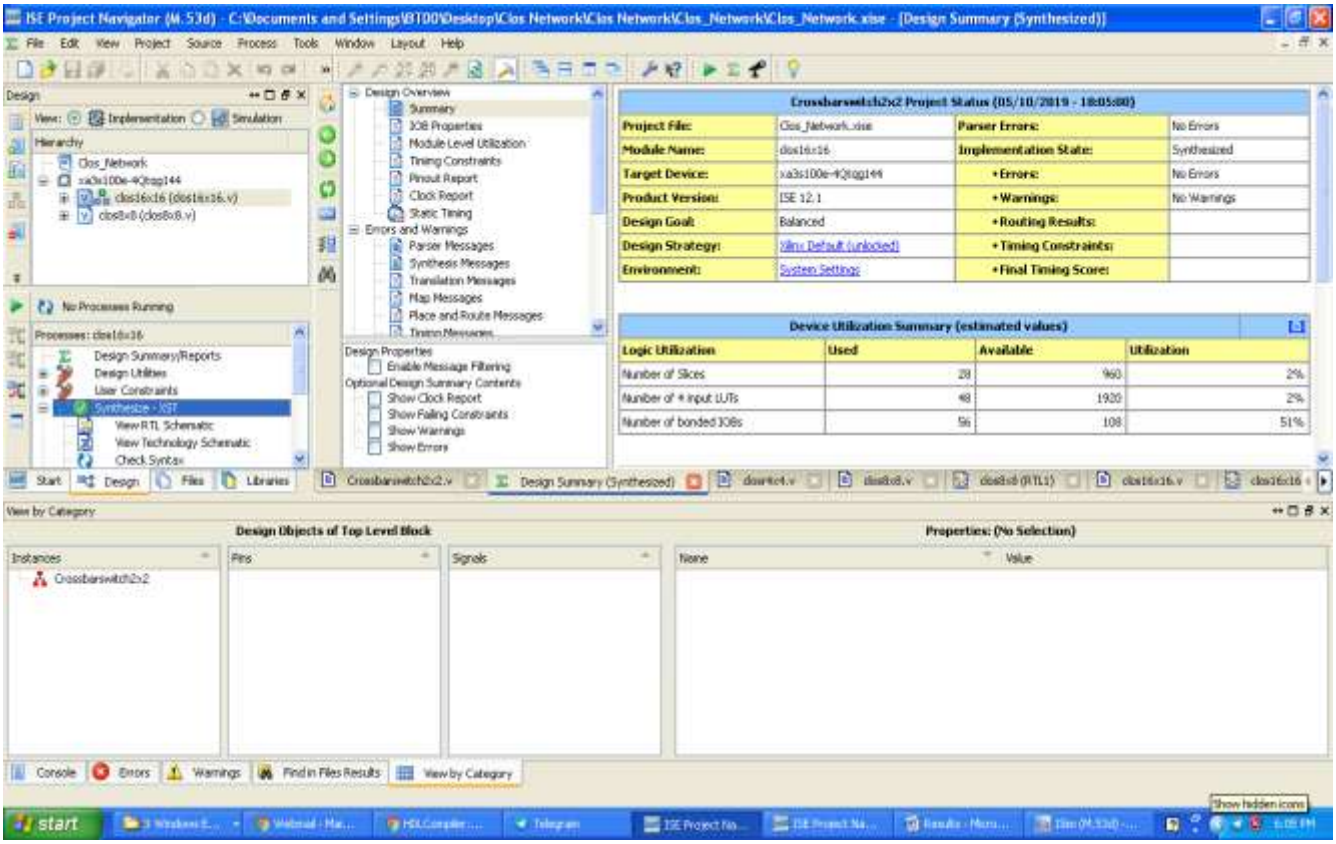


Figure 11: Design Summary of 16x16 Clos Network

Delay and Area:

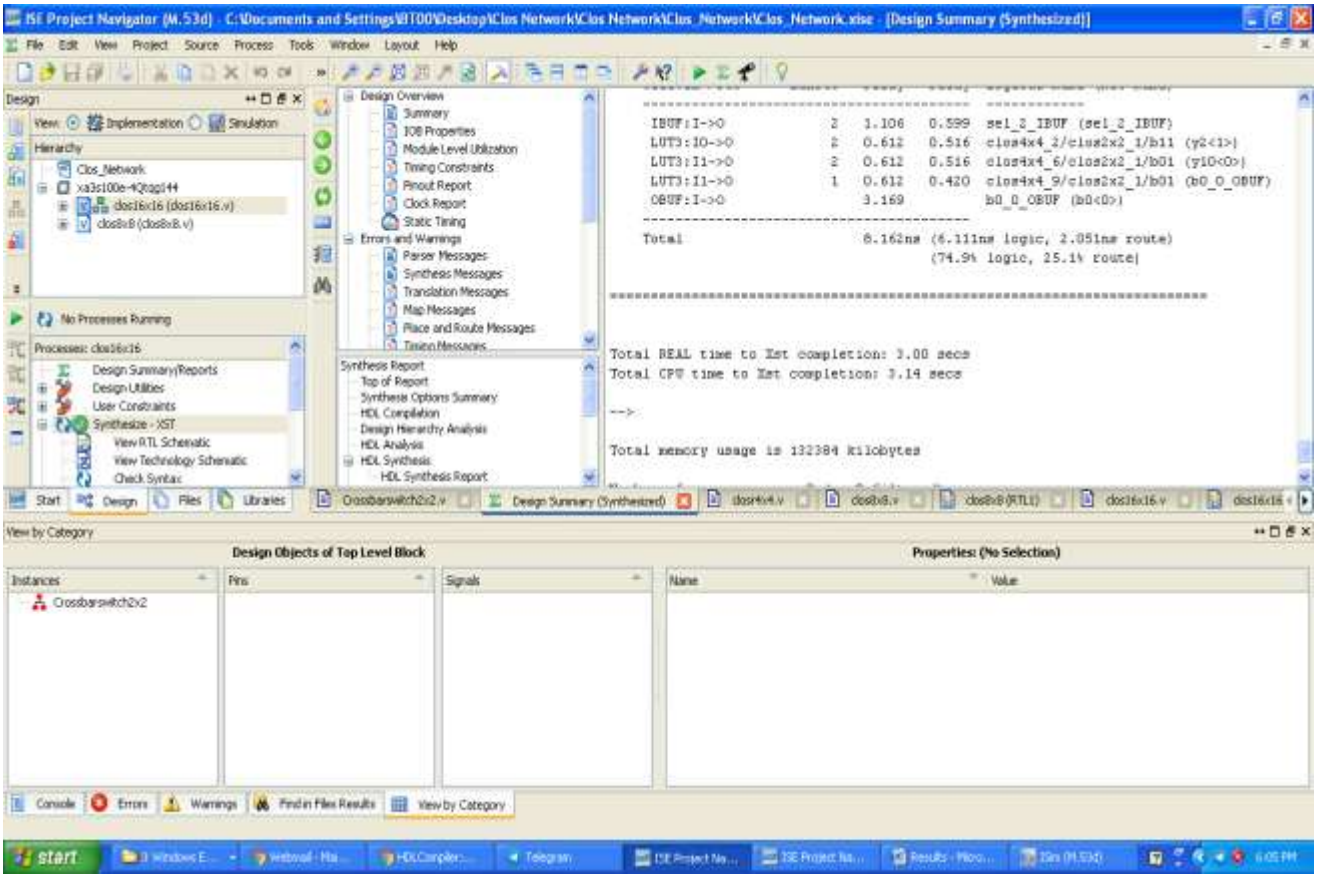


Figure 12: Delay and memory of 16x16 Clos Network

Benes16x16:

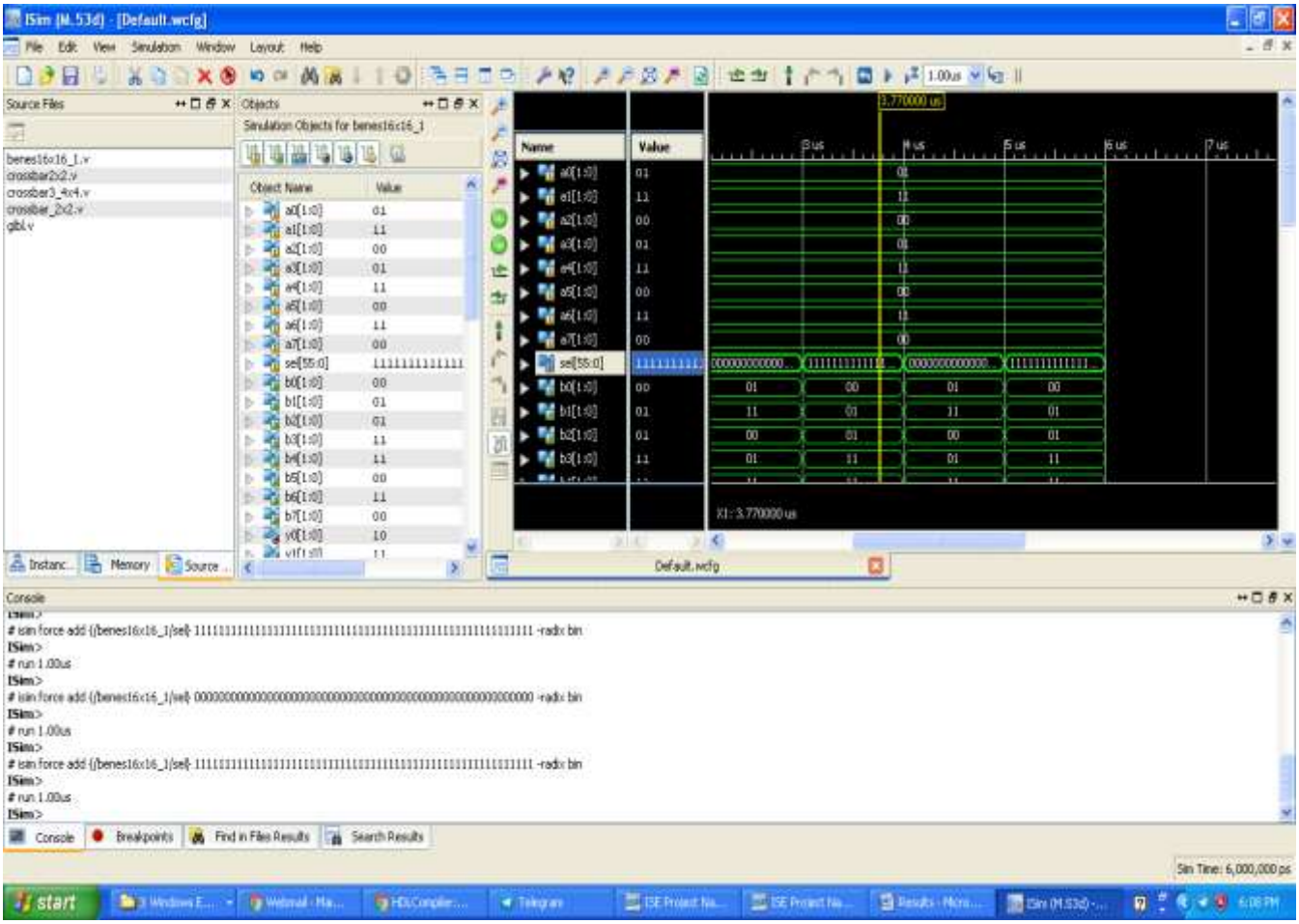


Figure13: Simulation result of 16x16 Benes Network

The comparisons of delay and area in the Benes and Clos networks are shown in below figures. As we know that the Clos network provides the better results low area and less memory when compare with the Benes network. Clos network reduces the number of stages in the network its have the only three stages for 8x8and 16x16 networks but Benes network have the 7 and 9 stages for the 8x8 & 16x16 designs.

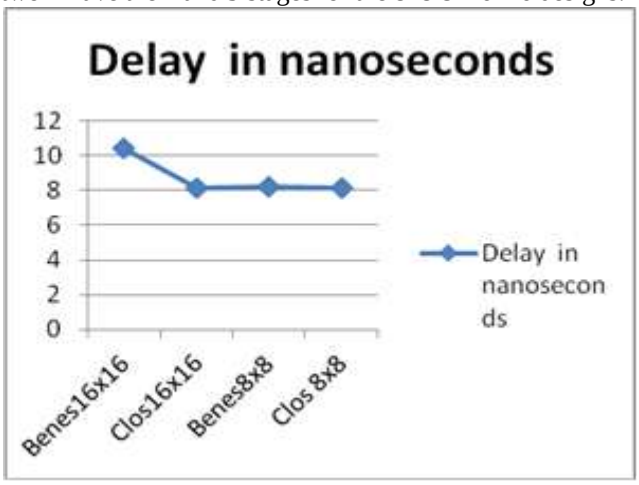


Figure14: Delay of Benes and Clos network

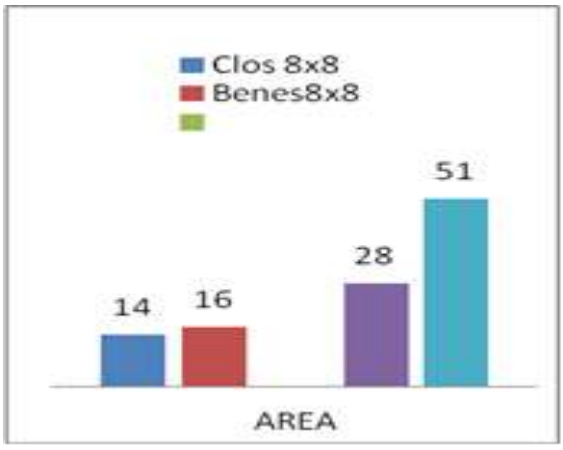


Figure 15: Area of Clos and Benes Networks

VIII. CONCLUSION

The results confirm that CLOS network is better than the BENES network. The Clos network is the extension of Benes network, the clos network provides the more flexibility when compare with the Benes network. In switching circuit system, a new connection may request a path in the network with the previous of old connections, however, the switching configuration can be rearranged at relatively low speed. The Clos and Benes networks are designed by the Verilog HDL, Simulated and synthesized by Xilinx 12.1 tool.

REFERENCES

1. Soung-yue liew, "Parallel Routing Algorithm in Benes/Clos networks", chineese university of hongkong.
2. Poornima jain pj, sreekanth T, "Design and Implementation of Efficient Permutation Clos Network Design for Mpnoc", International Journal of Computer Applications.
3. Aditya akella, T.Bensan, Balachandrasekharan, "A Universal Approach to Data Center Network Design", ICDCN '15 Jan. 4-7, Goa, India.
4. Tong Ye, Tony Lee, weisheng hu, "AWG-Based Non-Blocking Clos Networks", IEEE/ACM Transactions on Networking (Volume: 23 , Issue: 2)
5. Fadoua Hassen ; Lotfi Mhamdi, "A scalable multi-stage packet-switch for data center networks" Volume: 19 , Issue: 1
6. Fadoua Hassen, Lotfi Mhamd, "A Scalable Multi-Stage Packet-Switch for Data Center Networks", JOURNAL OF COMMUNICATIONS AND NETWORKS, VOL. X, NO. Y, DECEMBER 2016.
7. Ziqian Dong, Roberto Rojas –cessa, "Non-blocking memory-memory-memory Clos-network packet switch" 34th IEEE Sarnoff Symposium
8. Riccardo Melen, Jonathan S Turner, "NONBLOCKING MULTIRATE NETWORKS", Washington University.
9. Yuanyuan yang, Gerald M Masson, "Non blocking broadcast switching networks", vol 40, no. 9.
10. K.H Esmaeel zeinali , mehdi n fesharaki, "A new approach for optimal design of strictly non blocking multi stage interconnection networks", journal of applied sciences.