RTL Design of Efficient High-Speed Adders Using Quantum-Dot Cellular Automatation

P. Gayathri , R. Mohan Kumar

Abstract— *This article presents the design of high-speed adders using Quantum cellular automata. Quantum Automata is an efficient evaluation platform than CMOS in nanotechnology. Power, surface and performance play a virtual role in nanotechnology. Quantum Automata is an emerging technology in nanotechnology. QCA provides more speed, less power consumption and large scale integration in VLSI. By using Quantum-Dot cellular automata, we can reduce the power of leaks. Generally, for transferring the data and store data, electric fields are used in CMOS technology but in QCA, storing the data and transfer the data done by electronic polarization. This article presents different combinational logic circuits depend on QCA technology. The proposed modified CSLA (carry select adder) offer the best results of delay compared to the Ripple carry adder (RCA).*

Keywords: QCA, leakage power, modified carry selection adder, RCA, majority gate.

I. INTRODUCTION

VLSI is the process of creating a Integrated Circuit that uses thousands of transistors. The Power leakage & Size of transistor is the biggest problem in Present CMOS Technologies. QCA is the most effective technology for solving problems related to CMOS transistor technology. With the using of QCA we are reducing the leakage power, Area and it provides high performance.

In the year of 1990 the quantum dot cellular automata was proposed & which have been designed in typical models of cellular automata introduced by John Von Neumann. QCA is proposed to design nanoscale devices with highly computation density & performance. QCA is a new technology in nanotechnologies and which efforts are created to reduce the complexity of the circuits. Any nanoparticle has a width of about 50 nm to about 60 nm; therefore, these elements are classified as nanoparticles, but confinement is not so much to trap a single electron. At the quantum point it is possible to trap a single electron and also called as a single-electron transistor (SET). Quantum dots allow easily the formation of one or two electrons to the maximum, no morethan10to15electrons. If you have a quantum particle inside a chip but the chip consumes a lot less energy than the particle, you never need that much of energy to cross the barrier because you can reach the barrier with low power. Most research is based on QCA nanotechnology. The single-electron transistor(SET) is based exactly on quantum dots. Quantum dots are called

islands. The islands measure about 10 nm. Therefore, the 10nm range is never exceeded between 10 and 15 nm. If your nanoparticle is less than 10nm it's called as the quantum dot if your nanoparticle is more than 10 nm from what is called a nano material. Whenever you connect this quantum dot below a very very low level then the quantum dot band interval is exactly high, so you classify the quantum dot having a very high band gap.

A cellular automata has the set of cells of a form-specific grid with a specific set of rules depend on the states of the nearest neighboring cells. Cellular automata come in different forms. The most essential properties of advanced cellular automata is the type of grid and its calculation. Grids of hexagonal, triangular & square shapes are considered.

II. QUANTUM -DOT CELLULAR AUTOMATA

In QCA, the single device is used to design all the components of a complete circuit (computing elements and cables). QCA does not have transistors like CMOS technology. Cellular automata with quantum dots consist of square-shaped quantum cells. In the quantum cell, we have the 4 quantum dots placed in the corners of quantum cell. The basic model of Quantum cells is in below figure.
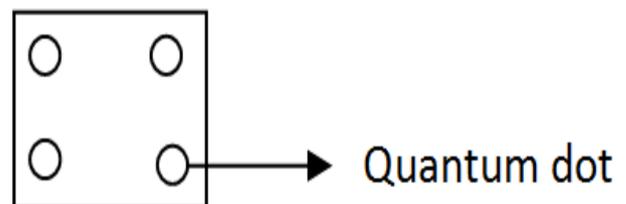

Figure1: Quantum cell

In these four quantum dots, it contains two electrons. Where the transmission of electrons occurs in the coulomb interaction of electrons. The quantum cell has contains electrons where the interaction of coulomb (electrostatic interaction) with nearest neighboring cells takes place. QCA uses a new technique for transferring data and store the data into it. It uses the polarization effect instead of the current for the transfer information containing the digital data (0, 1 bits). The quantum cell is responsible for transferring data across the circuit. The binary 1 representations of QCA and the binary 0 representations of QCA are illustrated in Figures 2 and3below.

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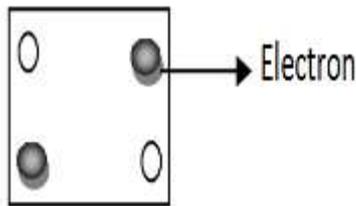*& Sciences Publication*

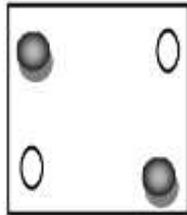**Figure2: Binary 1 Representation**

Figure3: Binary 0 Representation

The basic QCA logic has the three-input majority gate, the wires and the inverter. In the QCA logic, majority gate with the inverter called as a MI, it allows the creation of different QCA designs. In QCA, majority gates & inverters serve as basic logic gates. Majority Gate design is shown in figure 4.
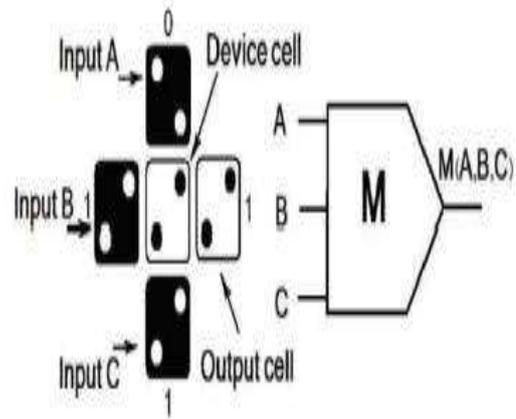

Figure4: QCA Majority Gate

III. IMPLEMENTATION OF ADDERS:

Adders are plays a virtual role in integrated circuits to increase the performance. In this article we are implementing the various types of adders like CSLA, SQRT CSLA and CSA to check the performance and delay in circuits.

IV. CARRY SELECT ADDER

Carry Select Adder (CSLA) is used in large number of processors to perform high-speed arithmetic operations. A CSLA will be designed with the use of RCA and multiplexers. In RCA, the carry result of each complete adder is used as a carry input for the next adder. The delay will be longer in RCA. The design of the 16-bit CSLA is shown in Figure 5 below.
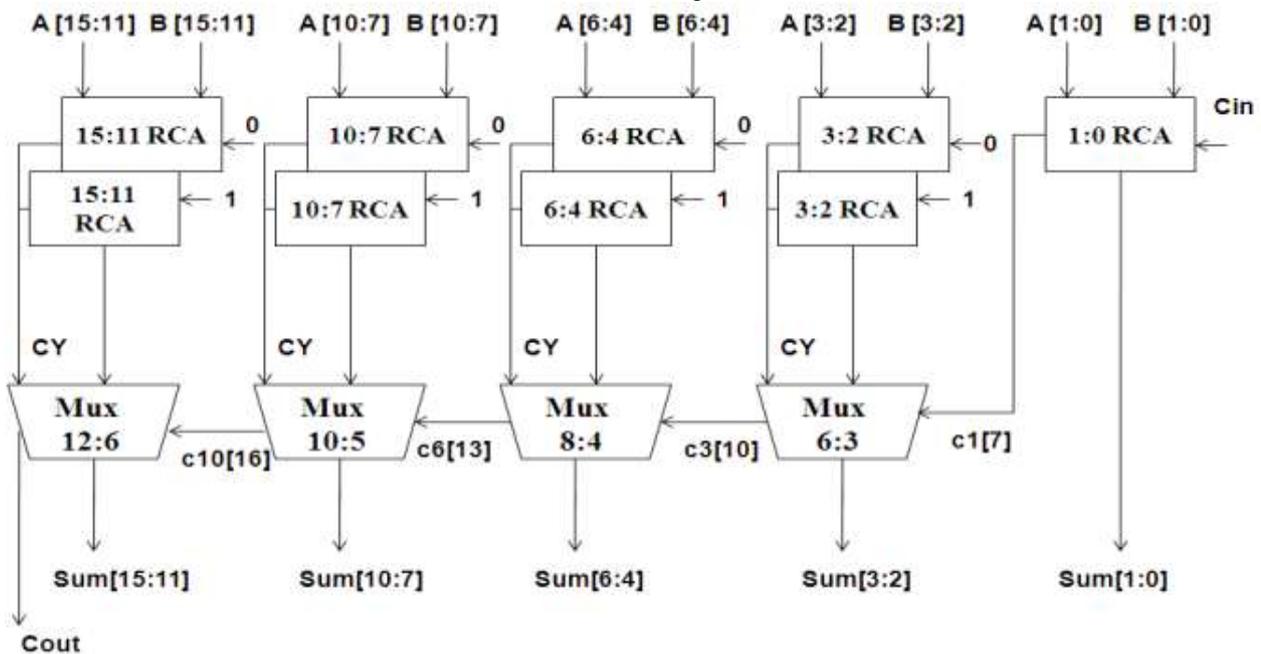

Figure5: 16bit CSLA

V. MODIFIED CSLA(MCSLA)

The CSLA is not area efficient because which uses multiples of RCA to provide carry and sum by carry input values Cin = 0 and Cin = 1 and the final output carry and sums are selected by the multiplexers. The design of the CSLA with the pair of RCA will give a longer delay. To reduce delays and increase performance, we replace RCA with BEC. The excess binary converter will reduce the CSLA

delay. The advantage of this converter logic is the least number of gates (logic gates) in the structure of the full adder of N bits. The basic logic design of the binary Excess-conversion is shown in Figure 6 below and the modified 16-bit CSLA adder circuit is shown in Figure 7.

Figure6: 4bit BEC

VI. CARRY SKIP ADDER

Carry-skip adder has the simple basic ripple carry adder with speed up a carry chain called a skip chain. Compare with RCA the CSA provides a less delay and high performance. This skip chain describes the distribution of RCB (Ripple Carry Blocks) and increase performance, we replace RCA with BEC. The excess binary converter will reduce the CSLA delay. The advantage of this converter logic is the least number of gates (logic gates) in the structure of the full adder of N bits. The basic logic design of the binary Excess-conversion is shown in Figure 6 below and the modified 16-bit CSLA adder circuit is shown in Figure 7
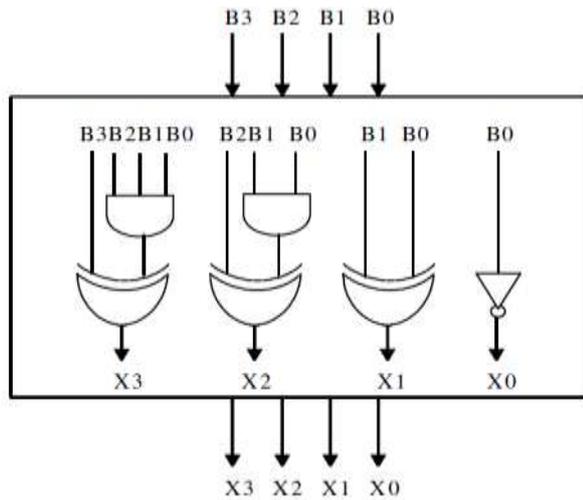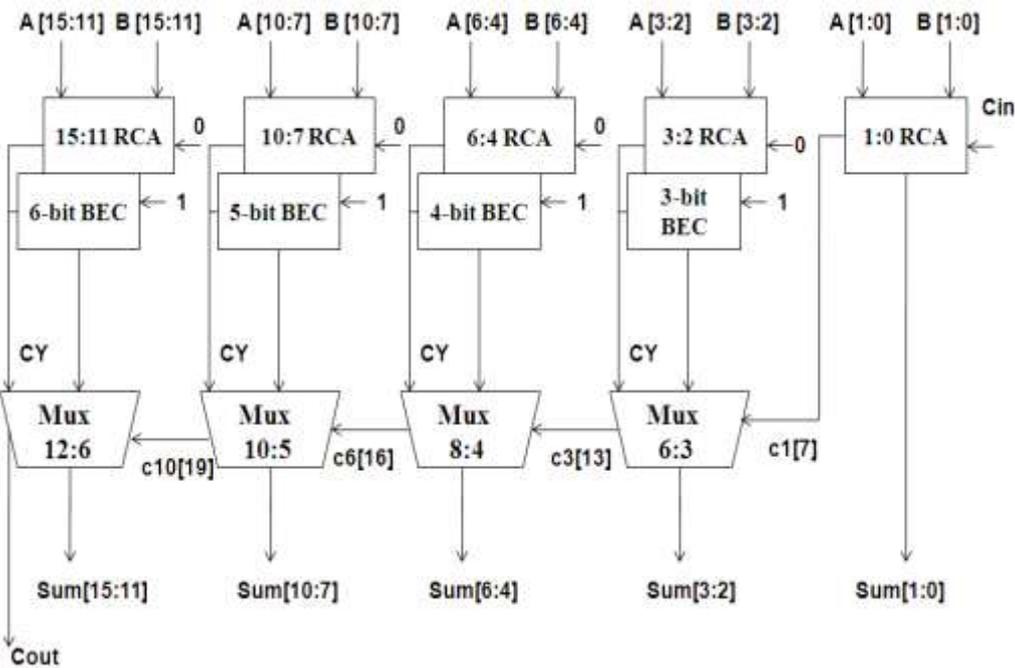

Figure7: Modified CSLA (SQRT CSLA)

which device the skip adder. A carry-skip adder implemented the speed up of an adder by assist the propagation of a carry bit around a segment of the entire adder. Carry-skip adder reducing the time of carry-propagation by skipping the groups of adder stages.
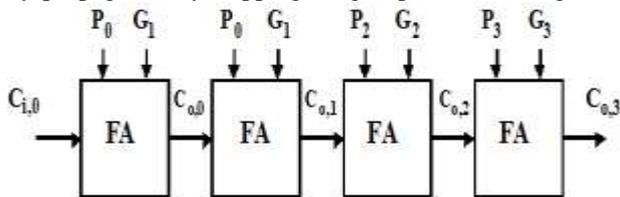

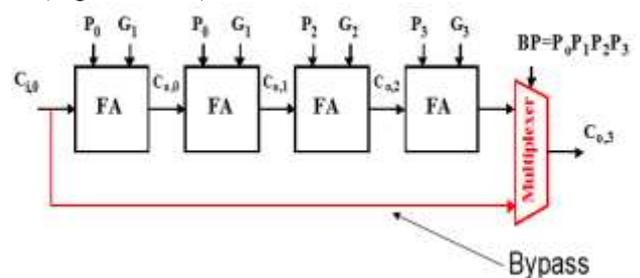**Figure7: Carry Propagation of Carry Skip Adder**

Figure8: Carry Skip Adder Structure

Carry-skip adder circuit consists of two logic gates. The AND gate obtains the carry input and matches it to the group of propagate signals with the using of respective propagate values. This bypass signal will be used to allow an incoming signal of carry to skip the all stages within the block and generate a block carry out. The CSA circuit will be shown in below figure9.
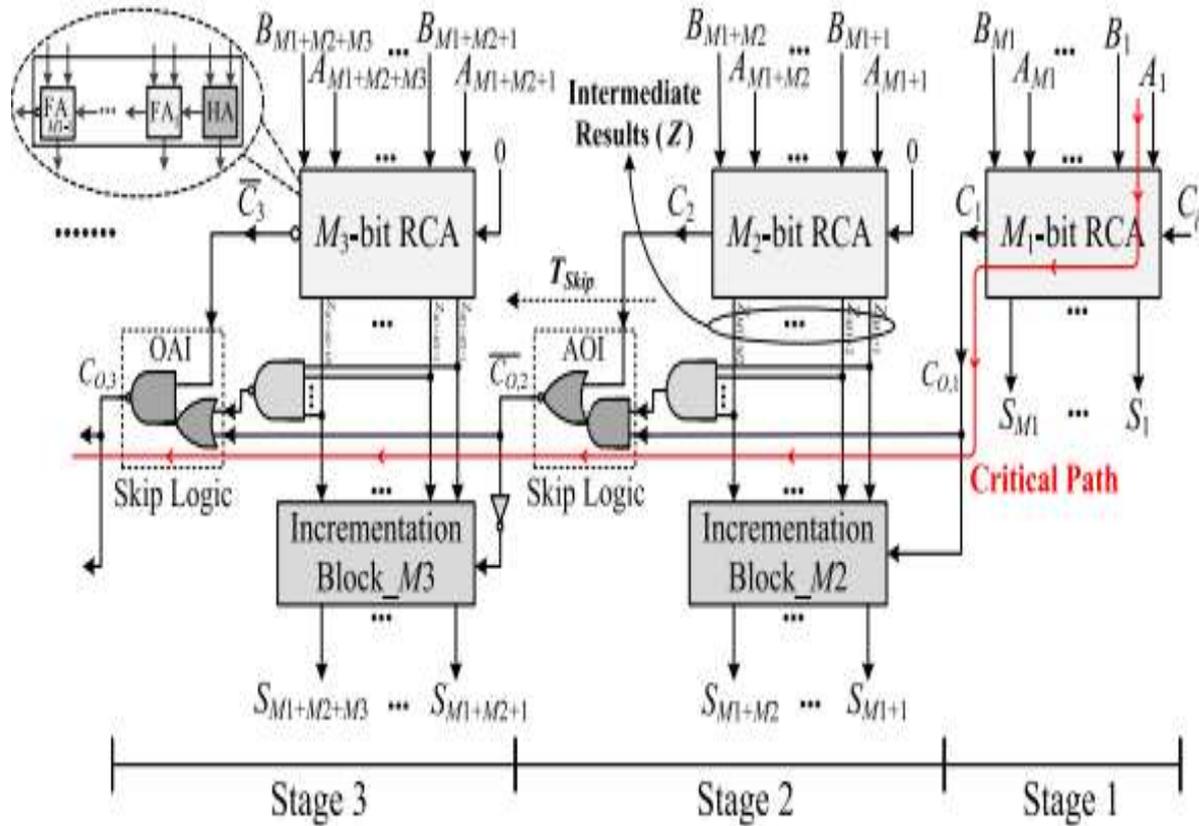
Figure9: CSA Circuit

VII. RESULTS

The CSLA with Couple of RCA's, Modified CSLA and CSA models are simulated and synthesized in XILINX 12.1 with the using of Verilog language. The delay and area results will be shown in below table.

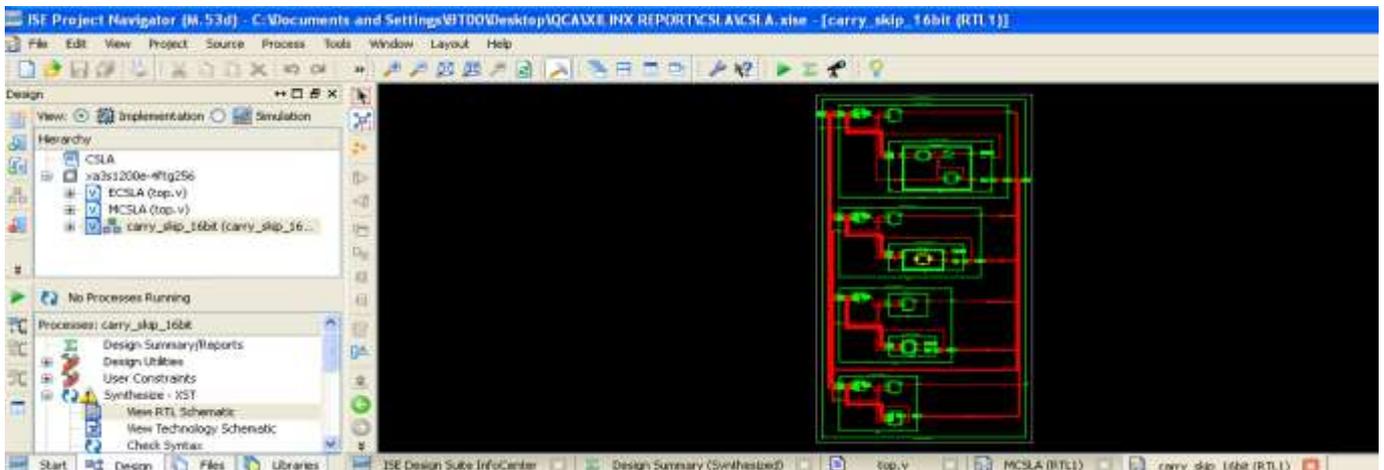|	CSLA	MCSLA	CARRY SKIP ADDER
AREA (No. Of SLICES)	24	23	25
DELAY	14.705ns	14.029ns	27.410ns

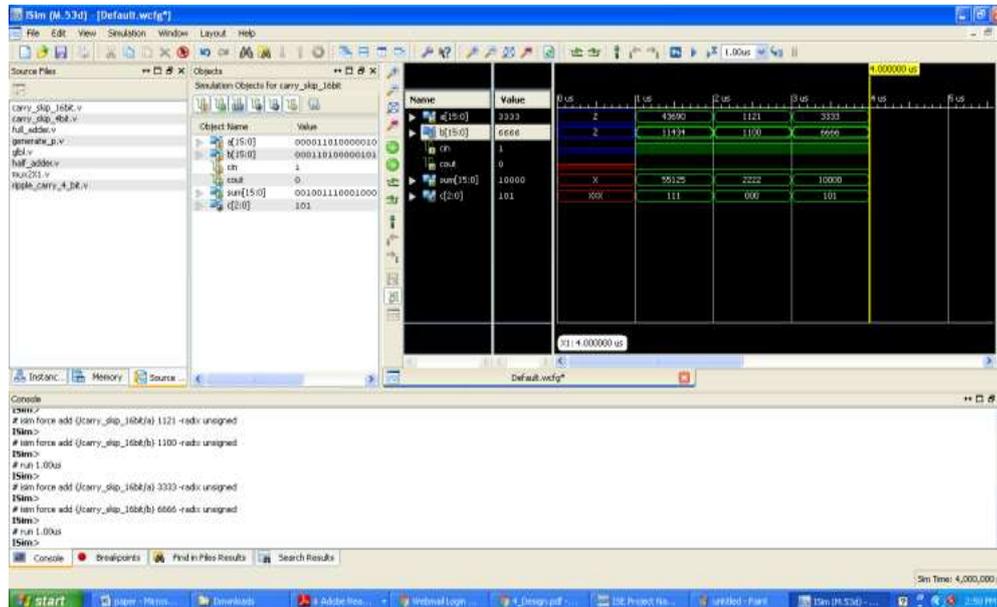**Figure10: RTL View of Carry Skip Adder**

Figure11: Simulation Result Of Carry Skip Adder

VIII. CONCLUSION

Power, delays and surface are important factors in VLSI design that improve the performance of any circuit. This work presents a quantum dots cellular automaton in nanotechnology to solve the problems of CMOS technology. We examined various types of adders and calculated surface and performance results in QCA. Simulations and synthesis are performed using Xilinx Verilog HDL. The outputs are very efficient, low latency and accurate for all combinations of inputs.

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