Qunatum-Dot Cellular Automata Technology based Optimized Multiplexers Design

Adepu Hariprasad, Sumanth Kumar Chennupati

Abstract— Multiplexer plays a dynamic role in the optimization of a digital circuit (FPGA, ALU and memory circuits etc) implementations. Due to continuous Scaling of CMOS device, has already reached to the minimum transistor size, hence , it is not possible to reduce the transistor dimensions further without scaling issues and functionality affect. QCA is one of the emerging and promising new nanotechnologies and is suitable to replace conventional CMOS technology, and potentially able to solve the physical limitations and challenges of CMOS scaling issues. In this paper, the proposed 2:1 multiplexer structure makes the use of inherent characteristics of QCA cells to act as an efficient multiplexer. The proposed QCA based multiplexer architecture improves 50% of design area, 29% of cell count and 75% of the cost when compared with the earlier designed best multiplexer architectures. Higher order multiplexers 4:1 and 8:1 are also designed using proposed 2:1 multiplexer which improved performance to a greater extent relative to existing efficient multiplexer architectures. The design and simulation of circuits have been performed using software tool QCA Designer Version 2.0.3.

Keywords: Scaling issues, Nanotechnologies, Quantum-dot Cellular Automata (QCA), Majority gate, QCA clock

I. INTRODUCTION

Continuous shrinking in the size of the transistor results more leakage currents and higher power consumption [4]. To overcome these shortcomings, as successor to CMOS, deep research proposed a few nanotechnologies like Single Electron Transistor (SET), Quantum dot Cellular Automata (QCA), Resonant Tunneling Diodes (RTD), carbon nanotubes, tunneling phase logic, etc. Among these technologies ultra low power dissipation, faster clocking and high device density make the QCA, an emerging research area in nanotechnology field. QCA is an emerging nanotechnology with extremely small size and it is not only works with ultra-low power consumption but also offers solutions for problems and limitations faced by the conventional CMOS technology in which the computation is performed by the quantum dots.

The multiplexers (MUXs) have wide applications in digital circuit implementation such as ALU, RAM, etc. [22]. The reduction in size of the multiplexer reduces the size of the digital circuits to a greater extent [1].

In this paper, we have proposed an optimized novel implementation of 2:1 MUX with which higher order multiplexers like 4:1 and 8:1 MUXs have been realized. The comparison of various characteristics of these designs with regard to the existing designs is also presented. The paper is knitted as follows. Section 2 introduction about QCA, section 3 Existing work, section 4 proposed multiplexer designs, section 5 simulation results and discussions and at the end section 6 concluding remarks of the work.

II. BACKGROUND

Each QCA cell presents with four quantum dots which are positioned at the corners of square and two free electrons. The electrons can quantum-mechanically tunnel among the dots and settle in polarization either p=-1 (logic 0) or p=1(logic 1). The basic building blocks in QCA technology designs are [1-2].

i) Majority gate function: This majority gate can be programmed in such a way that it functions as a 2-input AND gate or 2-input OR gate by fixing polarization of one out of three input cells to p= -1(ogic-0) or p= +1 (llogic-1) respectively.

M (A, B, C) =AB+BC+CA (1)

ii) QCA Inverter: The Inverter is the logical gate which produces output complement of the input. And it can be realized in different configurations.

iii) QCA Wire: Information is transmitted in QCA from one place to another place by QCA binary wires constructed from an array of cells having same polarization.

iv) QCA Clock: is used for providing power to the circuit which leads to adjustment of tunneling of barriers to raise or down between quantum dots and thus enabling transfer of electrons between the quantum dots and cells.

III. EXISTING WORK

Multiplexer is an important device in the implementation of digital memory circuits, allows us to choose one of the 2^n input lines to one output based on the value on 'n' select lines. The Boolean expression for output of 2:1 multiplexer is given by (2)

$$OUT = \bar{S}_0 I_0 + S_0 I_1 \quad (2)$$

The existing 2:1 multiplexer architectures are shown in Fig. 1 and 2. Recently proposed QCA multiplexer design [23] shown in Fig.1 (a). It has 17 QCA cells, 0.02 by μm^2 area and 2 clock zones latency. The design shown in Fig.1(b)[14], consists of 27 cells, 0.03 μm^2 area and 3 clock zones. The other structure shown in Fig. 1(c) [17], takes 26 cells, 0.02

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μm^2 area and 2 clock zones latency. The design in Fig. 1(d) [19] uses 22 cells, 0.02 μm^2 area and 2 clock zones. Fig. 1(e) design [20] needs 15 cells, 0.02 μm^2 area and 2 clock zones. The structure in Fig.1 (f) [7] has 36 cells, 0.04 μm^2 and 4 clock zones. The design in Fig.1 (g) [5], has 46 cells, 0.06 μm^2 and 4 clock zones. The multiplexer in Fig.1 (h) [8] requires 67 cells, 0.11 μm^2 and 4 clock zones. The structure shown in Fig.1 (i)[15], consists of 23 cells, 0.03 μm^2 and 3 clock zones. Another multiplexer shown in Fig.2(a) [16], consists of 57 cells, 0.09 μm^2 area and 4 clock zones. The other 2:1 mux as in Fig.2 (b) [18], has 25 cells, 0.03 μm^2 area and 3 clock zones latency. The structure shown in Fig. 2(c) [9], has 34 cells, 0.04 μm^2 area and 4 clock zones. Fig.2 (d) shows another design [13] with 49 cells, 0.06 μm^2 area and 2 clock zones latency. The structure shown in Fig.2 (e) [6] has 80 cells 0.12 μm^2 and 4 clock zones. The multiplexer structure presented in Fig.2 (f) [12] consists of 34 cells, 0.05 μm^2 and 4 clock zones.

To implement 2:1 multiplexer, three majority gates and one inverter is necessary. The 2:1 multiplexer with majority gate function can be expressed as (3)

$$OUT = M(M(I_0, S, 0), M(I_1, S, 0), 1) \quad (3)$$

Performance of the any digital design is measured by the following characteristics [26].

i) Cell count:

The number of QCA cells used for the design.

ii) Design Area:

The area occupied by the design. This area is displayed on the software tool QCA Designer 2.0.3 window once the design has selected by cursor. Design Area is expressed in μm^2

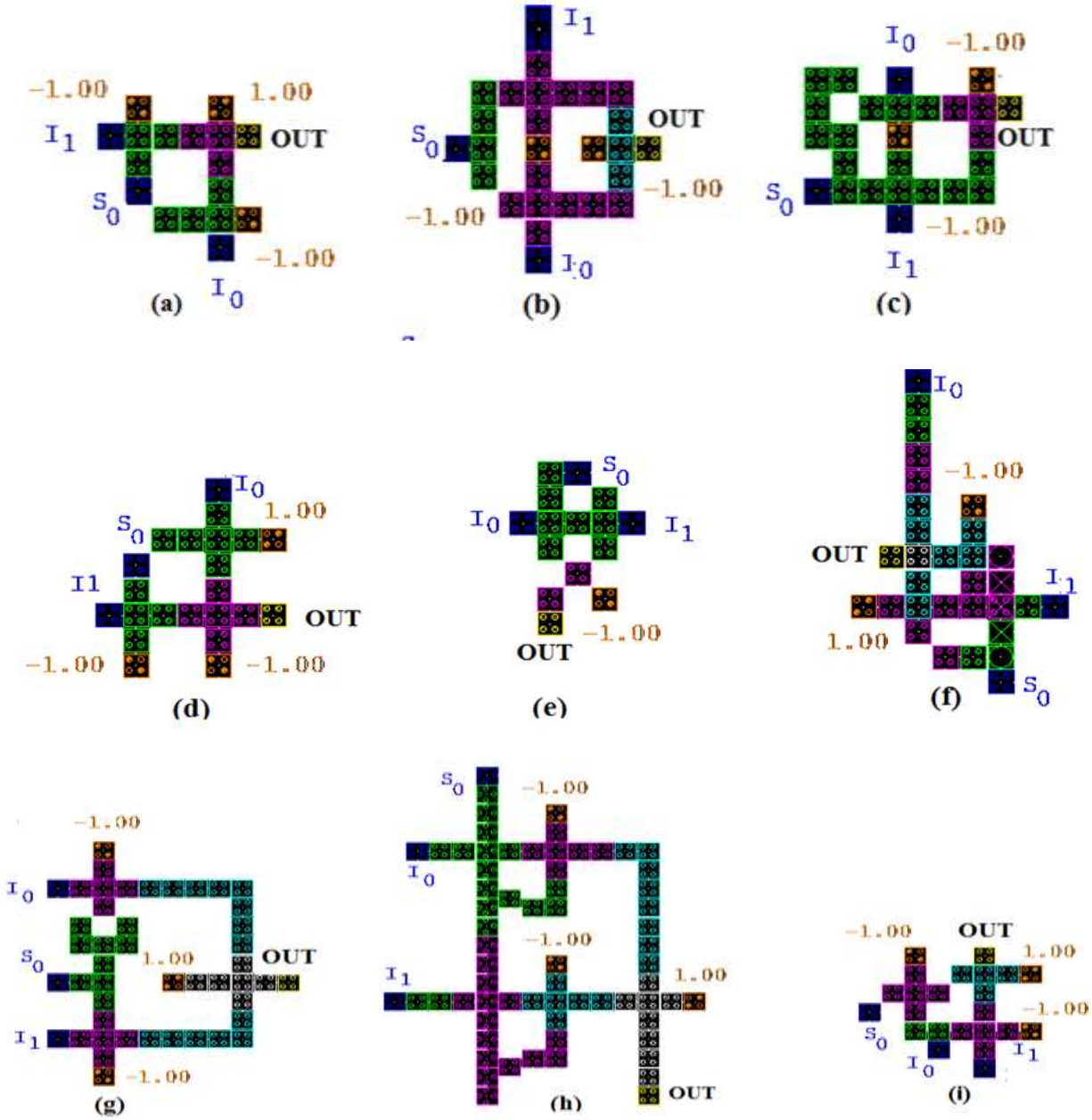


Fig.1. Existing QCA based 2:1 multiplexer; (a) [23], (b) [14],(c) [17], (d) [19], (e)[20] ,(f) [7], (g) [5], (h) [8], (i) [15].

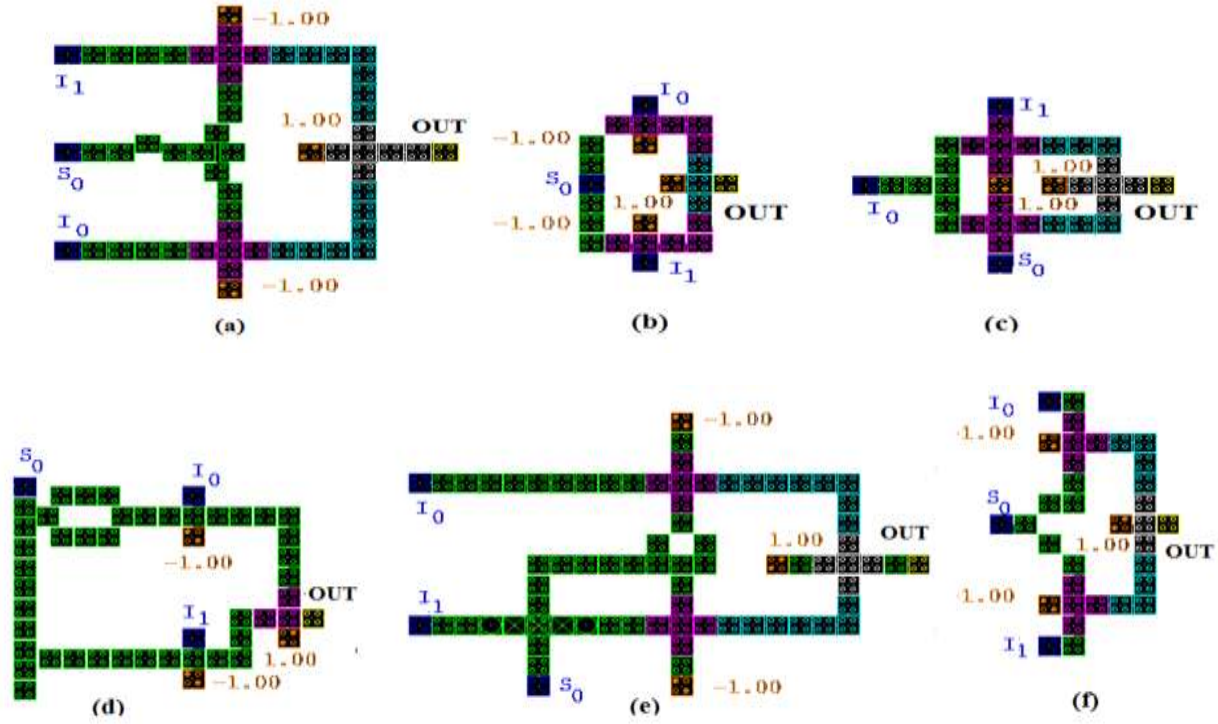


Fig.2. The existing QCA based 2:1 multiplexer designs (a) [16], (b) [18], (c) [9], (d) [13], (e) [6] and (f) [12]

iii) Ratio:

Provides the information regarding the amount of improvement has been made with respect to existing design. There are two types of ratios.

a) The ratio calculated with cell count information i.e improvement made in terms of number of QCA cells. b) Ratio with respect to the design area i.e the improvement in terms of design area.

iv) % design area improvement:

The information about the percentage of improvement in the proposed design area relative to existing design and is calculated by the formula

$$\%\ improvement\ in\ dessign\ = \frac{existing\ design - proposed\ design}{existing\ design} \times 100 \qquad (4)$$

v) Latency:

The time that the design takes to produce output after execution is the Latency and is expressed in terms of clock zones or clock cycles.

vi)Cost:

The performance of the system can also be measured by cost which is given by (5)

$$Cost = Dessign\ Area\ \times Latency \qquad (5)$$

Significance of the cost reduction implies that either area occupied or the latency (time delay) of the design to produce the output is small or both are small.

IV. THE PROPOSED MULTIPLEXER

Initially, unique ultra-efficient 2:1 MUX structure has been proposed, then 4:1 and 8:1 MUX structures has been designed using proposed 2:1 structure.

a) Proposed 2:1 Multiplexer:

Proposed 2:1 MUX makes uses inherent characteristics of the cell to perform the functionality of multiplexer and is required 12 QCA cells, 0.01 μm^2 design area and one clock zone. The majority gate representation, schematic, block diagram, and QCA design is shown in Fig.3.

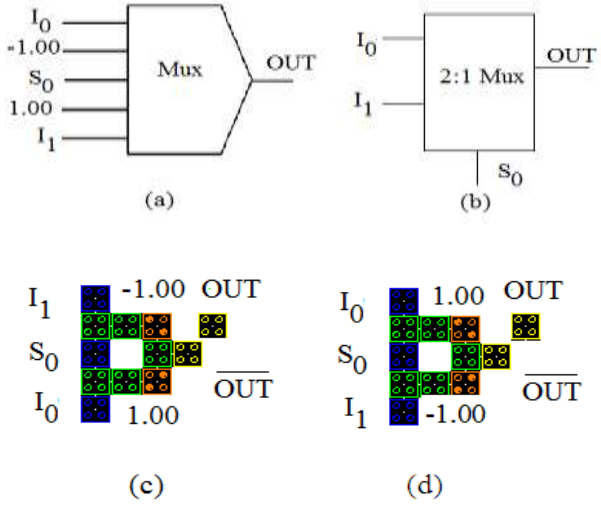


Fig.3 Proposed 2:1 MUX (a) Majority gate representation (b) Block diagram (c) QCA layout.

The design has two inputs 'I_0 & I_1', one output 'OUT' and one selector signal 'S' based on which one of the input is selected to the output. The output of the multiplexer is "I_0" when S=0 and "I_1" when S=1 as shown in truth table1.

b) 4:1 MUX Design:

Proposed 4:1 MUX has been generated by replicating the proposed 2:1 MUX. This takes 49 QCA cells, 0.06 μm^2 design area and 0.75 clock cycle (3 clock zones). The contains four inputs I_0,I_1,I_2,I_3 and two selectors S_1, S_0 and one output OUT as shown in Fig.4 Truth table for 4:1 MUX is in the table 2. 4:1 MUX Implementation with majority gate is in Fig.4 (a). Block diagram with 2:1 MUX and QCA layout are in Fig.4 (b) and Fig.4(c) respectively. The logic expression is given by (6)

$$OUT = \bar{S}_1\bar{S}_0I_0 + \bar{S}_1S_0I_1 + S_1\bar{S}_0I_2 + S_1S_0I_3 \quad (6)$$

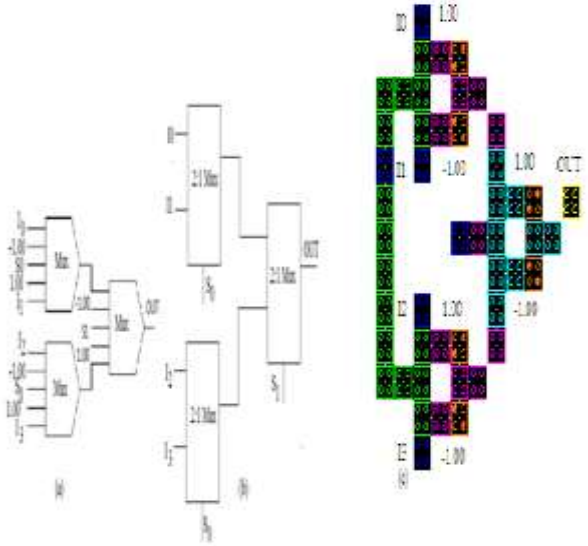
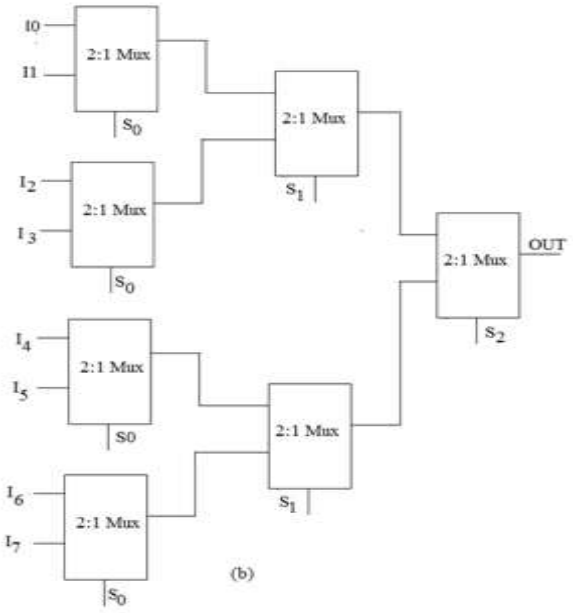


Fig.4.The proposed 4:1 MUX (a) majority gate representation (b) Block diagram (b) QCA layout.



c) 8:1 MUX Design:

8:1 MUX has been generated by replicating the proposed 2:1 MUX, it has 156 QCA cells, 0.20 μm^2 design area and 1.5 clock cycle (6 clock zones). The design has 8 inputs (I_0, I_1, I_2, I_3, I_4, I_5, I_6, I_7) , 3 selectors (S_2, S_1, and S_0) and one output OUT as shown in Fig.5. From the truth table the MUX OUT signal is equal to I_0, I_1, I_2, I_3, I_4, I_5, I_6, and I_7 when the decimal form of S_2, S_1, and S_0 is equal to "0", "1", "2", "3", "4", "5", "6", and "7" respectively. Output of the MUX is one of the inputs based on selector lines as in the truth table 3. The majority gate representation, schematic of 8:1 MUX using 2:1 MUX and QCA design layout are in Fig.4 (a), (b) and (c) respectively. Its Boolean expression for OUT is given by (7)

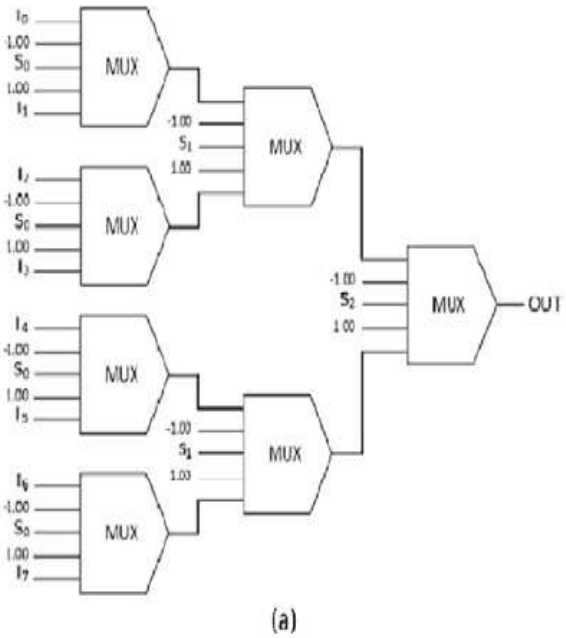
$$OUT = \bar{S}_2\bar{S}_1\bar{S}_0I_0 + \bar{S}_2\bar{S}_1S_0I_1 + \bar{S}_2S_1\bar{S}_0I_2 + \bar{S}_2S_1S_0I_3 + S_2\bar{S}_1\bar{S}_0I_4 + S_2\bar{S}_1S_0I_5 + S_2S_1\bar{S}_0I_6 + S_2S_1S_0I_7 \quad (7)$$

Truth tables: Table 1-2:1MUX Table 2- 4:1 MUX Table 3- 8:1 MUX

S_0	OUT
0	I_0
1	I_1

S_1	S_0	OUT
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

S_2	S_1	S_0	OUT
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7



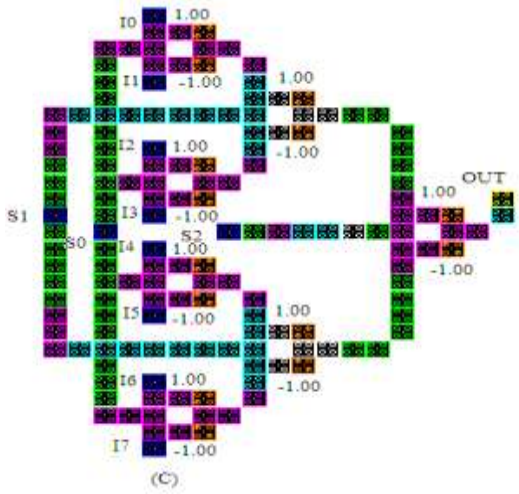


Fig.5. 8:1 MUX (a) Majority gate representation (b) Block diagram (c) QCA layout.

V. RESULTS AND DISCUSSIONS

The results of all the proposed designs and earlier designs have discussed. Bistable approximation is used for supplying input combinations with the following parameters: The dimensions of each QCA cell is 18nm in all sides, diameter of quantum dot is 5 nm, number of samples 12800, relative permittivity 12,900, maximum iterations in each sample 100, clock high 9.80000e-^{22}J and clock low is 3.80000e-^{23}J, amplitude factor of the clock is 2.0000, radius of effect is 65nm and convergence tolerance 0.0010000. The simulation results of 2:1 MUX with uncomplemented and complemented forms of output are shown in Fig.6. The results and performance of the proposed 2:1 MUX and earlier MUXs have been presented in terms of cell count, area, Latency and type of wire crossing in the table 6 [5-8,14,16,17,19,21-23].

From the table 4, the proposed 2:1 MUX provides the best in terms of cell count, latency, area and cost compared to the earlier structures without any wire crossings either coplanar or multilayer [27]. Simulation results of 4:1 MUX have presented in Fig.8. The performance of proposed 4:1 MUX and previous MUXs are comparisons are in table 5 [5-8, 19, 21-23]. The simulation results of 8:1 MUX have been presented in the Fig.8 [5,13,20-23]. Result of proposed 8:1 MUX and previous MUXs are presented in table 6 and the simulation results are shown in Fig.9. Thus the proposed 8:1 MUX affords good improvement in the cell count, design area, latency and cost. From tables, the proposed 2:1 MUX has an improvement of 29% in the cell count, 50% in the design area and an improvement of 75% in the cost compared to best existing MUXs. As well as the proposed 4:1 MUX provides 76% improvement in the design area,77% in the cell count and 88% improvement in the cost relative to best existing 4:1 MUXs. Also the proposed 8:1 MUX shows an improvement of 73% in the cell count, 76% in the design area and 33% in the cost relative to best existing 8:1 MUXs.

VI. CONCLUSION

The proposed ultra efficient 2:1 MUX takes the advantages of inherent characteristics of quantum technology to create desired output, the proposed one provides better speed, occupies less area and significantly more robustness than the previous designs. 4:1 MUX and 8:1 MUX are implemented by exploiting the proposed 2:1 MUX. It has been shown that, the proposed design provides much improvement in cell count, design area, latency and cost compared to previous QCA MUXs. Implementation and simulation of proposed designs are performed using QCA Designer-2.0.3[3].

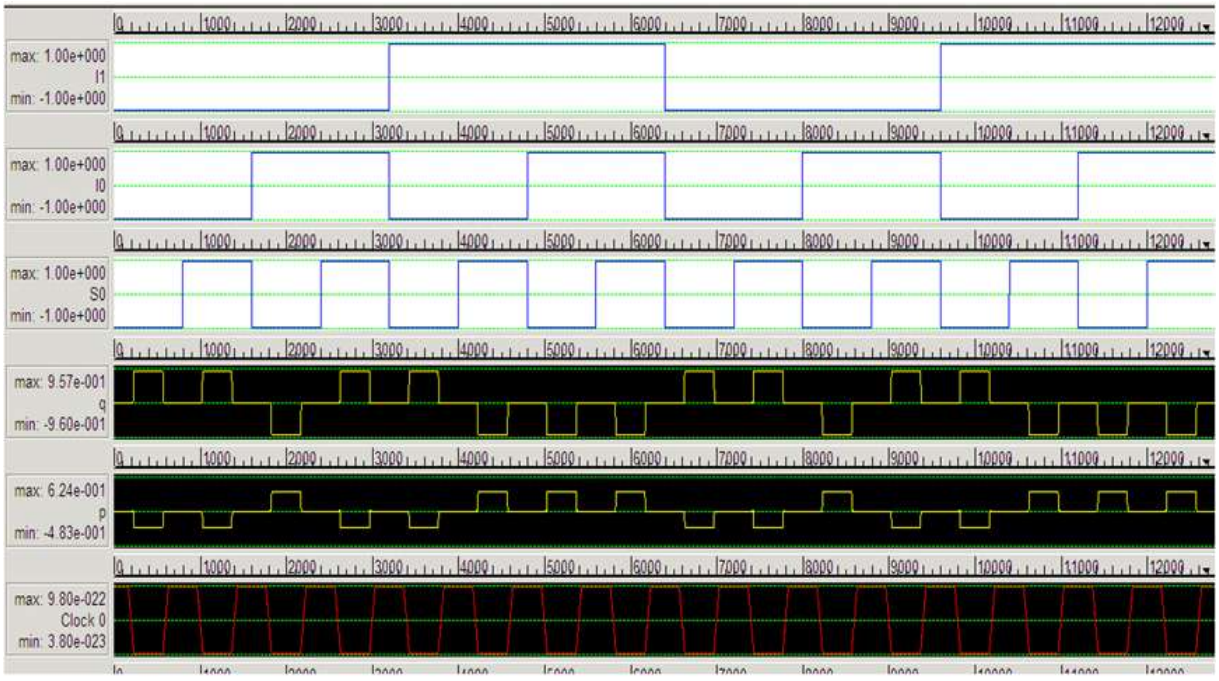


Fig.7.The simulation result of proposed 2:1 MUX

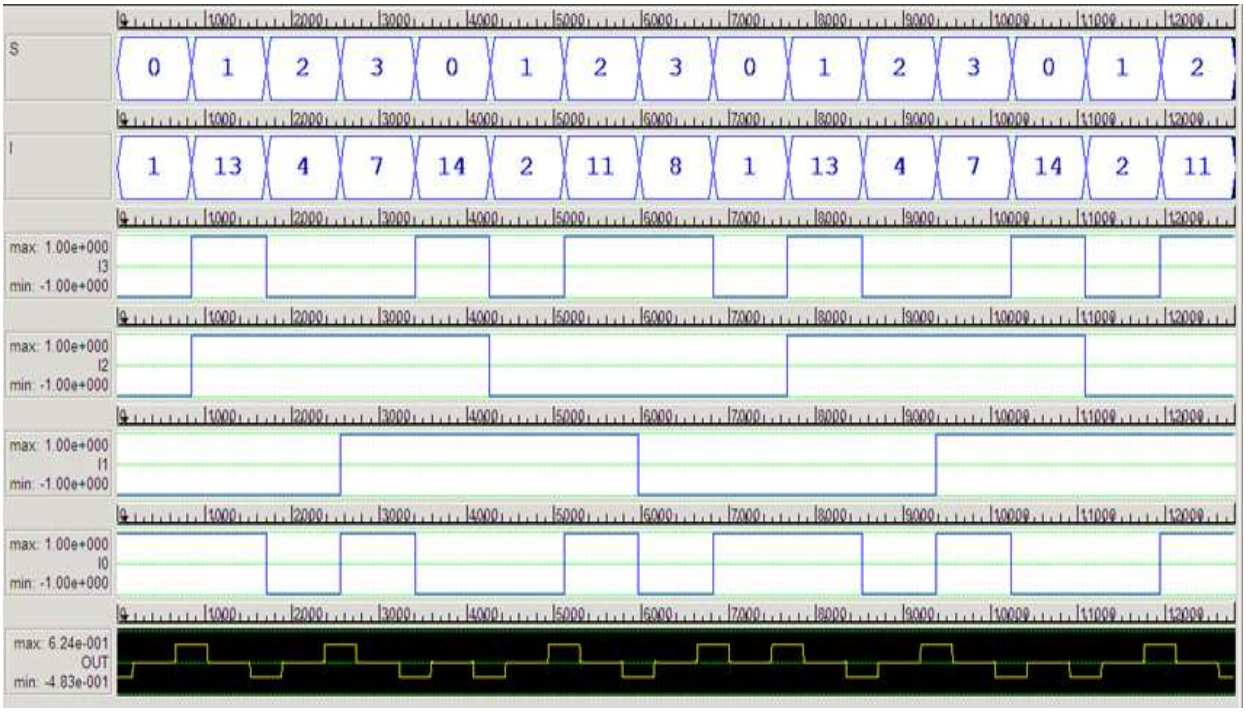


Fig.8. The simulation result of proposed 4:1 MUX

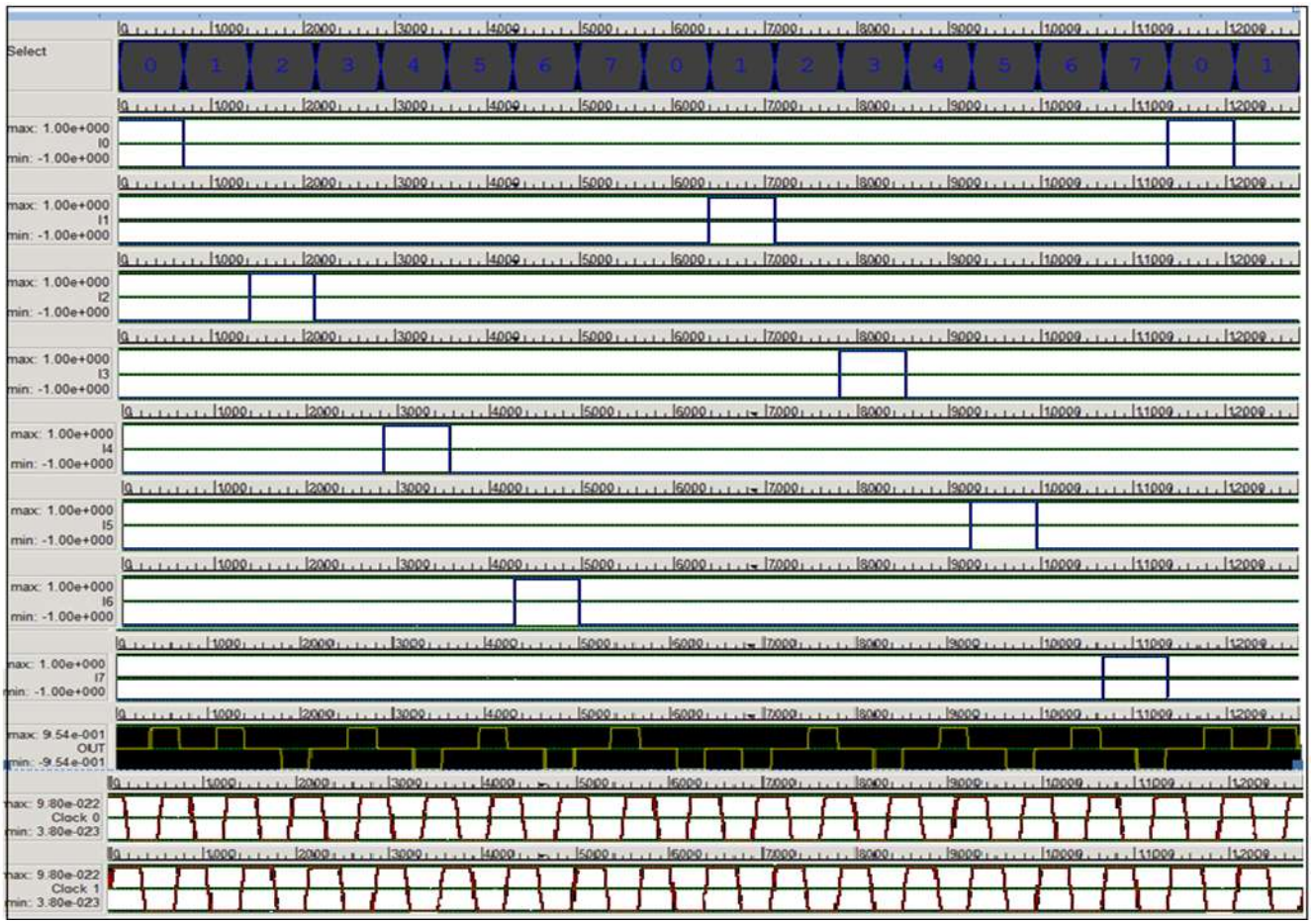


Fig.9.The simulation result of 8:1MUX

Table 4:The Comparison of performance for the 2:1 MUX architectures

Structure	Number of cells	Ratio	Design Area μm^2	Ratio	Percentage Reduction in design area	Latency in clock zones	Clock cycles	Wire crossing	Cost= Design Area * latency (in clock cycles)
Proposed	12	1	0.01	1	-	1	0.25	Coplanar	0.0025
[23]	17	1.41	0.02	2	50	2	0.5	coplanar	0.01
[14]	27	2.25	0.03	3	67	3	0.75	coplanar	0.0225
[17]	26	2.16	0.02	2	50	2	0.5	Coplanar	0.01
[19]	22	1.83	0.02	2	50	2	0.5	Coplanar	0.01
[20]	15	1.25	0.02	2	50	2	0.5	Coplanar	0.01
[7]	36	3	0.04	4	75	4	1	Multilayer	0.04
[5]	46	3.83	0.06	6	83	4	1	Coplanar	0.06
[8]	67	5.58	0.11	11	91	4	1	Coplanar	0.11
[15]	23	1.92	0.03	3	67	3	0.75	Coplanar	0.0225
[16]	57	4.75	0.09	9	89	4	1	Coplanar	0.09
[18]	25	2.08	0.03	3	67	3	0.75	Coplanar	0.0225
[9]	34	2.83	0.04	4	75	4	1	Coplanar	0.04
[13]	49	5.58	0.06	6	83	4	1	Coplanar	0.06
[12]	34	2.83	0.05	5	80	4	1	Coplanar	0.05
[6] using QCA LG	140	12.2	0.28	28	96	8	2	Multilayer	0.56
[6] using Handmad	80	7.33	0.12	12	92	4	1	Multilayer	0.12

Table 5: The Comparison of performance for the 4:1 MUX architectures:

Structure	Number of cells	Ratio	Design Area μm^2	Ratio	Percentage reduction in design area	Latency in clock zones	Clock cycles	Wire crossing	Cost= Design Area * latency (in clock cycles)
Proposed	49	1	0.06	1	-	4	0.75	coplanar	0.045
[8]	215	4.39	0.25	4.17	76	6	1.5	coplanar	0.375
[10]	124	2.53	0.25	4.17	76	8	2	coplanar	0.5
[29]	223	4.55	0.22	3.67	73	6	1.5	Multilayer	0.33
[25]	251	5.12	0.2	3.33	70	5	1.25	Multilayer	0.25
[25]	199	3.75	0.27	4.50	78	6	1.5	coplanar	0.405
[11]	290	4.06	0.35	5.83	83	7	1.75	coplanar	0.6125
[17]	271	5.53	0.37	6.17	84	19	4.75	coplanar	1.7575
[19]	155	3.16	0.24	4.00	75	5	1.25	coplanar	0.3
[20]	107	2.18	0.15	2.5	60	4	1	coplanar	0.15

Table 6: The Comparisons of performance for proposed and existing 8:1 MUX structures

Structure	Number of QCA cells	Ratio	Design Area μm^2	Ratio	Percentage reduction in design area	Latency in clock zones	Clock cycles	Wire Crossing	Cost= Design Area * latency(in clock cycles)
Proposed	156	1	0.20	1	-	6	1.75	Coplanar	0.35
[24]	576	3.69	0.82	4.1	76	9	2.25	Coplanar	1.845
[25]	608	3.89	0.71	3.55	72	9	2.25	Multilayer	1.5975
[25]	494	3.17	0.58	2.9	65	9	2.25	Coplanar	1.305
[11]	633	4.06	0.67	3.35	70	11	2.75	Coplanar	1.8425
[17]	1312	8.41	1.83	9.15	89	42	10.5	Coplanar	19.215
[19]	462	2.96	0.87	4.35	77	7	1.75	Coplanar	1.5225
[20]	293	1.88	0.58	2.9	65	6	1.5	Coplanar	0.87

VII. ACKNOWLEDGMENT

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