An Optimized Counter Design using T Flip-Flop in Quantum-Dot Cellular Automata Technology

Adepu Hariprasad, Sumanth Kumar Chennupati

Abstract— Conventional CMOS technology have lot of limitations and serious challenges threat this technology when scaled to a nano-level. Several alternative technologies have been proposed as solutions to overcome limitations and challenges encountered by CMOS. Quantum dot-cellular automata (QCA) is an emerging nanotechnology for the development of logic circuits such as combinational and sequential circuits.QCA seems to be best alternative to the conventional complementary metal-oxide semiconductor (CMOS) technology.QCA is a new computing paradigm in nanotechnology that can implement digital circuits with outstanding features such as ultralow power consumption, faster switching speed and extremely density structure . In this paper , a novel area efficient and optimized QCA layout design of sequential circuit T flip flop is proposed by which the QCA layout area has reduced by 57% , cell count improved by 56% in comparison with the earlier best designs. The use of proposed T flip flop in designing sequential circuits like synchronous 2 bit up counter,3 bit up counter and 4 bit up counter has reduced the QCA layout area by 65%,64% and 68% respectively where as QCA cell count are reduced by 53%, 62% and 59%.. The sequential circuits flip flop and counters are designed using three input XOR gate and are implemented by QCA layout. The paper also present the use of proposed T flip flop designed with 3 input XOR gate in designing not only synchronous binary up counters but also in synchronous binary down counter provides a significant reduction in the hardware and complexity than the existing methods. These circuits are simulated using computer aided design tool QCA Designer 2.0.3, which is a design and simulation tool for quantum dot cellular automata. The aim is to maximize the circuit density and focus on a QCA layout that uses minimal number of cells.

Keywords— CMOS,Logic gates, Latency, Nanotechnology, Quatnum-dot Cellular Automata (QCA), T flip flop, counters;

I. INTRODUCTION

According to the Intel cofounder Gordon Moore's law, the growth of number of transistors on a single chip will double in every 18 months. According to his prediction, the conventional CMOS based devices have been advanced from micron to submicron, submicron to deep submicron and to nanometer regime over last five decades[1]. But the scaling of CMOS devices at nano scale is affected by several limitations and challenging factors like leakage current, power dissipation, area overhead, noise margin, speed, error analysis problems (Difficulties in generation of DFTs) and oxide thickness. According to the high rate of shrinkage in dimensions of conventional CMOS circuits more and more devices are packed into the same area so that the heat generated can no longer dissipate and results in damage of chip. These limitations and challenges increase with the greater circuit complexity as we move to higher level of system integration .In order to overcome conventional CMOS scaling limitations and physical challenges ,the best suitable replacement for the CMOS technology has become an inevitable necessity. International Technology Roadmap for Semiconductors (ITRS) has Identified some novel nano electronic technologies to replace current transistor based technology in future. Single Electron Transistor (SET),Quantum dot Cellular Automata (QCA), Resonant Tunneling Diodes (RTD) are some of the novel nano-electronic technologies. Among all these technologies QCA seems to be robust and suitable new computing technology to overcome the scaling limitations of CMOS devices at nano-scale [2].The objective of this paper is to propose a detailed analysis and design strategy for a simple T flip-flop based sequential circuits for QCA implementation. The proposed designs are based on a simple T-type flip-flop constructed by a QCA cells and binary wire with four clocking zones. The rest of the paper is organized as follows: Section 2 present a background of QCA technology and clocking requirements. Section 3 provides earlier design and implementation of T flip flop and counters of various sizes using T flip flop . In Section 4, proposed novel design of an area efficient QCA T flip flop and its appllication to design sequential circuits such as various counter sizes such as 2 bit, 3bit and 4 bit counters are presented and followed by simulation results. In Section 5, comparison table of earlier design and proposed designs have been shown. The last section 6 contain conclusions followed by references.

II. QUANTUM-DOT CELLULAR AUTOMATA (QCA) BACKGROUND

The basic unit of QCA is the QCA cell consists of four quantum dots which are positioned at the vertices of a square and two mobile electrons are introduced in the cell that can move between diagonal positioned quantum dots situated at farthest from each other in the QCA cell by means of electron tunneling. The position of the logic state is encoded as position of electrons with in a cell. This novel idea was first proposed by Dr. Craig Lent in the year 1993 [2].The electrons can only occupy the quantum dots located at corners of QCA cell as a result of Coulombic repulsion force as shown in Fig.1.(a).Depending on the direction of position of electrons

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that reside in opposite corners in the quantum dots within the cell,it results in the two different polarizations either +1 or -1 as shown in Fig. 1. when the two qca cells are positioned together, The presence of high potential barrier impede the tunneling of electrons between the two cells. When the two cells are placed together, the Coulombic interaction between the electrons forces the cell to acquire a particular polarization either +1 or -1 [3,4].The polarization of any cell can be defined as

$$p = \frac{(p1 + p3) - (p2 + p4)}{p1 + p2 + p3 + p4} \qquad (1)$$

.

The equation (1) shows how the polarization of a cell is calculated. Here polarization P_i is the charge of the i th quantum dot [14]. The presence of an electron in a particular quantum dot is represented by P_i='1' and its absence by P_i='0'.These polarizations are represented by logic '1' and logic '0' or in other words binary '1' and binary '0' respectively as shown in Fig.1.(b). The arrangement of quantum dots in the middle of the edges of QCA cell is called symmetric cells used for representing binary information as shown in Fig.1.(c).

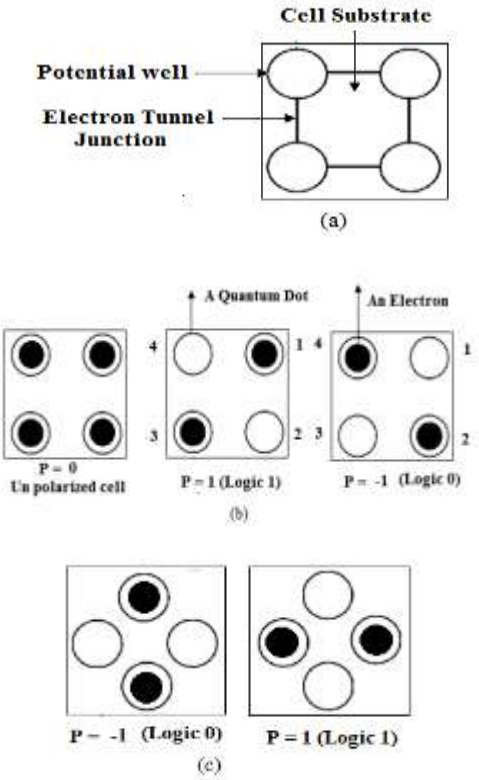


Fig.1. (a) Anatomy of QCA cell (b) Binary representation of QCA cell (c) Symmetric QCA cell

QCA logic : The fundamental elements for QCA logic implementation are majority gate and inverter which compute data based on Coulomb repulsion force of interactions. The majority gate comprise five QCA cells. Cells named A, B, and C are the input cells, and cell D is the output cell whose polarization according to the majority of polarization of the input cells. QCA majority gate layout and its logic symbol are shown in Fig. 2(a) and Fig.2(b). By assigning a fixed polarization either -1(binary 0) or +1 (binary 1) to the one of the input of the majority gate make it to function as AND gate or OR gate as shown in equation (3) and (4). The logic function of a majority gate and its truth table are given by as shown in equation (2) and table 1 respectively.

$$M(A, B, C) = AB + AC + BC \qquad (2)$$
$$M(A, B, 0) = A\,B \qquad (3)$$
$$M(A, B, 1) = A + B \qquad (4)$$

Table 1: Truth table of Majority gate

Inputs			Output
A	B	C	M(A,B,C)
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

.The simplest inverter is built by placing QCA cells in a diagonal structure also called corner inverter as shown in Fig.2.(c). The robust form of inverter is built by taking arrangement of QCA cells as shown in Fig. 2(d).As the output of the NOT gate is complement of the input, the polarization of the output QCA cell is reverse to the polarization of input QCA cell .

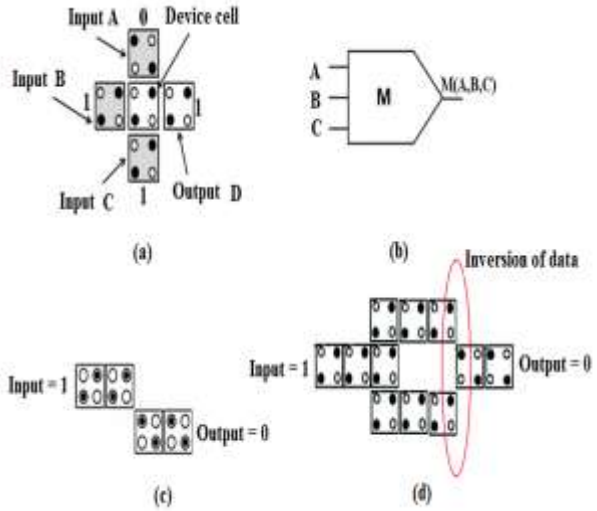


Fig.2 (a) Majority gate (b) Schematic symbol (c) corner inverter (d) robust inverter

QCA wire: The QCA wire is formed by an array of QCA cells through which the logical information is transferred from one place to another place [9]. In order to transfer logical data either logical 0 or logical 1, the corresponding polarization is maintained in accordance with the binary data to be transmitted in an ordinary QCA wire where as in QCA wire in which the symmetric cells are used carries opposite polarization relative to previous or driver cell [6]. Fig.3. shows how QCA wire is produced by an array of QCA cells and symmetric cells [18].

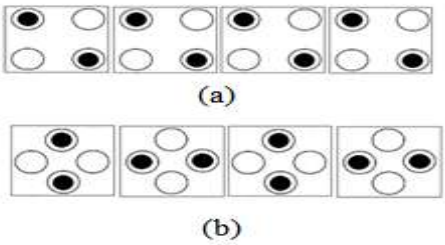


Fig.3.(a) shows an ordinary QCA wire (b) QCA wire using symmetric cells

QCA Clocking: In QCA, the clock is used mainly to propagate signal from one place to another place through cells as well as for synchronization of data. The clock is also used for controlling electron tunneling potential barrier between inter quantum dots inside the QCA cell. A QCA circuit is partitioned into four clock phases.The clock phases which are adjacent 90^0 out of phase from each other and non-adjacent clock phases are 180^0 out of phase from each other.These four clock phases are called as Switch, Hold, Release and Relax [10]. During the first phase of clock known as switch phase, QCA cells remain unpolarized and their inter dot potential barriers become low. The barriers are allowed to increase during the switch phase and the QCA cells become polarized according to the state of their neighbour driver cell. Switch phase is the clock phase in which the actual computation or switching takes place. At the end of switch clock phase, barriers are adequately high enough to avoid any electron tunneling and cell states become fixed. During the second phase named hold phase, barriers are sufficiently high so that outputs of the subarray cells can be used as inputs to the next stage. In the third phase, release phase, barriers are lowered and cells are allowed to relax to an unpolarized state. Finally, during the fourth clock phase, the relax phase, cell barriers remain at their lowest levels and cells remain in an unpolarized state [5,19] . In the meantime, the large scale QCA circuit is partitioned into four clock zones; The clock cycle then starts over again with the switch phase and the same process is repeated till the end of the last cell of qca layout [22].

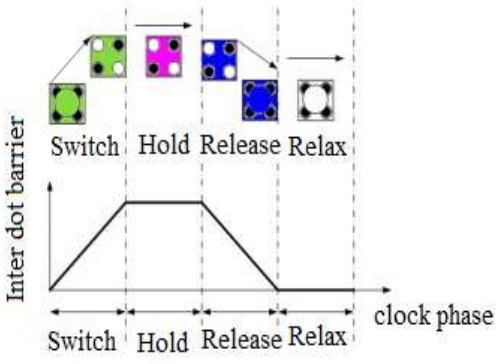


Fig.4. Four phases of the QCA clocking

clock 0 clock 1 clock 2 clock 3

QCA cells four clock zones

III. EXISTING T FLIP FLOP AND QCA COUNTER STRUCTURES

A digital system which is used for counting pulses is called counter. The Counter is a sequential circuit which will go through a certain predefined states either counting up or counting down based on the application of input sequence of pulses. Counters are the fundamental components of digital systems. Counters consists of a set of flip flop connected in an appropriate manner used to count the sequence of the input pulses [13]. The basic element used to construct counter and shift register is flip flop.As the size of QCA layout for T flip flop is reduced, obviously not only the cell count but also the QCA layout area and delay is also signigficantly reduced. Here, the previous best T flip flop QCA layout designs and QCA counter structures of various sizes 2 bit, 3 bit and 4 bit counters using T flip flop are presented.

Here a novel T flip flop made up of three input XOR gate has been proposed to model synchronus up counter which counts in the upward direction and synchronus down counter which counts in downward direction.Counters of various sizes 2bit , 3bit and 4 bit are implemented with the serial connection of proposed T flip flop. All these proposed counters are compared against the earlier best existing models in terms of number of cells, area occupied by cell and latency to illustrate that all the proposed counters are much optimized and area efficient over the best existing models. Both the up counter, down counter as well as the fundamental device of counter T flip flop is implemented in QCA using computer aided design tool QCA Designer 2.0.3.

T flip flop: T flip-flop is simpler in function compared to JK flip-flop as it only uses single input in its design [7]. T flip-flop holds its previous output as long as the input entered is logic 0 and toggle its previous output when the input entered is logic 1[16]. Here,The earlier best presented QCA structures of T flip-flop circuit have been shown[12].

The T flip flop presented in Fig.5.(a) need 43 cells an area of 0.04 μm^2 and 5 clock zones equal [20]. As 1 clock cycle is equal to 4 clock zones, 5 clock zones can be considered as 1 ¼ (1.25) clock cycles. T flip flop depicted in Fig.5.(b) [21] require 47 cells , 5 clock zones and an area of 0.048 μm^2. Fig.5(c) shows T flip flop which consists of 67 cells, 5 clock zones and an area of 0.08 μm^2 [15] . Another T flip flop circuit QCA layout comprises 58 cells, 5 clock zones and 0.056 μm^2 as shown in Fig.5(d) [24]. The T flip flop circuit which needs 108 cells, 5 clock zones and an area of 0.20 μm^2 is depicted in Fig.5(e) [8].

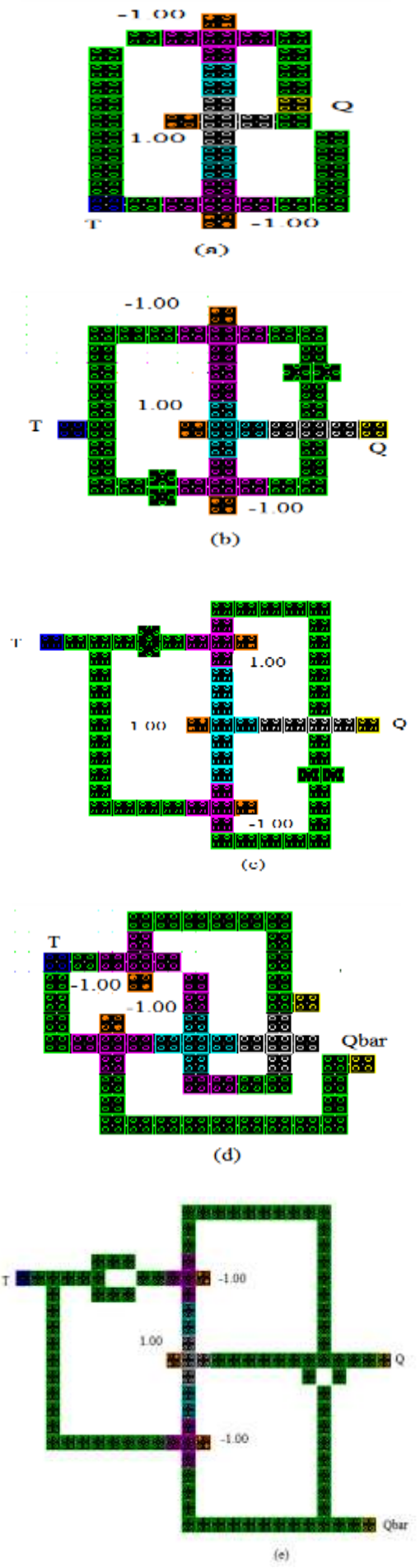


Fig.5.(a) T flip flop [20] (b) T flip flop [21] (c)T flip flop [15] (d) T flip flop [24] (e) T flip flop [8]

Existing 2 bit synchronus up counters:

The 2-bit synchronous up counter is a counter which counts 4 different binary states right from 00,01,10 and 11 (whose corresponding equivalent decimal values are equal to 0,1,2 and 3) respectively [12]. The synchronus 2 bit up counter is built by cascading two T flip-flops[7]. A T flip-flop is obtained by shorting together the two inputs of JK flip-flop. Output Q0 gives the least significant bit of the 2-bit counter.For every 2 cycles the output Q1 has to be comlemented to produce the most significant bit Q1.The output Q0 change for every clock pulse where as the output Q1 is complemented when output Q0 goes from logic 1 to logic 0 i.e. the output Q1 change after every two clock zones. The area efficient and optimized synchronus 2 bit up countes which are already existing have been depicted in the Fig.6. The 2bit counter which necessitate 140 QCA cells, , 0.17 μm^2 and 9 clock zones depicted in the Fig.6(a) [15].Another 2bit counter require 134 QCA cells, 0.18 μm^2 and 9 clock zones presented in the Fig.6(b) [8].The 2 bit counter need 92 QCA cells, 011 μm^2 and 13 clock zones as shown in Fig.6(c) [20].

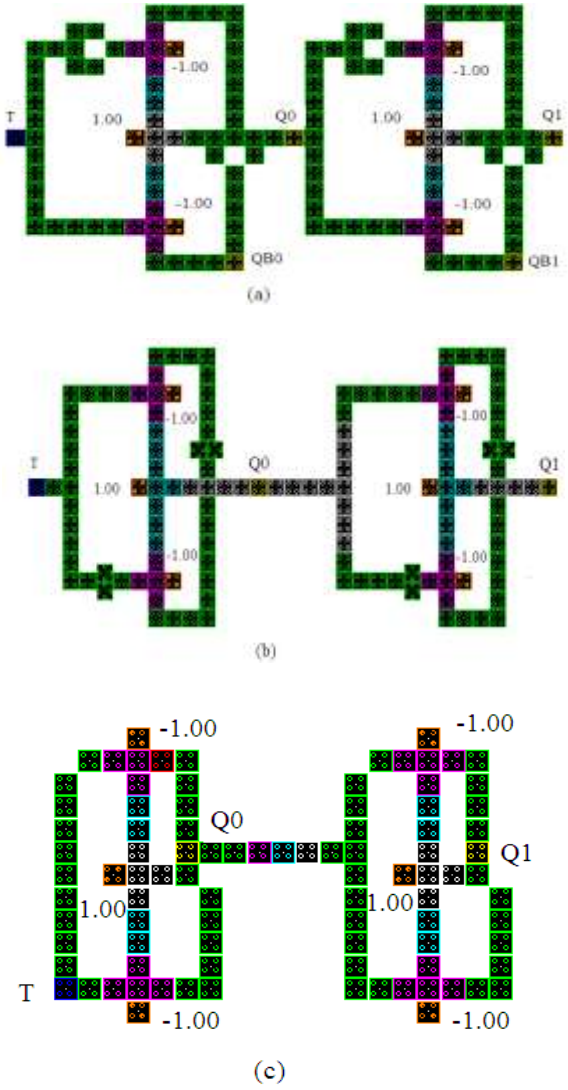


Fig.6.(a).Synchronus 2 bit counter [15] (b) Synchronus 2 bit counter [8] (c) Synchronus 2 bit counter[20]

Existing 3 bit synchronus up counters:

The 3-bit synchronous up counter is a counter which counts 8 different binary states right from 000, 001, 010, 011, 100, 101, 110 and 111 (whose corresponding equivelent decimal values are equal to 0,1,2,3,4,5,6 and 7) respectively.The synchronus 3 bit up counter is built by cascading serial connection of three T flip-flops[7]. Output Q0 gives the least significant bit of the 3-bit counter.For every 2 cycles the output Q1 is comlemented to produce the bit Q1.Every time the Q1 goes from 1 to 0,the output Q2 gets complemented.For every 4 clock pulses the output Q2 is complemented to produce the most significant bit Q2[17].The previous efficient synchronus 3 bit up counter which need 244 QCA cells, 0.33 μm^2 and 17 clock zones has been shown in Fig.7[15].

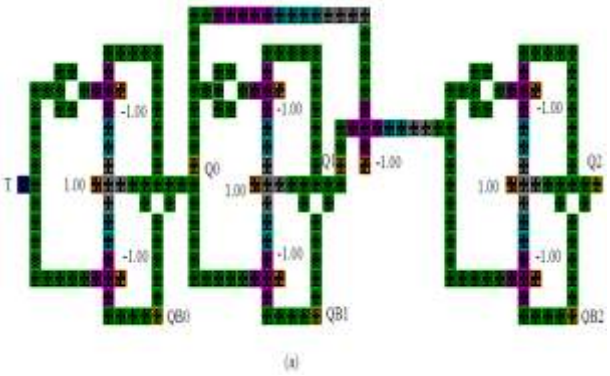


Fig.7.Synchronus 3 bit counter [15]

Existing 4 bit synchronus up counters:

The 4-bit synchronous up counter is a counter which counts 16 different binary states right from 0000, 0001, 0010, 0011, 0100, 0101,0110,0111,1000,1001,1010,1011,1100,1101,1110 and 1111 (whose corresponding equivalent decimal values are equal to 0,1,2,3,4,5,6 and 7) respectively.The synchronus 4 bit up counter is built by cascading serial connection of four T flip-flops. Output Q0 complements to each clock pulse which is known as the least significant bit of the 4-bit counter. Every time the output Q1 goes from 1 to 0, the output Q2 gets complemented.For every 4 clock pulses the output Q2 is complemented.Every time the Q2 goes from 1 to 0 the output Q3 gets complemented to produce the most significant bit Q3.Here, the earlier existing best synchronus 4 bit up counter which require 357 QCA cells, 0.57 μm^2 and 34 clock zones has been show has been depicted in the following Fig.7[8].

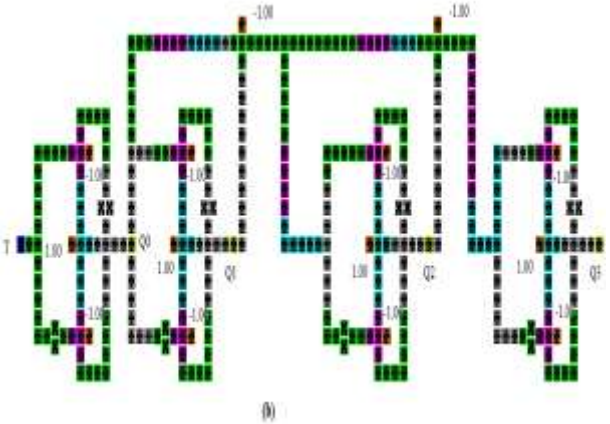


Fig.7.Synchronus 4 bit counter [8]

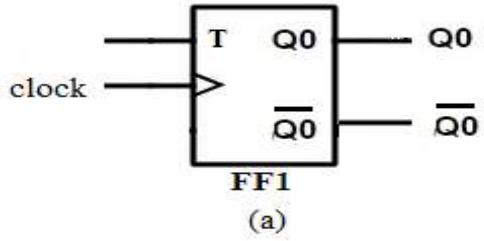
IV. PROPOSED QCA T FLIP FLOP AND QCA UPCOUNTER STRUCTURES

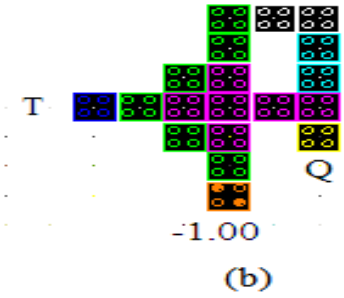
The proposed T flip flop is obtained by employing a 3 input XOR gate [23].When one of the its input is applied with polarizaton -1 the 3 input XOR gate functions as 2 input XOR gate as shown in Fig.8(b).

Proposed T flip flop: T flip-flop compared to JK flip-flop it only uses single input in its design. T flip-flop previous output Q0 gets toggled when input is held at logic 1 otherwise it holds its previous output. The proposed T flip flop require 19 cells, an area of 0.017 μm^2 and 4 clock zones as shown in Fig.8(b) [23]. The T flip flop schematic, QCA structure and its simulation results are shown in the following Fig.5.

The output of T flip is given by following equaton

$$Q0 = T\,\overline{Q0} + \overline{T}\,Q0 \qquad (5)$$





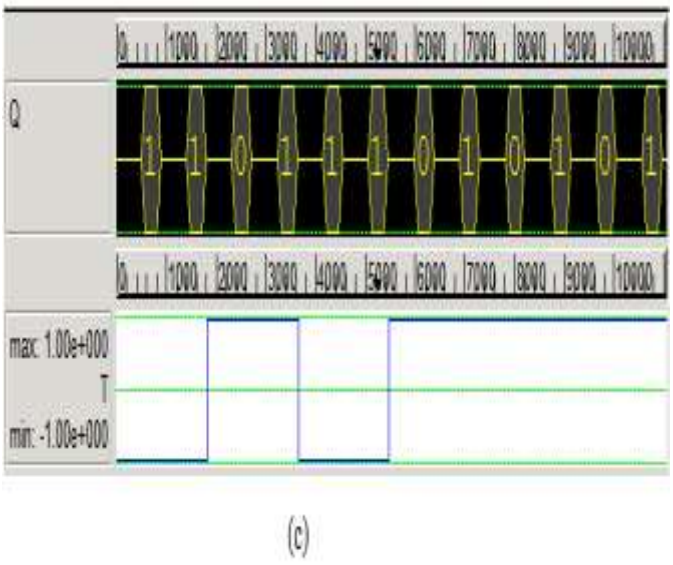
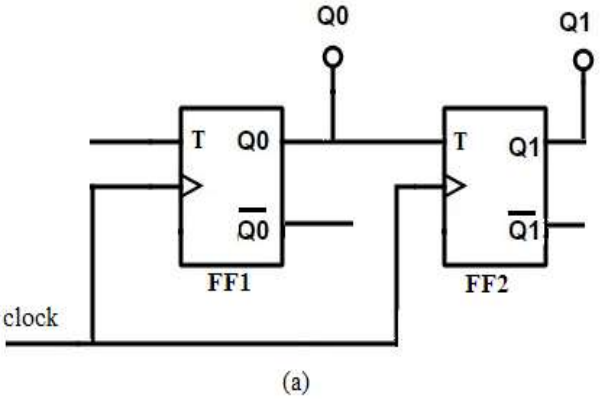
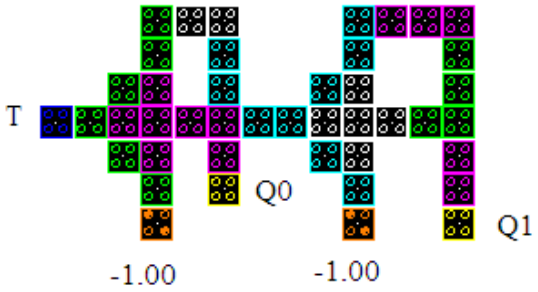


Fig. 8.(a) Schematic symbol of T flip flop (b) QCA structure of proposed T flip flop (c) its simulation reuslts.

Proposed 2 bit synchronus up counter: The 2 bit up counter is obtained by cascading 2 T flip flops in serial connection [11]. The 2 bit up counter with proposed T flip flop require 43 QCA cells, 0.038 μm^2 and 6 clock zones as depicted in the Fig.9(b).



(a)



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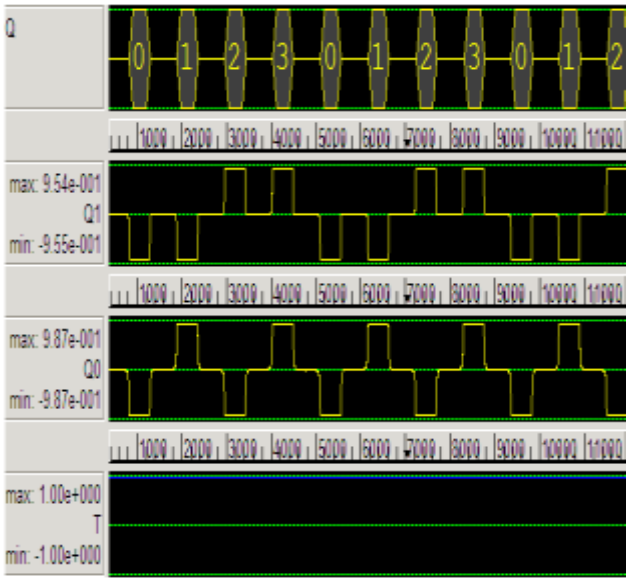
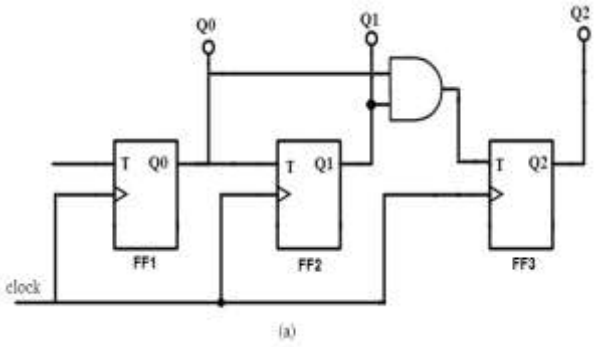


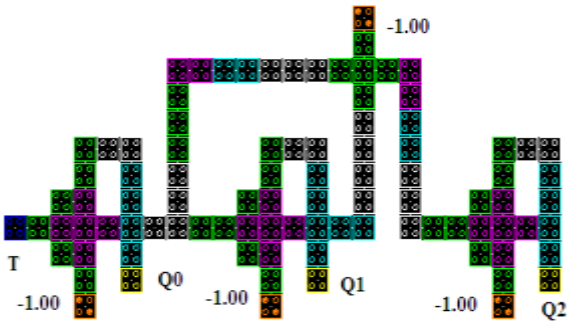
(c)

Fig. 9.(a) Block diagram of synchronus 2 bit up counter (b) QCA structure of 2 bit up counter using proposed T flip flop (c) Simulation reuslts of 2 bit up counter.

Proposed 3 bit synchronus up counter: The synchronous 3 bit up counter is attained by joining 3 Tflip flops serially as shown in Fig.10(a)[11]. The 3 bit up counter designed with proposed T flip flop require 93 QCA cells, 0.12 μm^2 and 16 clock zones as sown in Fig.10(b).



(a)



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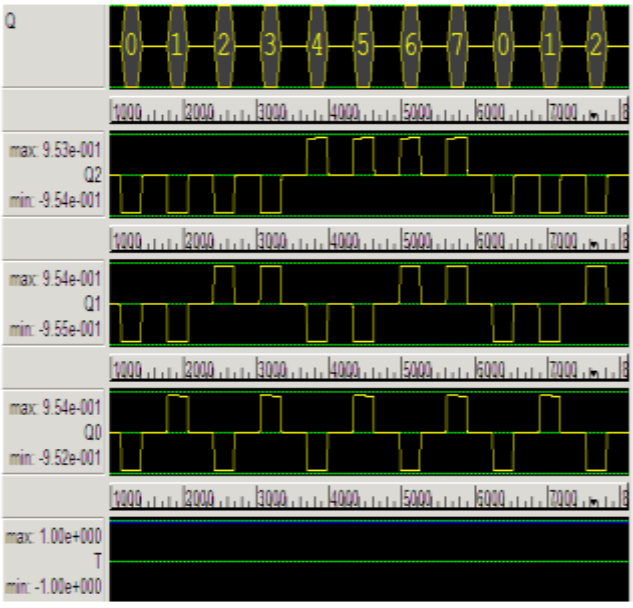


(c)

Fig.10.(a) Block diagram of synchronus 3 bit up counter (b) QCA structure of 3 bit up counter using proposed T flip flop (c) its simulation reuslts.

Proposed 4 bit synchronus up counter: the 4 bit up counter need 4 serially connected T flip flops[11].The 4 bit up counter designed with proposed T flip flops require 146 cells,0.18 μm^2 and 32 clock zones.The simulation results of the up counter have been shown with hexadecimal representation.

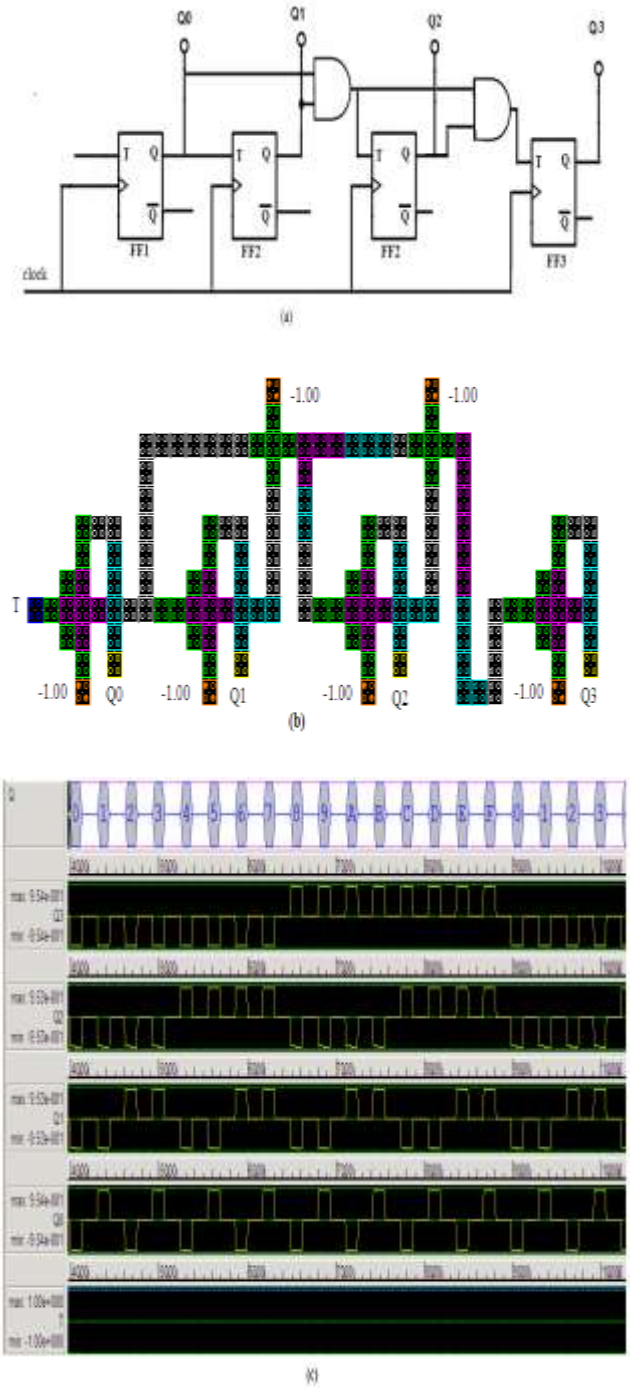


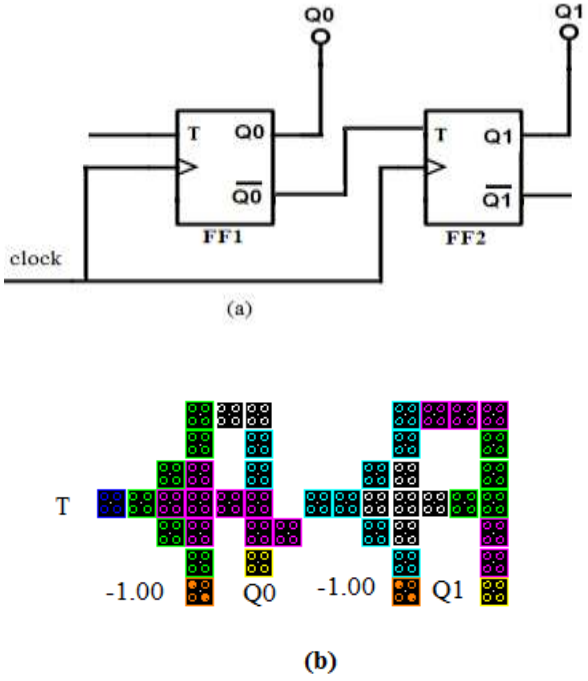
Fig.11.(a) Block diagram of synchronus 4 bit up counter (b) QCA structure of 4 bit up counter using proposed T flip flop (c) simulation reuslts.

Proposed QCA synchronous down counter structures:

synchronous down counters are formed by connecting flip-flops together and any number of flip-flops can be attached or "cascaded" simultaneously to form a "divide-by-n" binary down counter.

The proposed down counters are optimized much area efficient structures.

Synchronous 2 bit down counter: The 2 bit down counter operation is quite reverse to that of 2 bit up counter.The 2 bit up counter follows the sequence from 0 to 3 with an increment of 1 where as the 2 bit down counter follows the sequence in reverse direction right from maximum count to minimum count i.e. 3 to 0. The 2bit down counter with proposed T flip flop presented in the Fig,12(b) require 44 cells,0.04 μm^2 and 6 clock zones



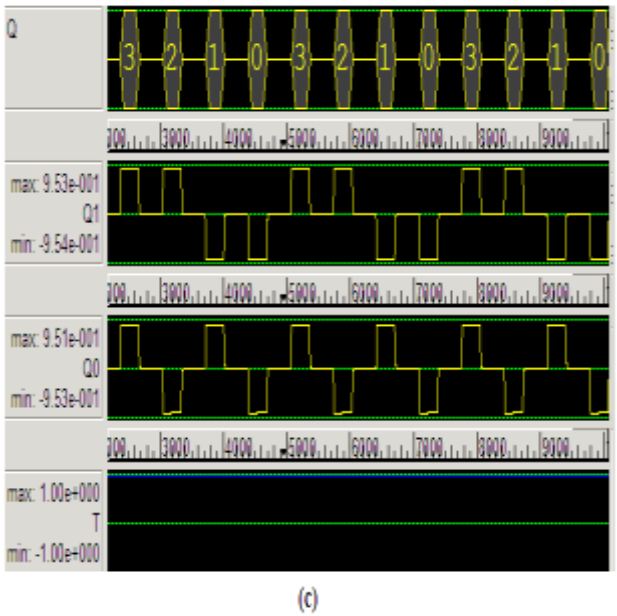


Fig.12.(a) Block diagram of synchronus 2 bit down counter (b) QCA structure of 2 bit down counter using proposed T flip flop (c) simulation reuslts.

Synchronous 3 bit down counter: The 3 bit down counter operation is opposite to the 3 bit up counter.The 3 bit up counter follows the sequence from 0 to 7 with an increment of 1 where as the 3 bit down counter follows the sequence in reverse direction right from maximum count to minimum count i.e. 7 to 0.The 3 bit down counter 95 QCA cells, 0.12 μm^2 and 15 clock zones depicted in the Fig.13(b).

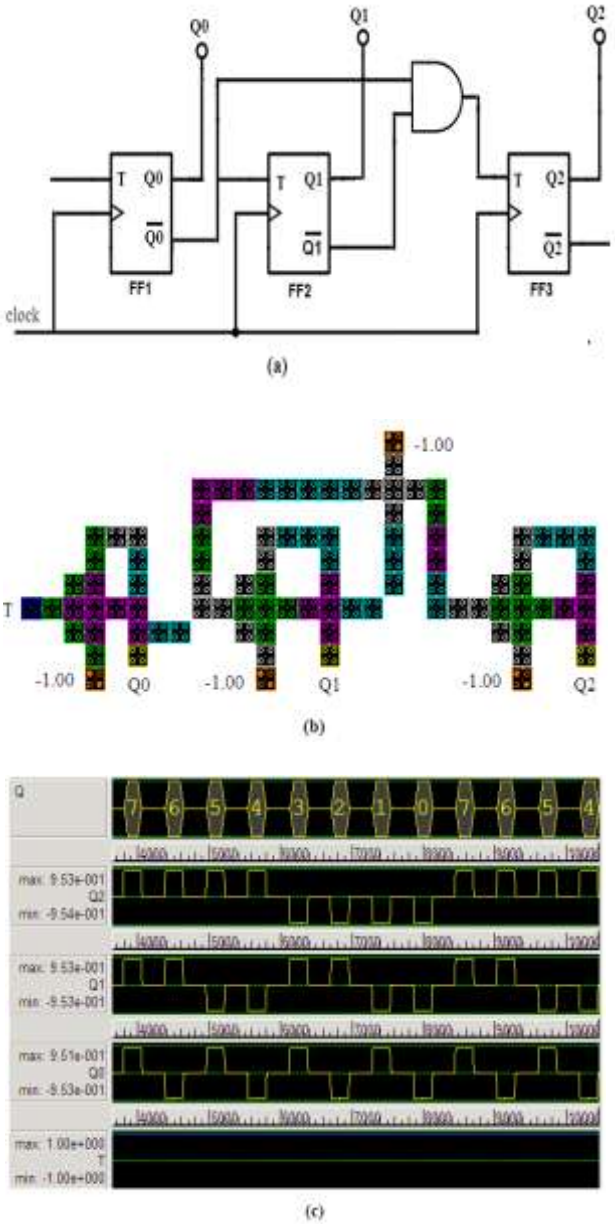
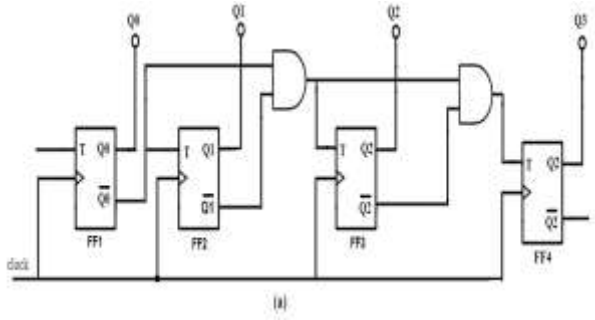


Fig.13.(a) Block diagram of synchronus 3 bit down counter (b) QCA structure of 3 bit down counter using proposed T flip flop (c) its simulation reuslts.

Synchronous 4 bit down counter: The 4 bit down counter operation is converse to the 4 bit up counter.The 4 bit up counter follows the sequence from 0 to 16 with an increment of 1 where as the 3 bit down counter follows the sequence in backward direction right from maximum count to minimum count i.e. 16 to 0.The simulation results of the down counter are presented with hexadecimal representation. The 4 bit down counter 149 QCA cells, 0.19 μm^2 and 31 clock zones as shown in the Fig.14(b).



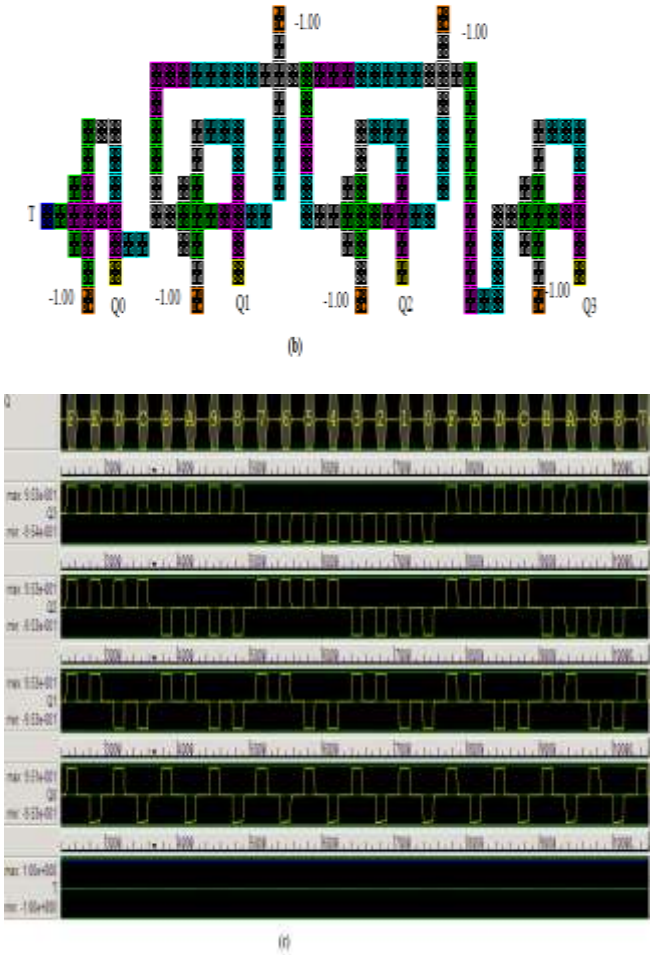


Fig.14.(a) Block diagram of synchronus 4 bit down counter (b) QCA structure of 4 bit down counter using proposed T flip flop (c) simulation reuslts of 4 bit down counter.

V. PERFORMANCE COMPARISION & RESULTS

Table 2 shows the comparison of the proposed QCA T flip flop with other T flip flops in [20,21,24,15,8].

Performance comparision table for proposed and existing T flip flops :

Table 2:

S.No.	Type of T flip flop	cell count	Ratio	% reduction in cell count	Design Area (μm^2)	Ratio	% reduction in area saving	Latency (in clock zones)
1	proposed	19	1	-	0.017	1	-	4
2	[20]	43	2.26	56	0.04	2.35	57	5
3	[21]	47	2.47	59	0.05	2.94	66	5
4	[24]	58	3.05	67	0.056	3.29	70	5
5	[15]	67	3.53	72	0.08	4.7	79	5
6	[8]	108	5.68	82	0.2	11.76	91	5

According to Table 2, our proposed design achieved the best results in comparison with other QCA T flip flop circuits in terms of area occupation, cell count, latency and cost. In

particular, the cell count and design area of the proposed T flip flop are reduced by about 56%, 57%, and 20% in comparison with QCA T flip flop in [20].

Table 3 present the comparison of the synchronus 2 bit upcounter using proposed QCA T flip flop with other 2 bit counters in [20,8,15] which are designed in single layer.

Performance comparision table for existing and proposed 2 bit up counters:

Table 3:

S.No.	Type of qca 2 bit up counter	cell count	Ratio	% reduction in cell count	Design Area (μm^2)	Ratio	% reduction in area saving
1	proposed	43	1	-	0.038	1	-
2	[20]	92	2.14	53	0.11	2.89	65
3	[8]	134	3.12	68	0.18	4.74	79
4	[15]	140	3.25	69	0.17	4.47	78

From the table 3 it can be observed that our proposed design attained the best results in comparison with other 2bit counters circuits in terms of area occupation, cell count, latency and cost. In particular, the cell count and design area of the 2 bit counter using proposed T flip flop are reduced by about 53%, 65%, and 84% in comparison with QCA 2bit counter in [20].

The following Table 4 illustrate that the comparison of the 3 bit up counter using proposed QCA T flip flop with the other 3 bit counter in [15] .

Performance comparision table for existing and proposed 3 bit up counters:

Table 4:

S.No.	Type of qca 3 bit up counter	cell count	Ratio	% reduction in cell count	Design Area (μm^2)	Ratio	% reduction in area saving	Latency (in clock zones)
1	proposed	93	1	-	0.12	1	-	16
2	[15]	244	2.62	62	0.33	2.75	64	17

As it is shown in Table 4, 3 bit up counter using our proposed QCA T flip flop design achieved the best results in contrast with the other 3 bit counter circuits in terms of area occupation, cell count and latency . In particular, the cell count, design area and latency of the 3 bit counter using our proposed T flip flop are reduced by about 62%, 64% and 6% respectively in comparison with QCA T flip flop in [15].

Table 5 shows the comparison of the 4 bit up counter using proposed QCA T flip flop with other 4 bit counter in [8].

Performance comparision table for existing and proposed 4 bit up counters:

Table 5:

S.No.	Type of qca 4 bit up counter	cell count	Ratio	% reduction in cell count	Design Area (μm^2)	Ratio	% reduction in area saving	Latency (in clock zones)
1	proposed	146	1	-	0.18	1	-	32
2	[8]	357	2.44	59	0.57	3.16	68	34

According to Table 5, 4bit up counter design using our proposed QCA T flip flop present the best results in comparison with other QCA T flip flop circuits in terms of area occupation, cell count and latency . In particular, the cell count, area, and latency of the 4 bit counter using our proposed T flip flop are reduced by about 59%,68% and 6% respectively in comparison with QCA T flip flop in [8].

Table 6 shows the comparison of the 4 bit synchronus down counter using proposed QCA T flip flop .

Performance comparision table of 4 bit synchronous down counters using proposed T flip flop:

Table 6:

S.No.	Type of qca down counter	cell count	Ratio	Design Area (μm^2)	Ratio	Latency (in clock zones)
1	2 bit	44	1	0.04	1	4
2	3 bit	95	2.15	0.12	3	19
3	4 bit	149	3.39	0.19	4.75	31

As it is shown from the table 6, the synchronus 2bit, 3 bit and 4 bit down counter designs using proposed QCA T flip flop design require cell count of 44,95 and 149 respectively where as QCA layour area of 0.04 μm^2 ,0.12 μm^2 and 0.19 μm^2 respectively.According to the comparision tables, the synchronus 2 bit, 3 bit and 4 bit down counter need almost same number of cells, area and latency as that of 2 bit, 3bit and 4 bit up counters.

VI. CONCLUSION

The QCA is an best alternative for conventional CMOS technology at Nano-scale level due to its small size, very high switching speed and ultralow power consumption. QCA T flip flop is one ofthe most important sequential circuit in digital circuits such as counters. In this paper, a novel QCA structure was proposed for QCA T flip flop. Using the proposed QCA T flip flop as the main building block, a novel QCA structure was presented for synchronous 2bit, 3bit and 4 bit up counters as well as for down counters.The proposed designs were implemented using QCADesigner version 2.0.3. with the proposed QCA T flip flop structure Our simulation results of counters have attained significant improvement in the performance in term of cell count, design area and speed.

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