

Low Power Design of 0.8V based 8 Bit Content Addressable Memory using MSML implemented in 22nm Technology for Aeronautical Applications

G. Naveen Balaji, M. Karthiga, D. Swetha, M. Suchitra

Abstract— Proposed Paper contains Master slave match line (MSML) architecture which is implemented in traditional Content Addressable Memory (CAM) cell for storing 8 bit of data. Objective of the proposed methodology is to improve searching speed with less power consumption. MSML operation depends on two things one is Master Match Line (MML) and slave match line (SML). Design is performed using SPICE in 22nm technology which is weightless and can be used in Aeronautical Equipment. Various parameters such as temperature, power and delay are calculated for various types of CAM cell. Proposed methodology power consumption is found to be 598mw with delay of 5.98ns for 22nm technology.

Key Words— CAM Architecture, NAND architecture, NOR Architecture, MSML design.

I. INTRODUCTION

Memory assumes a urgent job in style of the numerous processors. In case of RAM, when user gives the address of the data, RAM will return the value of data present in that address. CAM architecture is planned in such the least complex way that client gives the data ,CAM cell looks through its whole memory to detect the information is blessing wherever. Advantage of CAM cell is that it operates in single clock cycle and has more searching speed when compared to RAM.in any case, the dimensions of CAM cell is hyperbolic, that will build the office utilization. Memory is that the vital half by and large the processor style. A memory has significant effect on the execution of chip. basic circuits acclimated style CAM is lock and XOR rationale. affordable power investigation of the CAM cell will be gotten by exploitation MSML style. CAM cell is authorized exploitation numerous procedures. There region unit 2 assortments of matchline models [1-6] i.e NAND kind matchline and NOR kind matchline. NOR kind gives higher inquiry execution contrasted with NAND kind matchline anyway it devours high power NAND kind matchline design

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consumes less power contrasted with Nor kind matchline. matchline control utilization will be diminished by many strategies like matchline division [2], pipelining look strategy [1],[4] and also lessening the voltage swing [3] inside the matchline.

To conquer these ml control utilization new ml configuration alluded to as Master Slave Match Line [MSML] is planned. Fundamental origination behind the MSML style is to blend the ace slave structure and charge sharing method and consequently lessening the capacity scattered inside the ml. This paper is given as pursues: Area II centers around style system of standard CAM cell style and MSML. Area III explains the design level usage of Master slave Match Line style for 22nm innovation. Segment IV describes concerning the Simulation results and furthermore the correlations zone unit all over in Section V.

II. ARCHITECTURE OF MASTER SLAVE MATCH LINE

Dissimilar to standard Content addressable memory that utilizes one match line for pursuit task, this MSML configuration utilizes one MML and various other SML to play out the hunt activity. The charge misfortune will be diminished by making confused SMLs head from MML thus released to zero. Power consumed by ML is reduced because of charge shared by SML mismatch.Fig.1. explains about conventional CAM architecture.

A. CAM Architecture

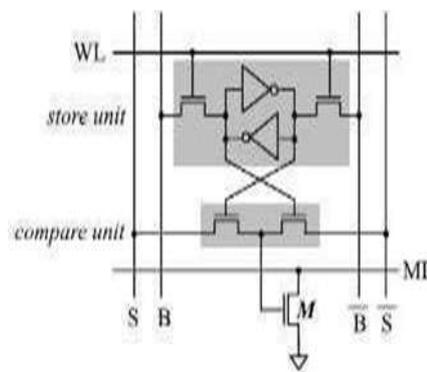


Fig. 1. CAM architecture



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CAM architecture comprises of 2 units, Store unit and correlation unit. store unit comprises of 6T SRAM cell that is particularly utilized for putting away the bit line data inside the lock. Correlation unit is that the one that looks at each the {input information |input file| computer file} and along these lines the hang on information by misuse the XOR activity. Draw down intersection transistor M is associated at the least that makes the ML charge or release to vdd or ground that is appeared in Fig. 1.

B. MSML architecture:

Three activities that is performed in MSML Design. They are given by following.

C. Search Operation

In Normal CAM cell, there are two modes of operation available. During precharge phase, FML & MML values are set to one. In Match Evaluation phase when one or more SML are mismatched, FML values goes low.

D. Precharge phase

When PRE=1, the values of master match line and Final match line are set to one and all the Slave match line gets low value. Because of pull down transistor going to low, charge sharing path gets separated.

E. Evaluation phase

Under this condition, PRE=0 and data are loaded in the search line. There are two parts in cam cell design .SML1 and SML2 .Due to this two parts there is possibility of four outcomes in this phase. Exact match occurs only when both SML's are same.

Case1:(SML's match)

In this condition Both Final match line & Master match line are set to one and the SML1, SML2 are set to low value. (i.e.Zero).Under this condition there is no conduction in charge sharing path.

Case2:(One of the SML match)

Under this phase, Either one of the SML is matched, Suppose if SML1 is matched and SML2 is in mismatch.one of the transistor gets on because of which voltage of SML2 gets increased due to charge is distributed to SML2 by MML. Once charge sharing gets completed both MML and SML2 will have voltage values equal.

Equation (1) gives the final voltage which is derived from charge sharing concept

$$V_b = \frac{CMML}{CMML + CSML2} VMML \cong \frac{2}{3} VMML \quad (1)$$

Where CMML represents capacitance of Master Match Line,CSML2 represents capacitance of Slave match Line and VMML represents final voltage of Master Match line.

Case 3:(SML's Mismatch)

If both SML1 and SML2 are mismatched, Charge sharing path conducts and because of this MML SML value is obtained from MML

Equation (2).represents final voltage

$$V_b = \frac{CMML}{CMML + CSML1 + CSML2} VMML \cong \frac{1}{2} VMML \quad (2)$$

Case 2 consumes less power when compared with Case 3. Master slave Match Line configuration using Conventional Content addressable memory is given in Fig.2.

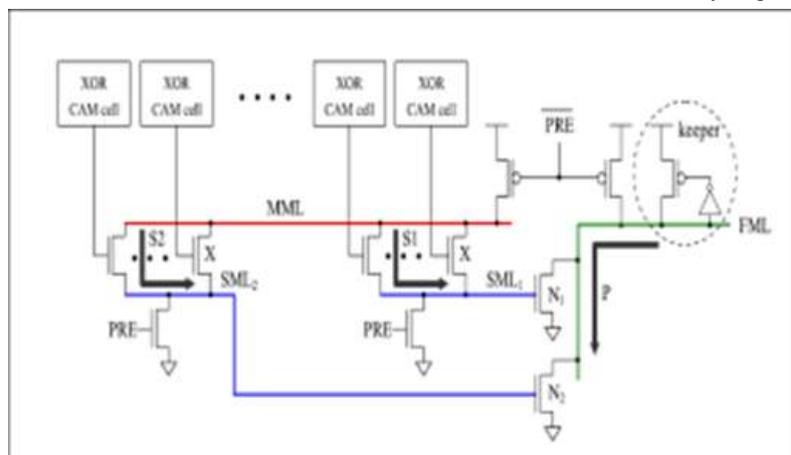


Fig.2.CAM cell using MSML Design

III. CALCULATION OF POWER AND DELAY

CAM performance depends on Power, Speed. Various parameters such as temperature, delay and Power are calculated for various type of CAM cell.

A. Power Estimation

There are two types of power in every circuit. They are static or leakage power and Dynamic power. Static power is due to leakage current. Dynamic power is due to switching between two nodes.

Equation (3) represents dynamic power equations

$$\text{Power} = V_{DD}^2 * f * \sum_{i=1}^j \alpha_j * C_j \quad (3)$$

VDD is the power supply and αj is probability of toggle. CJ is the capacitance between the nodes and f is the input frequency.

B. Delay Estimation

Delay calculation is explained using elmore delay model. RC circuit is given in Fig.3.

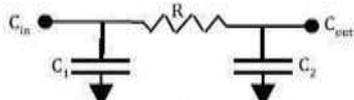


Fig. 3. RC Circuit

Propagation Delay is calculated using Equation 4.

$$t_{pd} = 0.69R(C_1 + C_2) \quad (4)$$

Where R is the Resistance C1, C2 are parasitic capacitances

IV. SPICE LEVEL IMPLEMENTATION OF VARIOUS CAM CELL DESIGN USING 22NM

CAM Cell configuration is executed in SPICE level as appeared in Fig. 4. Configuration is done in 22nm innovation to examine the execution in innovation scaling situations.

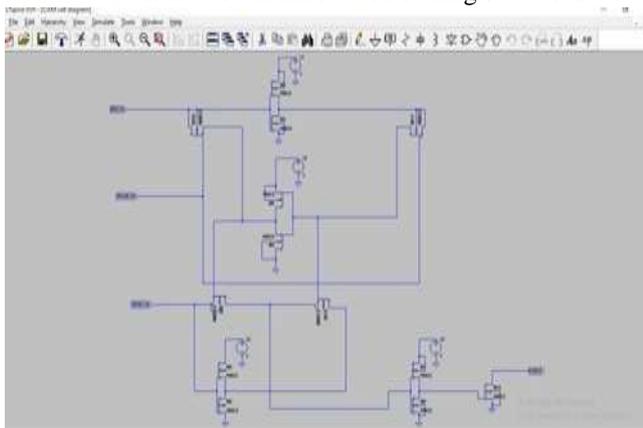


Fig. 4. Circuit Diagram of CAM cell

Fig.4 shows circuit diagram of Traditional CAM cell using SPICE .Fig.5. shows circuit diagram of NOR based CAM cell based design. Fig.6. shows Circuit diagram of NAND based CAM cell design and Fig.7. shows Circuit diagram of proposed MSML design

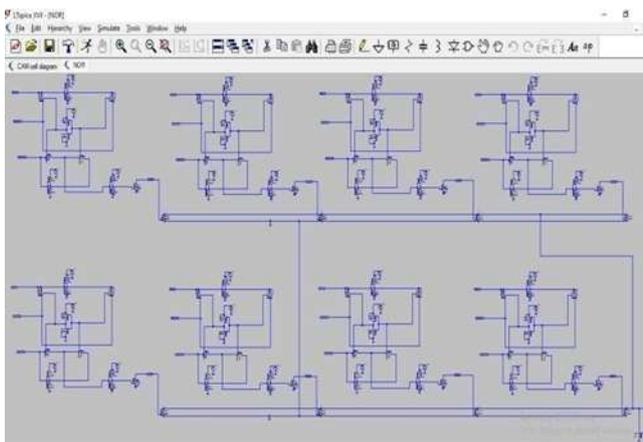


Fig. 5. Circuit Diagram of NOR Architecture

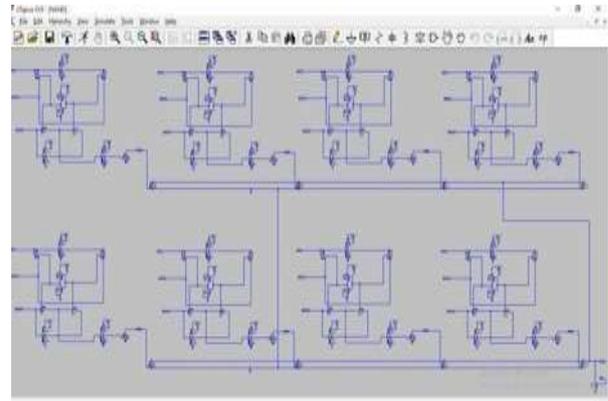


Fig. 6. Circuit Diagram of NAND Architecture

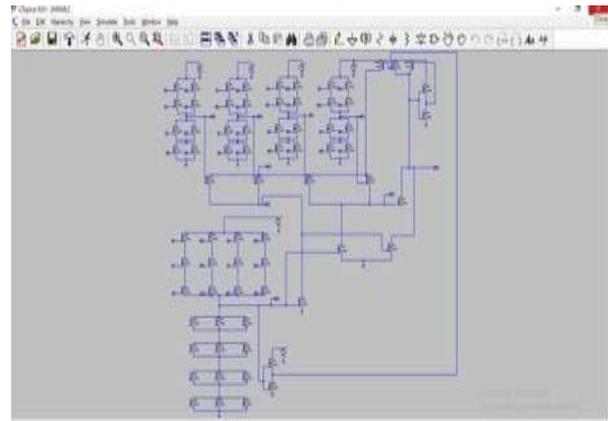


Fig. 7. Circuit Diagram of MSML Architecture

V. SIMULATION RESULTS

Simulations for different CAM Architectures are completed utilizing SPICE at 22nm innovation. Yield waveforms of MSML Architecture in Fig.8, nand architecture yield simulation results in Fig.13. Nor type architecture yield simulation results in Fig.16.

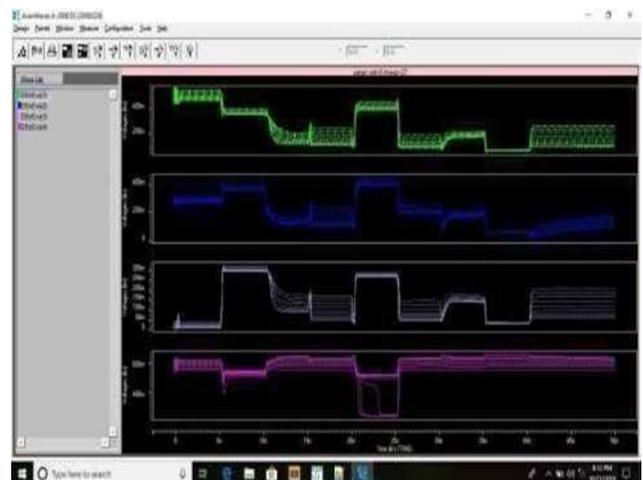


Fig. 8. Waveform for MSML architecture at different temperature

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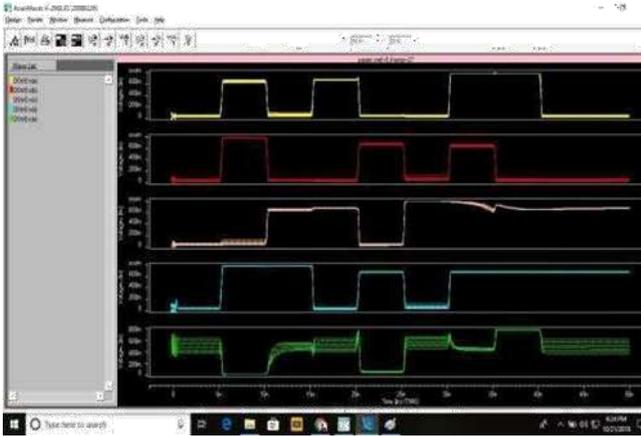


Fig. 9. Expanded simulation results for MSML design

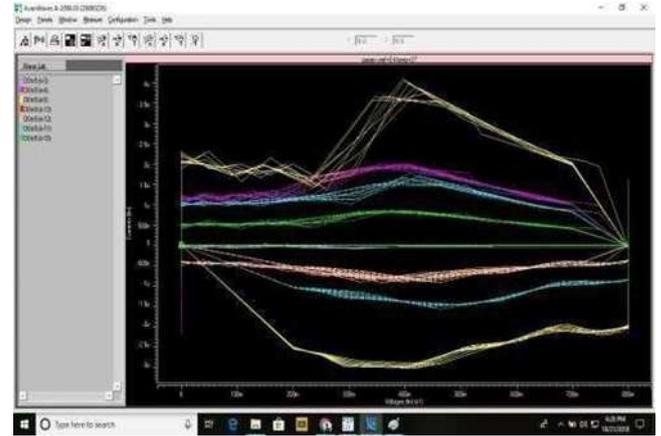


Fig. 12. Expanded simulation results of MSML architecture

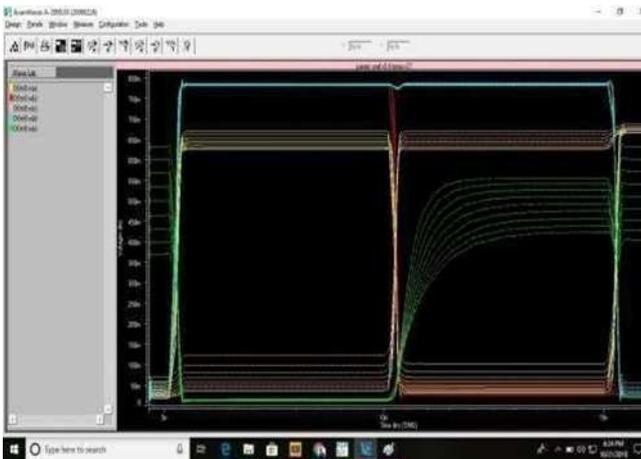


Fig.10.Characteristic Waveform of master slave match line

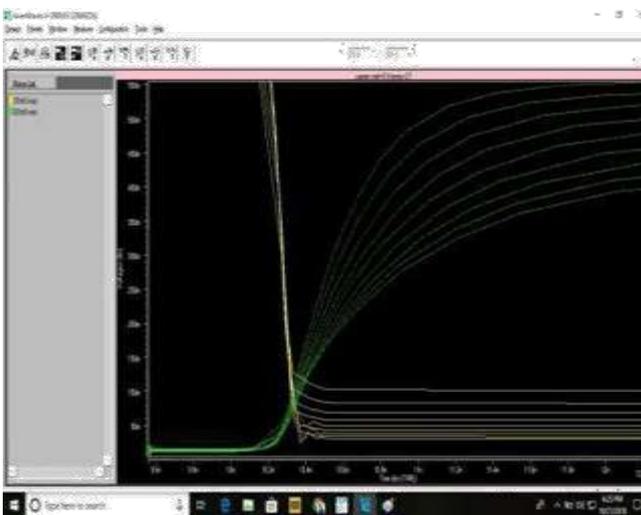


Fig. 11. Expanded waveform of Master Slave Match Line

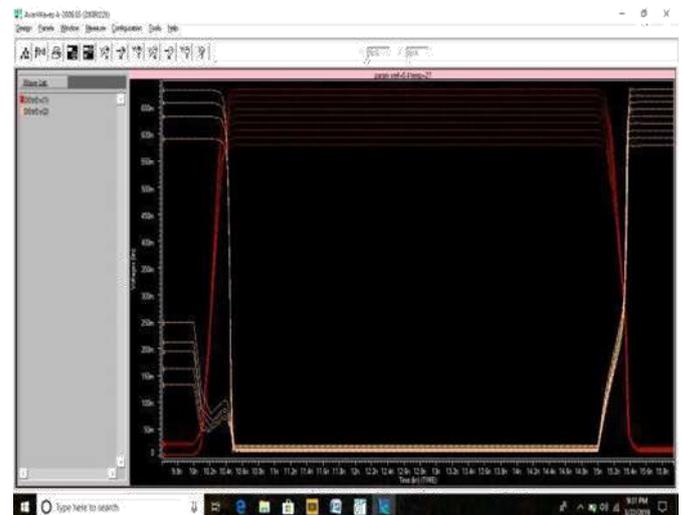


Fig.13.Characteristic Waveform of NAND Type CAM cell

The figure 10 portrays the simulation yield of MSML type CAM plan. Temperature is varied from 27°C to 97°C for MSML design and power is calculated for every 10°C change in temperature. From the Waveform it is observed that from 27 to 37 degree the power consumption gets reduced form 598mw to 592mw with delay of 5.28ns. From 37 to 47 degree the power consumption is reduced form 592mw to 582mw with delay of 5.23ns. From 47 to 57 degree the power consumption is reduced form 582mw to 572mw with delay of 5.25ns. From 57 to 67 degree the power consumption is reduced form 572mw to 568mw with delay of 5.31ns. From 67 to 77 degree the power consumption is reduced form 568mw to 563mw with delay of 5.33ns. From 77 to 87 degree the power consumption is reduced form 563mw to 560mw with delay of 5.35ns. From 87 to 97 degree the power consumption is reduced form 560mw to 534mw with delay of 5.40ns.

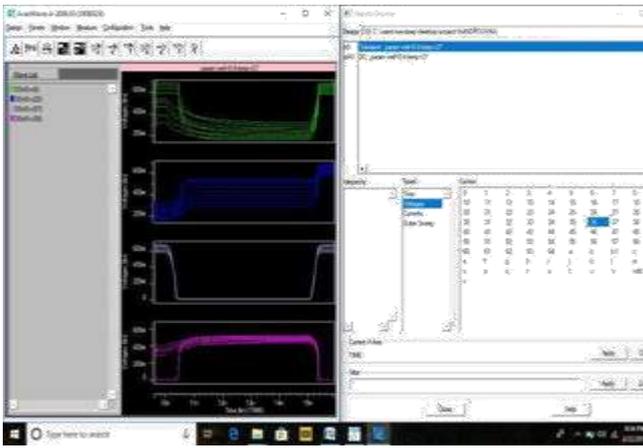


Fig. 14. Output Waveform of NAND design for different temperature

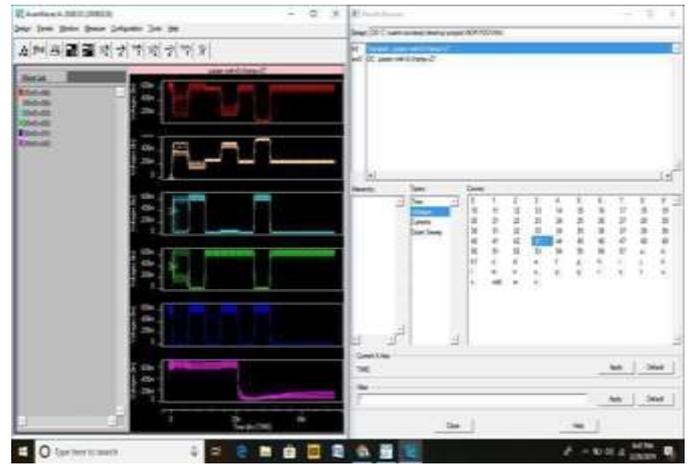


Fig. 16. Output Waveform of NOR design for different temperature

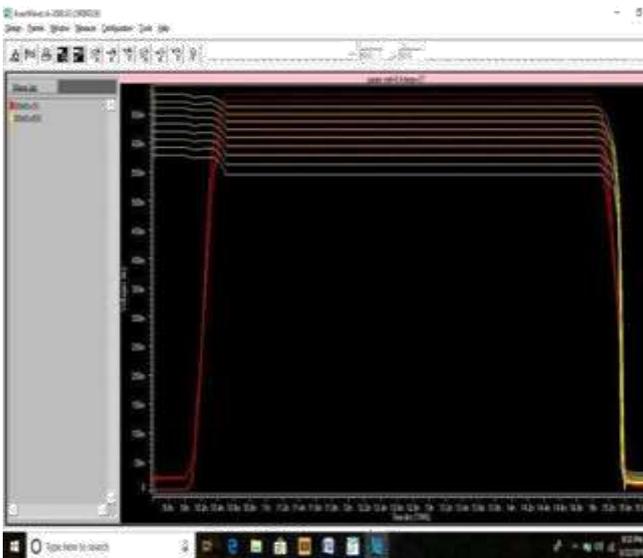


Fig. 15. Expanded Waveform of NAND Architecture

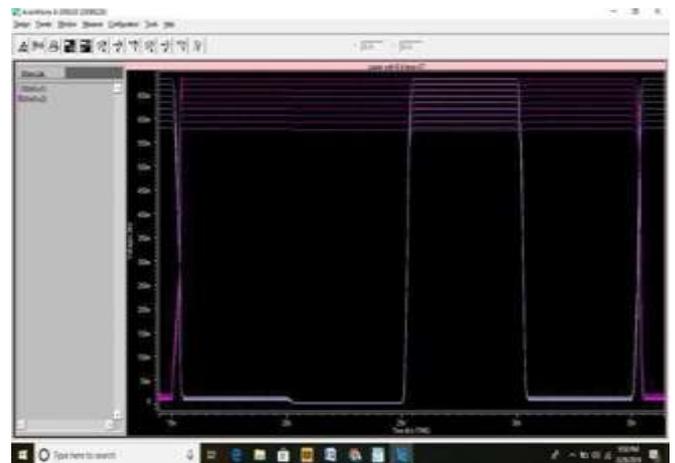


Fig. 17. Characteristic Waveform of NOR Architecture

The figure 13 portrays the simulation yield of NAND type CAM plan. Temperature is varied from 27°C to 97°C for NAND design and power is calculated for every 10°C change in temperature. From the Waveform it is observed that from 27 to 37 degree the power consumption gets reduced from 667mw to 654mw with delay of 5.28ns. From 37 to 47 degree the power consumption is reduced form 654mw to 644mw with delay of 5.23ns. From 47 to 57 degree the power consumption is reduced form 644mw to 632mw with delay of 5.25ns. From 57 to 67 degree the power consumption is reduced form 632mw to 618mw with delay of 5.31ns. From 67 to 77 degree the power consumption is reduced form 618mw to 607mw with delay of 5.33ns. From 77 to 87 degree the power consumption is reduced form 607mw to 594mw with delay of 5.35ns. From 87 to 97 degree the power consumption is reduced form 594mw to 584mw with delay of 5.40ns.

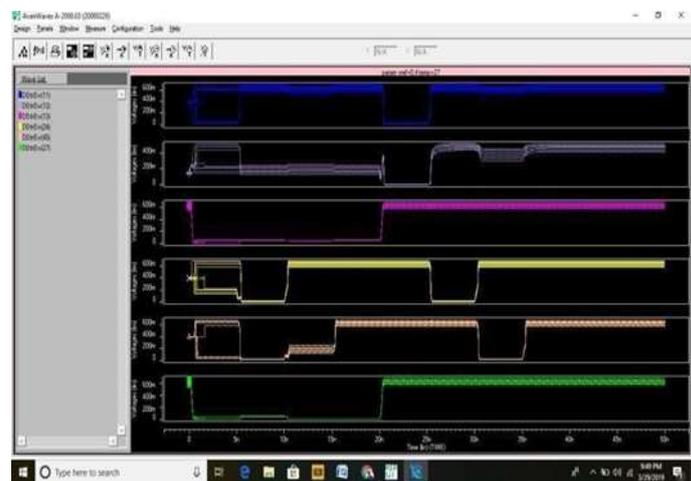


Fig. 18. Expanded output waveform of NOR Architecture

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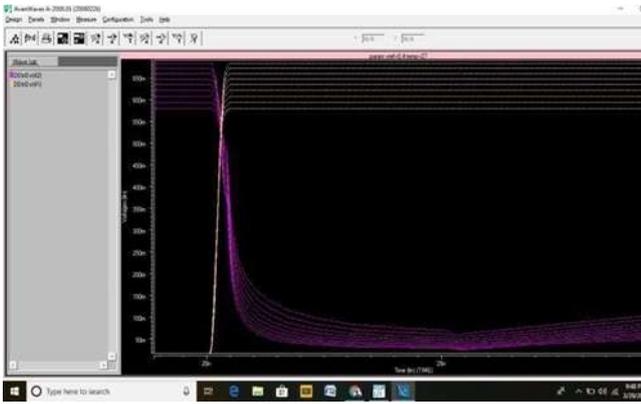


Fig. 19. Expanded Waveform of NOR Architecture

The figure 16 portrays the simulation yield of NOR type CAM plan. Temperature is varied from 27°C to 97°C for NOR design and power is calculated for every 10°C change in temperature. From the Waveform it is observed that from 27 to 37 degree the power consumption gets reduced form 618mw to 613mw with delay of 5.28ns. From 37 to 47 degree the power consumption is reduced form 613mw to 604mw with delay of 5.23ns. From 47 to 57 degree the power consumption is reduced form 604mw to 590mw with delay of 5.25ns. From 57 to 67 degree the power consumption is reduced form 590mw to 580mw with delay of 5.31ns. From 67 to 77 degree the power consumption is reduced form 580mw to 576mw with delay of 5.33ns. From 77 to 87 degree the power consumption is reduced form 576mw to 564mw with delay of 5.35ns. From 87 to 97 degree the power consumption is reduced form 564mw to 560mw with delay of 5.40ns.

**TABLE I
POWER AND DELAY ESTIMATION FOR NAND
CAM CELL**

CAM	Temp (°C)	Time (ns)	Power (mw)
NAND	27°C	5.28	667
	37°C	5.23	654
	47°C	5.25	644
	57°C	5.31	632
	67°C	5.33	618
	77°C	5.35	607
	87°C	5.40	594
	97°C	5.45	584

Table I shows control utilization and delay in 22nm for 1V supply for different temperature From 27°C to 37°C, Power is diminished from 667 to 654 at 5.28ns. From the table it is seen that as the temperature builds control esteem gets diminished at various timeframe.

**TABLE II
POWER AND DELAY ESTIMATION OF NOR CAM
CELL**

CAM	Temp (°C)	Time (ns)	Power (mw)
NOR	27°C	5.28	618
	37°C	5.23	613
	47°C	5.25	604
	57°C	5.31	590
	67°C	5.33	580
	77°C	5.35	576
	87°C	5.40	564
	97°C	5.45	560

Table II shows control utilization and delay in 22nm for 1V supply for different temperature From 27°C to 37°C, Power is decreased from 618 to 613 at 5.28ns. From the table it is seen that as the temperature expands control esteem gets diminished at various timespan.

**TABLE III
POWER AND DELAY ESTIMATION FOR MSML**

CAM	Temp (°C)	Time (ns)	Power (mw)
MSML	27°C	5.28	598
	37°C	5.23	592
	47°C	5.25	582
	57°C	5.31	572
	67°C	5.33	568
	77°C	5.35	563
	87°C	5.40	560
	97°C	5.45	534

Table III shows control utilization and delay in 22nm for 1V supply for different temperature From 27°C to 37°C, Power is diminished from 598 to 592 at 5.28ns. From the table it is seen that as the temperature expands control esteem gets decreased at various timespan.

VI. CONCLUSION

MSML configuration conveys most productive execution among other CAM cell plans is obvious from power examination table. MSML configuration devours 15% less power than NOR Architecture in 22nm and NAND architectre expends 6% more power than MSML plan in 22nm under different temperatures. Along these lines MSML rationale devours less power than all rationale plans and the deferral is likewise determined for different CAM cells. This work can be connected to manufacture low power fast memory which can improve the speed.



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