TCAD Simulation of Nano-Crystal Floating Gate EEPROM

Surya Deo Chaudhary, Ashish Pathak

Abstract— The present invention relates to a Nano crystal floating gate memory which is reflected as a future nonvolatile memory. The reason behind this reflection is its invulnerability in tunnel oxide to weak-point leakage and therefore its higher scalability of tunnel oxide thickness and utilization of power. The Foremost feature attribute in NCM is that it functions on a low value of voltage.

Index Terms— TCAD, MOSFET, Tunnel Oxide Layer, EEPROM.

I. INTRODUCTION

Due to the high scalability and performance flash memory type devices that uses nano crystals as floating gate got [1]. In this type of flash memory, the charges are reserved in nano crystals rather than a full poly silicon floating gate. In usual floating gate, when there is at least 1 fault across tunnel oxide terminal, floating gate charges gate drips back to the drain or source channel (or) through the defect chain. Thick tunnel oxide layer is compulsory to avoid the loss of charge. The problem related to leakage may be removed with the help of memory structure of semiconductor nano crystals [2]. A single FET device is integrated in the memory wherein small amount of electrons are reserved in the form of a layered isolated type nano crystal. For studying NCM structure technology CAD tools have been used that provides good features like, data storage of non-volatile flash memory devices, programming, erasing data examined via TCAD simulation by the employment of different models wherein a *'Hot-carrier injection model'* describes the writing process and *'Fowler Nordheim tunneling model'* that defines the removal of charge or process of erasing by the nano-dot in *'nano-crystal-flash-memory'* type devices.

II. DEVICE STRUCTURE

The *'multi-nano-crystal-memory-cell'* comprises of a *'FET'* device wherein few number of electrons are reserved in a layerd form of isolated type nano crystals. From figure 1 [3] in nano crystal CMOS compatible memories, a segregated and drifting type semiconductor having size in nano-meters has been joined with the MOSFET channel [3].

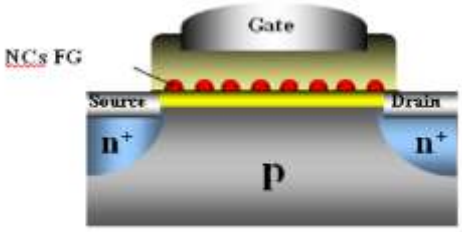

Fig.1 Device structure of nanocrystal memory [3]

Fig.2 Geometry of Nanocrystal flash memory

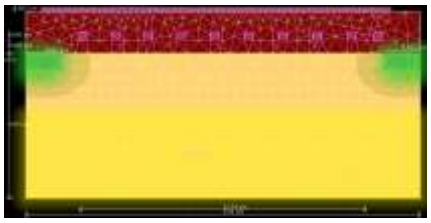

Fig. 3 Meshing File of NCM cell

The gate terminal comprises of an eight nano meter tunnel oxide layer, size of the nano crystal are five nano meters, and a thirteen nm blocking oxide layer between the poly silicon gate material and the channel having a work function i.e. 4.7 electron volts. Ten nano crystal with the size of 5 have been taken. Figure 2 represents the interlocking file of nano crystal flash memory, the file of simulation and material is shown in Figure 4 and Figure 5.

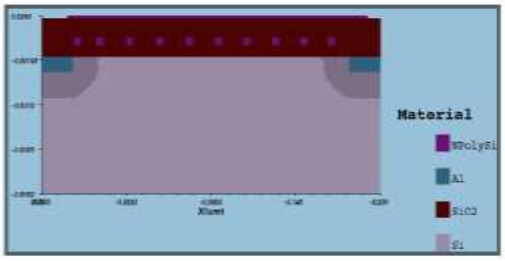

Fig. 4 Materials used in memory device

Revised Version Manuscript Received on 10 September, 2019.

Dr. Surya Deo Chaudhary, Department of Electronics & Communication Engineering, Noida Institute of Engineering and Technology, UttarPradesh, India. (Email: researchnietip@gmail.com)

Ashish Pathak, Department of Physics, Noida Institute of Engineering and Technology, UttarPradesh, India. (Email: researchnietip@gmail.com).

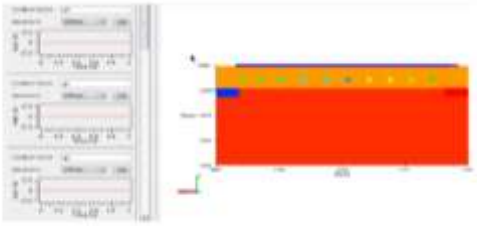

Fig.5 Simulation File of NanoCrystal non-volatile memory cell

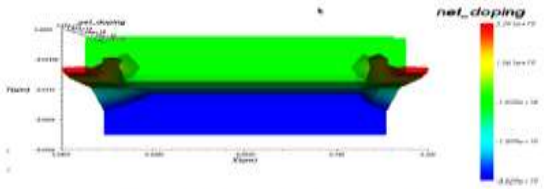

Fig. 6 Doping Profile of NCM cell

At the time of erasing *"Hot Carrier Injection"* and *"Fowler Nordheim"* a process called as tunnelling has been used. For processing the "write" function, channel inversion-layer is kept at a +ve voltage, and applied to electrons into the nano crystals. For the erasing process, a negative voltage is applied to cause the electrons to tunnel back into the channel and accumulation tunnel into the nano crystal from the channel. The thickness of the blocking oxide is enough to block the electron and how tunnelling between the control gate and the nano crystal [2]. Hence tunneling across the control oxide is neglected [2].

III. RESULTS AND DISCUSSION

A. Channel hot electron programming

Once the device gets on by providing high drain voltage then the number of electrons in this channel would move from the source side to the drain region.

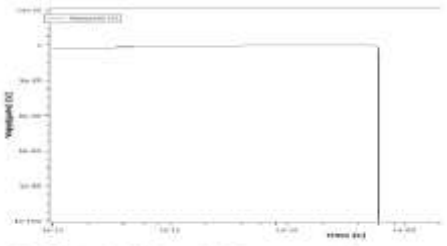

Fig. 7 potential during writing in a nanocrystal memory

The electrical field increases at the pinch-off point of the device. Due to the presence of high value of electric field, the electrons gets speeded i.e. hot electron. For creating influence of ionization, number of carriers get adequate energy that would help in breaking the pairs of electron and hole and generates the subordinate (secondary) electron and holes. In the nano crystal cell, channel hot electron programming can be effortlessly achieved. Initially the value of hot electron current is great during programming, and starts dropping as the –ve charge inserted onto the dot makes it substantial and drops the dot potentials, as represented in Figure 7. This would result in an increased threshold voltage decreases hot carrier injection. The different characteristics like write and erase are represented in Figure 8.

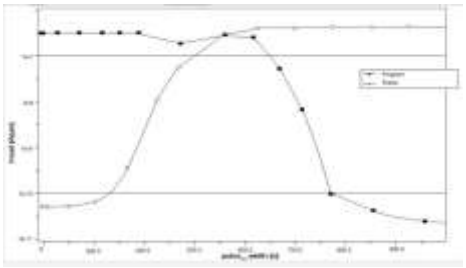

Fig. 8 Write and Erase waveform for NCM

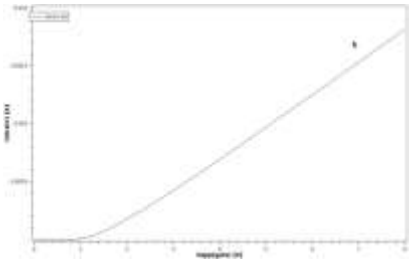

Fig. 9 Before Programming

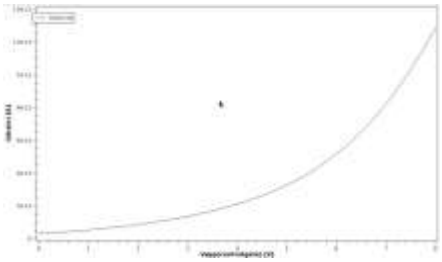

Fig. 10 After Programming

In starting the value of tunneling current is at a high level while erasing but it drops when the nano gate is less negative, therefore while dropping the field the threshold voltage value reduces in the tunneling oxide as represented shown Figure 10.

IV. CONCLUSION

The *"Nano Crystal Floating gate EEPROM"* has been intended & simulated with the help of a software called Visual TCAD, wherein writing and deleting operations in the memory cell has been considered. The result from the output of nano-crystal dots displays the low voltage action and decreases tunneling oxide's size that provides improved performance. [4]

REFERENCES

1. P. L. Vijayvergiya and R. K. Panigrahi, "Single-layer single-patch dual band antenna for satellite applications," IET Microwaves, Antennas Propag., 2016.
2. B. Li and Z. Shen, "Dual-band bandpass frequency-selective structures with arbitrary band ratios," IEEE Trans. Antennas Propag., 2014.
3. D. Cure, "Reconfigurable Low Profile Antennas Using Tunable High Impedance Surfaces," ProQuest Diss. Theses, 2013.
4. S. M. Sze, R. H. FOWLER, and L. NORDHEIM, "Electron Emission in Intense Electric Fields," in Semiconductor Devices: Pioneering Papers, 2014.
5. C. M. Compagnoni, D. Ielmini, A. S. Spinelli, A. L. Lacaita, and C. Gerardi, "Study of nanocrystal memory reliability by CAST structures," in Solid-State Electronics, 2004.