Energy Efficient Digital Circuit Based on Self Cascoding Positive Feedback Adiabatic Logic for Low Power VLSI Design

Vivek Jain, Sanjiv Tokekar, Vaibhav Neema

Abstract*:-Emphasis in VLSI design has shifted from high speed to low power due to the proliferation of portable electronic systems. The continuing decrease in feature size and corresponding increase in chip density and operating frequency have made power consumption as a prime concern in VLSI design. For ultra low power applications, the idea of self cascode positive feedback adiabatic logic (SC-PFAL) has reported as a promising candidate to reduce power dissipation at low operating frequency. To enhance the energy efficiency of the logic circuits, self cascoding of transistor is applied to charge recovery logic working in sub-threshold region. Based on this proposed technique, we design a basic MOS digital library cell. Simulation results are found using 70nm technology model file available from predictive technologies. At low clock frequency, the proposed logic i.e. SC-PFAL has significant improvement in terms of energy consumption than original PFAL.

Keywords: ***Charge recovery logic, PFAL, Self cascode, Ultra low power***

I. INTRODUCTION

Due to increase in complexity of the chips day by day the challenge to reduce the power dissipation results in limiting the functionality of the computing systems.With the advent in the era of communication system where multiple devices are continuously exchanging data with each other, technologies like IOT demands for ultra low power consumption. Portable and handheld devices needs high speed computation with low power consumption as most of the devices are battery operated. There must be a trade off between speed and power for optimization of a circuit as higher speed leads to higher power dissipation and vice versa.While focussing on the performance and area for VLSI chip design, power dissipation is a prime factor which must be given importance. Many techniques are used for optimization of power among which adiabatic logic is a promising technique to reduce dynamic power loss in digital systems. Reduction in energy loss is achieved by returning back the major portion of charge supplied by the power supply by restricted the charge to flow to the ground terminal. [1].

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The charge flow in conventional CMOS logic is from supply to ground terminal through parasitic capacitances, while in case of adiabatic logic, a major portion of the energy supplied by battery is returned back to the supply as shown in Fig. 1[2]. We can also reduce the power consumption by keeping the system to work in sub-threshold region by reducing the supply voltage below threshold level (V_{TH}) of a transistor resulting in reduction of power without sacrificing noise immunity and driving ability [3].These two techniques can work together toaccomplishultra low power VLSI systems. These systems work at power clock frequencies range from a few Hundreds of hertz to a few Megahertz. The power consumption can be in range of few pico-watts. These systems are suitable for the domain where low power consumption is more important than the processing speed [4], such as biomedical application which typically works at clock frequency below one MHz [5].

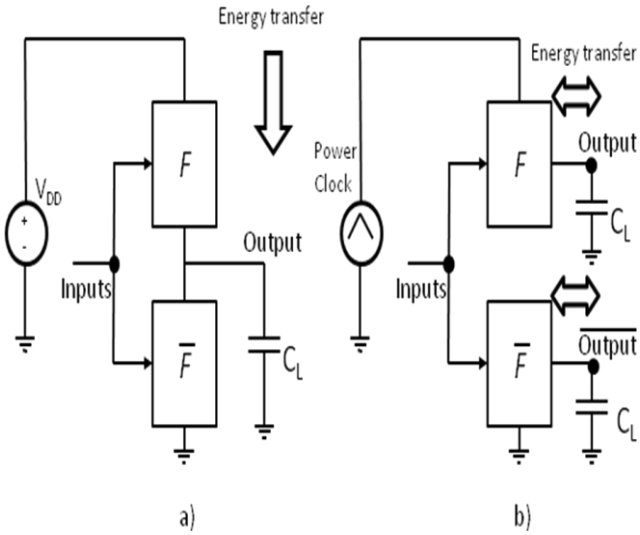

Fig. 1 The energy flow in

a) conventional CMOS logic and b) Adiabatic logic

The adiabatic logic family has different members like 2N2N2P [6], ECRL [7] and PFAL [8].These adiabatic circuits have latch based structure. The positive feedback in the latch ensures that system will attain either of the two stable states and avoid logic level degradation at the output nodes [9]. The performance of the latch depends on its loop gain which is of the order of $(g_m r_o)^2$. The reduction in output

impedance due to channel length modulation effect is a big issue for highly scaled devices [10]. This effect directly reduces the loop gain of the latch. The loop gain can be increased using cascoding of MOSFETs. The cascoding of transistors also reduces the leakage current and further improves the efficiency [11]. Regular cascode may not be suitable in highly scaled devices, as the supply voltage available may be of order of twice V_{TH}. Self cascode technique can be used to obtain cascoding of transistors without reducing the swing [12].

II. METHODOLOGY

The idea of self cascoding of transistor to adiabatic logic circuit used in sub-threshold region can reduce power consumption significantly [3].

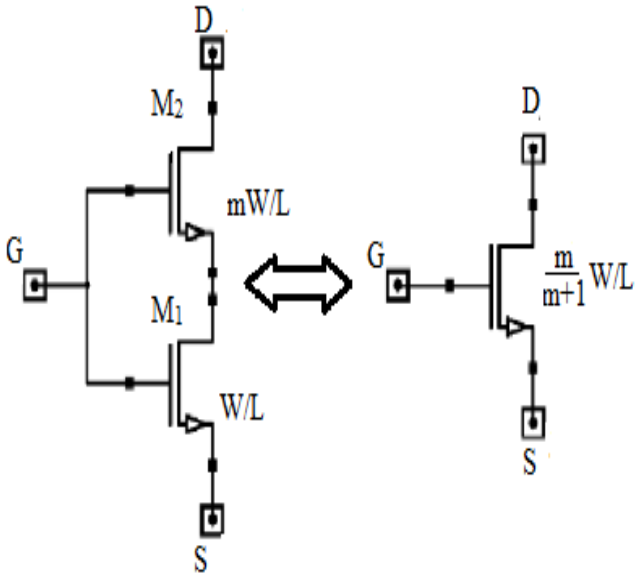

Fig. 2 Self cascode transistor

Fig. 2 shows that MOSFETs are in series, so currents in both transistors will be same. The two MOSFETs have same length but different widths thus the larger of the transistor will be in linear region and will have small drop across it, eventually in deep triode region, the transistor M_2acts like a small source degeneration resistor for M_1.This makes the self-cascode arrangementsuitable for low voltage applications. The effective β of new transistor is not changed much as new β is given by equation 1.

$$\beta_{eff} = \frac{\beta_1\beta_2}{\beta_1+\beta_2} \quad (1)$$

$$\text{if } \beta_2 = m.\beta_1 \quad (2)$$

$$\beta_{eff} = \frac{m}{m+1}\beta_1 \quad (3)$$

And if *m* is large, β is almost equal to $\beta_1$where as the small signal output resistance of the new cascode transistor is given by equation 4. The equation suggests the resistance is increased by a factor of intrinsic gain of transistor M_2; this can be seen in I_DV_D curves as shown in Fig. 3. The figure shows I_DV_D curve for both self cascode transistor and a normal NMOS transistor. It can be seen that the slope of self cascode structure is smaller that indicates increase in output resistance.

$$r_0 = (gm_2r_2).r_1 - r_1 - r_2 \quad (4)$$

$$r_0 \approx (gm_2r_2).r_1 \quad (5)$$

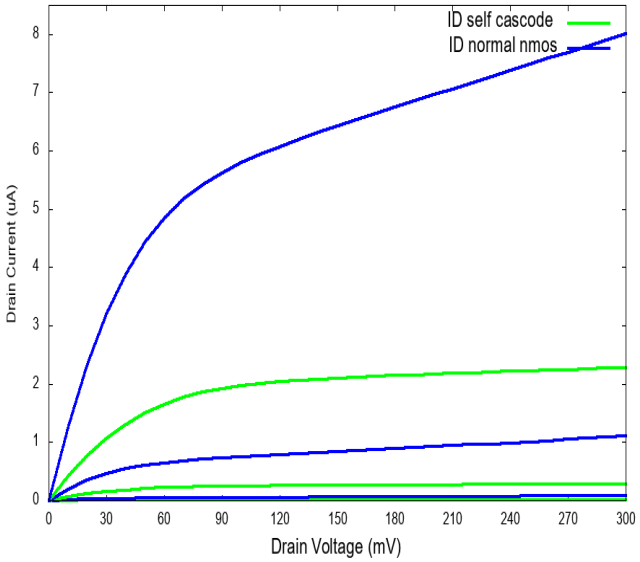

Fig. 3 I_DV_D graph to demonstrate increase in output impedance of a self cascode transistor in subthreshold region. The curves are plotted for gate potential of 0.1, 0.2 and 0.3 volts.

The overall gain of a self cascode inverter is given by equation 6 .

$$A = gm_1.r_1 + gm_2.r_2 + gm_1.gm_2.r_2.r_1 \quad (6)$$

The small signal output resistance is multiplied by intrinsic gain of the wider transistor. Thus, the self cascode transistor is able to provide higher output resistance without sacrificing much performance. The increase in r_0 of transistor will improve the performance of the latch as mentioned earlier. The loop gain of a latch is product of gain of individual inverter of the latch as shown in Fig. 4.

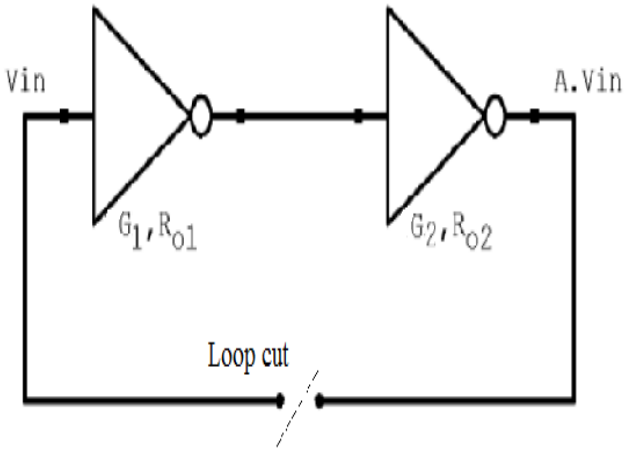

Fig. 4 loop gain for a latch

The loop gain is given by equation 7

$$A = (G_1 R_{01}).(G_2 R_{02}) \quad (7)$$

Improvement in R_0 will improve the loop gain in square proportion.

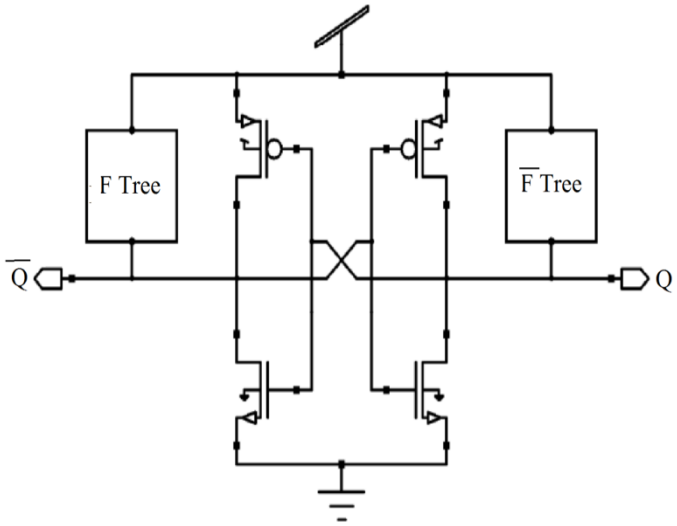

Fig. 5 PFAL circuit

Some standard adiabatic logic topologies like 2N2N2P, ECRL and PFAL [16] were simulated by replacing MOS transistors with self-cascodetransistors in the latch. ThePFAL topology was observed to provide better results. The PFAL adiabatic logic architecture contains a latch and two pull up network that realize a Boolean logic equation to be implemented as shown in Fig. 5.

III. PROPOSED CIRCUIT

A basic logic circuit as inverter using PFAL logicwith fanout of four is designed and simulated using 70nm model file provided by Predictive Technologies Model (PTM) [14]. The circuit is as shown in Fig. 6.

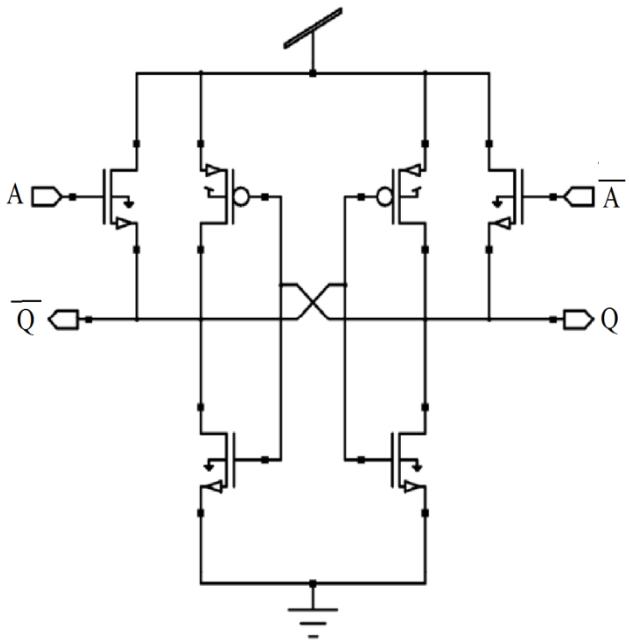

Fig. 6 PFAL inverter

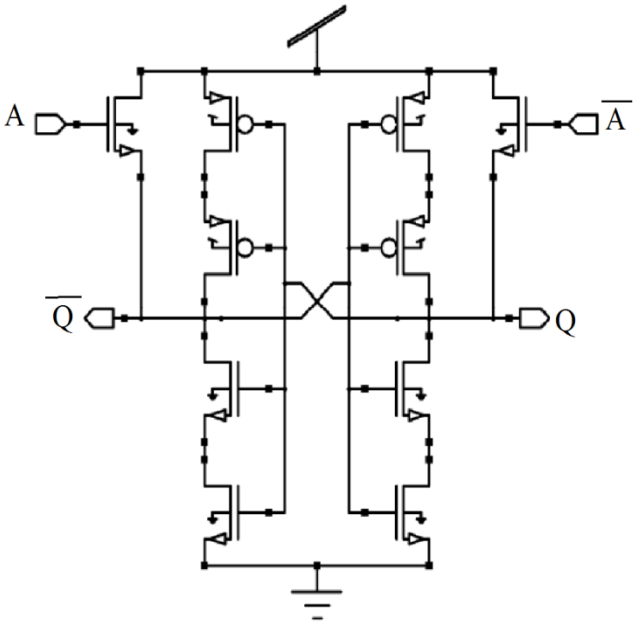

Fig. 7 SC-PFAL inverter

The latch transistors of the PFAL inverter circuit are replaced with self cascode transistors as shown in Fig. 7 to obtain SC-PFAL inverter as proposed circuit. To calculate the power consumption and propagation delay of the circuit, a test bench is developed with a triangular wave voltage source assupply voltage and a load of four unitload(inverter) is placed at output of design under test.

IV. RESULTS AND DISCUSSION

The circuit is designed using 70nm PTM model file with threshold voltages V_{thP} = -326mV and V_{thN} = 310mV and simulated using T-Spice simulator. A 300mV triangular supply is used to power up the logic gate. To evaluate the performance of proposed architecture, basic logic gate is designed and simulated. The results are tabulated in table 1 and table 2. Simulated waveform of proposed inverter is shown in Fig. 8.

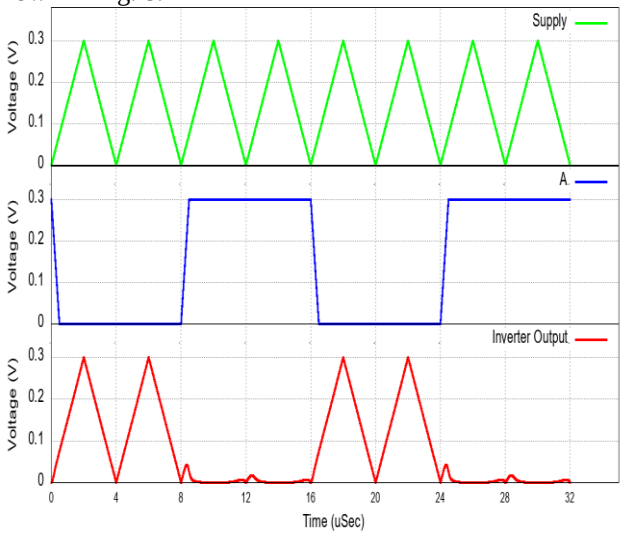

Fig. 8 Input output waveform of SC-PFAL inverter

It can be seen that the performance enhancement is better for SC-PFAL inverter than PFAL. The best enhancement in power reduction is observed to be obtained for inverter. Statistics shows that inverters are most used logic gates in a typical logic circuit.

Table 1. Basic inverter performance of PFAL for different clock frequencies

Frequency (MHz)	PFAL		
	Average Power Dissipation (W)	Propagation Delay (Sec)	PDP(J) (Dynamic)
0.5	2.77E-10	4.63E-07	1.28E-16
1	2.80E-10	2.32E-07	6.49E-17
1.5	2.83E-10	1.55E-07	4.40E-17
2	2.88E-10	1.17E-07	3.37E-17
2.5	2.93E-10	9.39E-08	2.75E-17
3	2.99E-10	7.85E-08	2.35E-17
3.5	3.06E-10	6.75E-08	2.06E-17
4	3.13E-10	5.95E-08	1.86E-17

Table 2. Basic inverter performance of SC-PFAL for different clock frequencies

Frequency (MHz)	SC-PFAL		
	Average Power Dissipation (W)	Propagation Delay (Sec)	PDP(J)
0.5	1.92E-10	4.64E-07	8.90E-17
1	2.01E-10	2.33E-07	4.70E-17
1.5	2.13E-10	1.57E-07	3.33E-17
2	2.26E-10	1.19E-07	2.68E-17
2.5	2.40E-10	9.57E-08	2.30E-17
3	2.56E-10	8.05E-08	2.06E-17
3.5	2.73E-10	6.95E-08	1.90E-17
4	2.91E-10	6.14E-08	1.79E-17

The power, delay and energy dissipation of SC-PFAL inverter is compared with PFAL inverter in plots a), b) and c) of Fig. 9 respectively. It is revealed that the SC-PFAL logic gives better results at lower frequencies. The SC-PFAL logic has shown better energy efficiency than PFAL adiabatic logic up to 4MHz. The plot of power dissipation versusoperating frequency shows thatpower efficiency performance of proposed circuit is better at lower operating frequency.

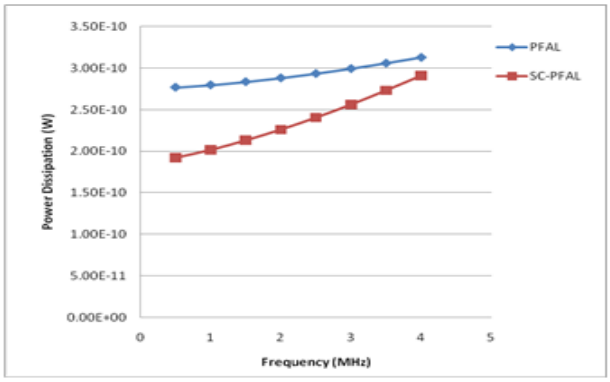

Fig. 9 (a) Comparison of power dissipation for inverter

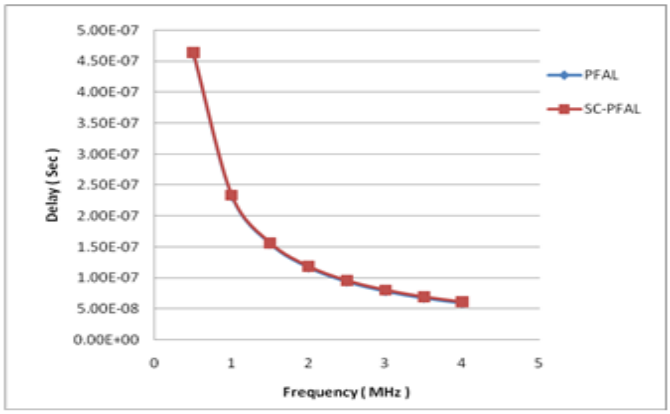

Fig. 9 (b) Comparison of propagation delay for inverter

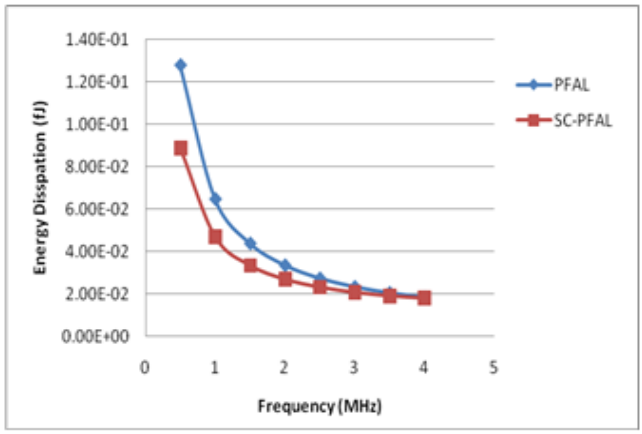

Fig. 9 (c) Comparison of energy dissipation for inverter

V. CONCLUSION

Proposed SC-PFAL circuit has better energy efficiency than PFAL circuit at lower operating frequencies in sub-threshold region. To reduce the power consumption, the concept of self cascoding is applied to the latch present in PFAL circuit. The effect of self cascoding was explored for PFAL and other adiabatic logic techniques also. It is revealed that PFALlogic is better suited for applying self cascodetransistors. The simulation results show that power consumption of proposed SC-PFAL circuit is about 32% less than its original PFAL circuit at 0.5 MHz operating

frequency. In summary, the SC-PFAL logic provides useful building blocks in design of energy recovery systems operating at very low power regime.

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