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Power Quality Enhancement in Multi-Feeder Distribution System using Mf-Upqc Device

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Abstract*: The significant usage of power semi-conductor devices in modern single or multi-feeder distribution system is increasing a lot in present situation. The non-linear characterization of power distribution is highly responsible for degradation of power-quality standards. The usage of large-sized non-linear loads provokes the harmonic pollution, voltage interruptions, voltage sag/swell issues are the key problems faced by distribution systems. Over the various compensation methodologies, the highly validated universal device is Unified-Power Quality Compensator. The multi-feeder universal devices play a prominent role and provide the attractive performance with improved characteristics in multi-feeder distribution system. In this work, Multi-Feeder UPQC device is used to compensate all voltage and current related PQ issues in multi-feeder distribution systems and also furnishes load-sharing between adjacent feeders, reduce the power-shortages, maximizes the stable performance. The performance evaluation of proposed MF-UPQC is verified under various case studies with the help of Computer-Simulation tool, results are validated with improved PQ features.

***Index Terms*:Multi-Feeder Distribution System, Multi-Feeder UPQC, Power-Quality Improvement, Harmonic Elimination, Voltage Interruptions, Total-Harmonic Distortion**

I. INTRODUCTION

The small-scale industries suffers and doesn't meet the stable power demand due to electric utility system gives eminent priority to large-scale industries, which leads to proliferate the distribution system ensures the quality power, power shortages, scheduled block-outs, partial-interruptions, etc [1]. Uncertainly, the usage of power-electronic devices are increased in current situation causes the poor power-quality and creates serious problems in power distribution system. The term Power-Quality (PQ) mainly intensifies on two features such as reliability and performance, subjected to current-quality, voltage-quality, supply-quality and consume-quality. Ideally PQ is defined by electric-energy with pure sinusoidal source voltage with fundamental frequency with constant amplitude. Severe techno-economic impacts are well experienced because of current and voltage imperfections in common point of distribution system [2].

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The presence of PQ issues is not new in distribution system, but realization of PQ issues has been recently increased by end-user level consumers. This large-sized non-linear load provokes the harmonic distortions in current sequences with non-ideal power-factor which initiates the critical obstacles in distribution system. On other side, some utility-side PQ issues are concentrates on voltage quality issues like voltage interruptions, voltage sag-swell, voltage harmonics, unbalanced voltages, faulty situations, so on, creates the major obstacles in distribution system [3]. Formal, PQ mitigation schemes like passive devices are available which are unsuitable due to limited compensation characteristics; hence, an attractive active compensation scheme is required to achieve enhanced PQ features in distribution system [4], [5].

The obstacles posed by electric power systems and exploring feasible PQ has been attracted more researchers into this area. Several emerging methodologies are defined such as Flexible AC Transmission System (FACTS) and Custom-Power Devices (CPDs) finds feasible results of continuous enhancement of PQ issues. In general, FACTS devices are significantly used in transmission system for compensating reactive power and control the reliable power flow with unity power-factor [6]. The application of power semi-conductor technology to distribution system for more beneficial to group of consumers, both FACTS and CPD techniques compensates PQ issues but their operational strategy and control is different. The CP devices are classified based on PQ issues such as Distributed Static Compensator (D-STATCOM), Dynamic-Voltage Restorer (DVR) and Unified-PQ Compensator (UPQC), etc [7]. This class of devices is highly developed to overcome all current-voltage related PQ issues and improves reactive power and harmonic distortions generated and/or absorbed by load apparatus.

This custom-power technology utilizes power-electronic converters to achieve quality power, reliable operation, continuity power, etc. The well recognized devices in CPD technology utilizes Voltage-Source Inverters (VSI) for PQ enhancement integrated between utility-grid system and consumer side appliances. The UPQC is an updated PQ compensating device relatively new member of CPD family and consisted as combination of both series and shunt compensators [8]. The unique VSI topologies connected as back-to-back formation simultaneously handles load current and source voltage concerns integrated at Point of Common-Coupling (PCC) of three-phase 3-wire and/or 4-wire distribution system. But, it is inappropriate for multi-feeder distribution system, an alternate choice of multi-feeder CPD's can be used for compensating PQ issues in own and adjacent feeders.

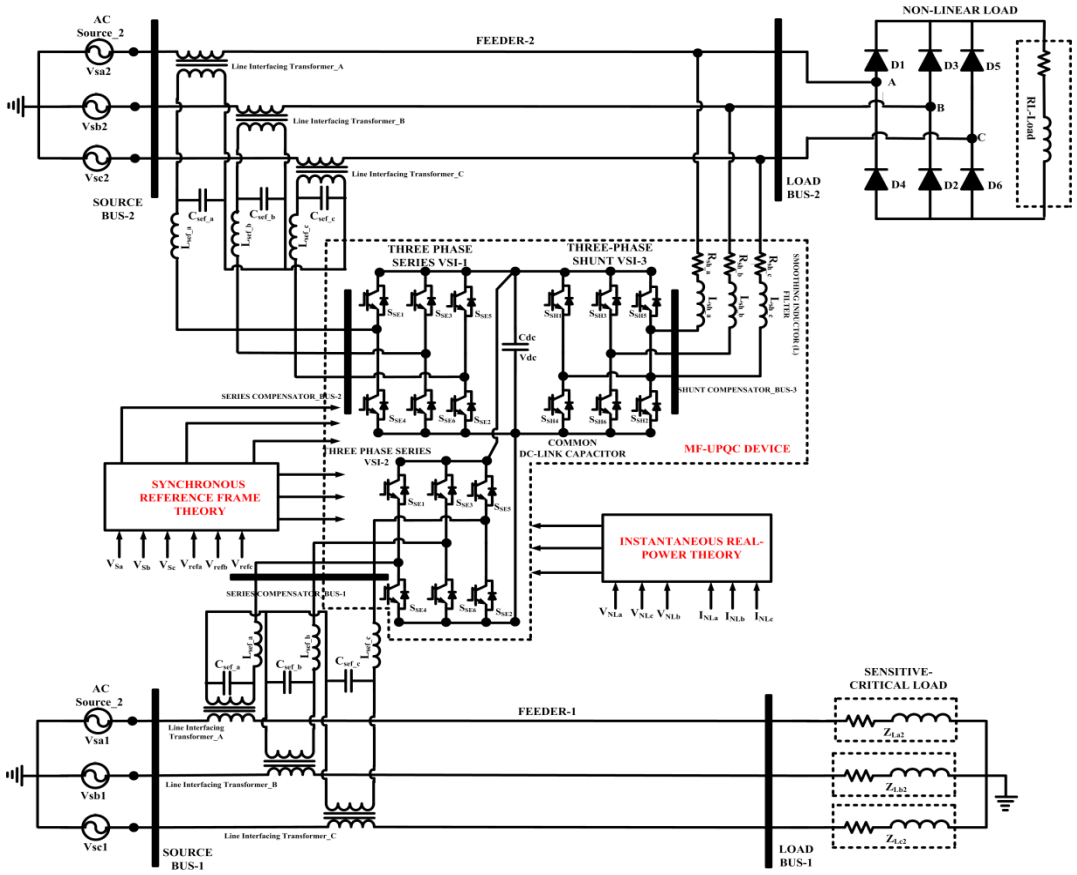


Fig.1 Schematic Diagram of Proposed MF-UPQC Device

The concept of multi-feeder CPD techniques pre-requisites multi-VSI topologies integrated as shunt-series, series-series and series-shunt via common DC-link capacitor in between two adjacent feeders. Various MF-CPD techniques are studied such as, Interline DVR [9], Interline Power-Flow Compensator (IPFC) [10], Interline-UPQC [11], so on for furnishing the optimal compensation features. This MF-CP device compensates all PQ issues in both single and multi-feeders, voltage-current qualities with additional features like load-sharing, regulate sudden interruptions, enhance the stable operation, etc. In this work, Multi-Feeder UPQC device is proposed to compensate PQ issues in multi-feeder distribution system with attractive control strategies. The performance evaluation of proposed MF-UPQC is verified under various case studies with the help of Matlab/Simulink tool, results are validated with improved PQ features.

II. PROPOSED MF-UPQC DEVICE

The proposed MF-UPQC consisting of 3-VSI structures established as one shunt-VSI for compensating all current related issues in feeder-2 and another two as series-VSI formation for compensating all voltage related issues in both feeders. These three-VSI structures are powered by a common DC-link capacitor (C_{dv}) and interfaced to multi-feeder distribution system through line-integrated 1:1 transformers (for series-VSI only). The proposed MF-UPQC device is more capable to improve PQ in multi-feeder system as well as load-sharing capability between the neighboring feeders. The MF-UPQC device is mitigating any level of interruptions in feeder-1, no need of any energy-back up. The secondary side of line integrating transformers (LT-1 and LT-2) is connected in series with the main feeder-1 and adjacent feeder-2. The schematic configuration of proposed MF-UPQC device is presented in Fig.1.

In this configuration, shunt-connected VSI of MF-UPQC in feeder-2 mitigates the all current related issues like current harmonic distortions, reactive power control, power-factor correction, unbalanced load, coming from power-electronic conversion based non-linear load and sustains DC-link voltage as constant. The series-connected VSIs of MF-UPQC in both feeder-1 and feeder-2 mitigates the all voltage-related issues like voltage interruptions, voltage-sag, voltage swell, unbalanced voltages, several fault cases, etc, and injects the 38% of available power from a DC-link point of feeder-2. In this system, a high sensitive Non-Linear (NL-2) load comprising of three-phase Uncontrolled-Bridge Rectifier (UBR) load furnishing the respective conversion energy to combination of resistive-inductive RL-load is connected to feeder-2. The other critical loads (L-1) in feeder-1 consisting of regular sensitive balanced load as Resistive-Inductive (RL) is connected to feeder-1 which pre-requisites pure sinusoidal and fundamental voltage terms.

III. CONTROL STRATEGIES OF PROPOSED MF-UPQC DEVICE

The proposed MF-UPQC device requires well-professional control objectives to acquire attractive control performance in MF-distribution systems.

The attractive control objectives play a key role in power-electronic controlled CPD techniques for furnishing feasible operation and behaviour of MF-UPQC to regulate the power system dynamics in multi-feeder distribution system. Mainly, the control schemes of MF-UPQC device comprising of complex mathematical functions for extracting reference current signals of shunt-VSI device; as well as reference voltage signals of series-VSI devices. The feasible switching functions of both series and shunt compensators in MF-UPQC device is attained by sending proper information to control functions through sensing elements. In general, for sensing the harmonic distortions a harmonic analyzer is pre-requisite and for sensing voltage issues a potential transformer is required. Based on these sensing signals, respective controller extracts the reference voltage/current sequences for controlling the action of both series- VSI and shunt-VSI of MF-UPQC through gate-drive circuitry. The main intension of control schemes are furnishing information to respective compensation structures as well as maintaining DC-link voltage as constant for regulation of loss power.

A. Control Scheme for Shunt-VSI of MF-UPQC in Feeder-2

The control scheme for Shunt-VSI of MF-UPQC in feeder-2 is considered as attractive Instantaneous Real-Power Theory (IRPT) for extraction of reference current sequences with controllable active-reactive power quantities. The working principle of IRPT is carried-out based on conversion of three-phase (abc) sequences to two-phase ($\alpha\beta$) sequences accorded in orthogonal frame by using Clarke's Transformation system [12]. Various inputs of IRPT are sensed from sensing elements of load voltages of feeder-2 (V_{L2-abc}) and three-phase NL-load currents ($i_{NL2-abc}$) are the inputs of conversion scheme. This conversion scheme provides the voltage & current sequences in orthogonal coordinates ($V_{L2\alpha\beta}, I_{NL2\alpha\beta}$) as instantaneous real-reactive quantities. The $V_{L2\alpha\beta}$ *and* $I_{NL2\alpha\beta}$ quantities posed on axis-a and axis-b respectively and the amplitudes of are changed with positive and/or negative time instants. By utilizing this transformation process, various functions in three-phase sequences are described in rotating-reference frame as represented in Eqn. (1) & Eqn. (2).

$$\begin{bmatrix} v_{L2-\alpha} \\ v_{L2-\beta} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \cdot \begin{bmatrix} v_{L2-a} \\ v_{L2-b} \\ v_{L2-c} \end{bmatrix} \quad (1)$$

$$\begin{bmatrix} i_{NL2-\alpha} \\ i_{NL2-\beta} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \cdot \begin{bmatrix} i_{NL2-a} \\ i_{NL2-b} \\ i_{NL2-c} \end{bmatrix} \quad (2)$$

The active and reactive power in rotating reference frame (αβ) over classical power strategy for three-phase components can be defined as,

$$p = v_{L2-\alpha} i_{NL2-\alpha} + v_{L2-\beta} i_{NL2-\beta} \quad (3)$$

$$q = -v_{L2-\beta} i_{NL2-\alpha} + v_{L2-\alpha} i_{NL2-\beta} \quad (4)$$

These instantaneous active & reactive power values are illustrated under matrix formation is depicted as below;

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} v_{L2-\alpha} & v_{L2-\beta} \\ -v_{L2-\beta} & v_{L2-\alpha} \end{bmatrix} \begin{bmatrix} i_{NL2-\alpha} \\ i_{NL2-\beta} \end{bmatrix} \quad (5)$$

The (αβ) currents are extracting based on conversion theme as described in below Eqn. (13),

$$\begin{bmatrix} i_{NL2-\alpha} \\ i_{NL2-\beta} \end{bmatrix} = \frac{1}{\Delta_k} \begin{bmatrix} v_{L2-\alpha} & v_{L2-\beta} \\ -v_{L2-\beta} & v_{L2-\alpha} \end{bmatrix} \begin{bmatrix} p \\ q \end{bmatrix} \quad (6)$$

Where,

$$\Delta_k = v_{L2-\alpha}^2 + v_{L2-\beta}^2 \quad (7)$$

The instantaneous active (p), reactive power (q) can be constituted in a oscillatory AC and DC-average components defined as,

$$p = \bar{p} + \tilde{p}$$
$$q = \bar{q} + \tilde{q} \quad (8)$$

Where, $\bar{p}, \bar{q}$ represents the averaged DC component, $\tilde{p}, \tilde{q}$ represents the oscillatory AC quantities. Based on above-mentioned equations final reference current ($i_{c2-\alpha\beta}^*$) form IRPT scheme can be represented in below Eqn. (9),

$$\begin{bmatrix} i_{c2-\alpha}^* \\ i_{c2-\beta}^* \end{bmatrix} = \frac{1}{\Delta_k} \begin{bmatrix} v_{2-L\alpha} & -v_{L2-\beta} \\ v_{L2-\beta} & v_{L2-\alpha} \end{bmatrix} \begin{bmatrix} p \\ q \end{bmatrix} \quad (9)$$

The active current quantities are generated based on extraction of non-linear currents and main source voltages in orthogonal αβ frame by utilizing second-order High-pass filter. This filter regulates the low-order frequencies enables the high-order frequencies pretended in reference-current extraction. With respect to controlling the orthogonal frame quantities, the voltage of DC-link capacitor as (V_{dca}) is administered by employing Proportional-Integral (PI) controller, which is mainly used for extended loss-power extraction and constant DC-link voltage. The attained reference DC-link voltage (V_{dcr}^*) and obtained DC-link voltage (V_{dca}) is differentiated for error current sequences which is administered by PI controller for acquiring active-current value as (Δ_{iNL-2}) at n[th] instants are illustrated in below Eqn. (10) & Eqn. (11),

$$V_{dcer} = V_{dcr}^* - V_{dca} \quad (10)$$

$$\Delta_{iNL-2} = \Delta_{iNL-2n} - K_{p2} * \left(V_{dcer\,(n)} - Vdcer\,(n-1) + Ki2 * Vdcer\,(n)\right) \quad (11)$$

The generation of active-current component (Δ_{iNL-2}) and fundamental reference current ($i_{c2-\alpha\beta}^*$) can be incorporated to extended reference current sequences in αβ-orthogonal frame; it can be retransformed to (abc) quantities as (i_{R2-abc}^*) is described in below Eqn. (12),

$$\begin{bmatrix} i_{R2-a}^* \\ i_{R2-b}^* \\ i_{R2-c}^* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1/\sqrt{2} & 1 & 0 \\ 1/\sqrt{2} & -1/2 & \sqrt{3}/2 \\ 1/\sqrt{2} & -1/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} i_0^* \\ i_{c2-\alpha}^* \\ i_{c2-\beta}^* \end{bmatrix} \quad (12)$$

The schematic configuration of IRPT control scheme for shunt-VSI of MF-UPQC in feeder-2 is illustrated in Fig.2. The extraction of reference current (i_{R2-abc}^*) and actual current $i_{sa2-abc}$ are the key inputs of Hysteresis Current Controller (HCC) for generation of feasible switching states to shunt-VSI of MF-UPQC device. Typically, HCC is highly engaged for providing feasible switching states to shunt-VSI of MF-UPQC based on certain limits of hysteresis bands. These bands establish the boundary limits of reference current controlled between these upper and/or lower limits, it swings continuously between these bands followed by fundamental reference current for generation of switching states.

B. Control Scheme for Series-VSI of MF-UPQC in Feeder-1 and Feeder-2

The series-VSI of MF-UPQC device accomplishes the voltage control action to mitigate voltage harmonic, voltage interupptions, voltage sag-swell and all voltage-related PQ issues in both feeder-2 and feeder-1.

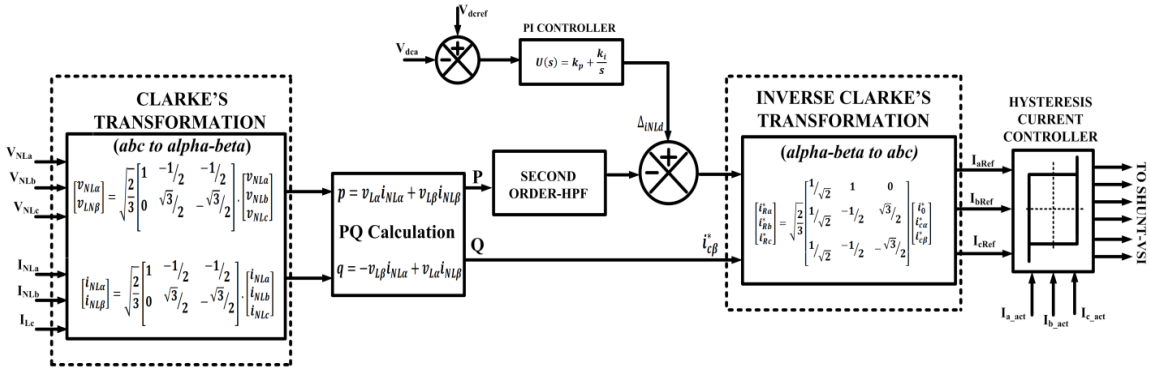


Fig.2 Schematic Configuration of IRPT Based Control Scheme for Shunt-VSI of MF-UPQC Device

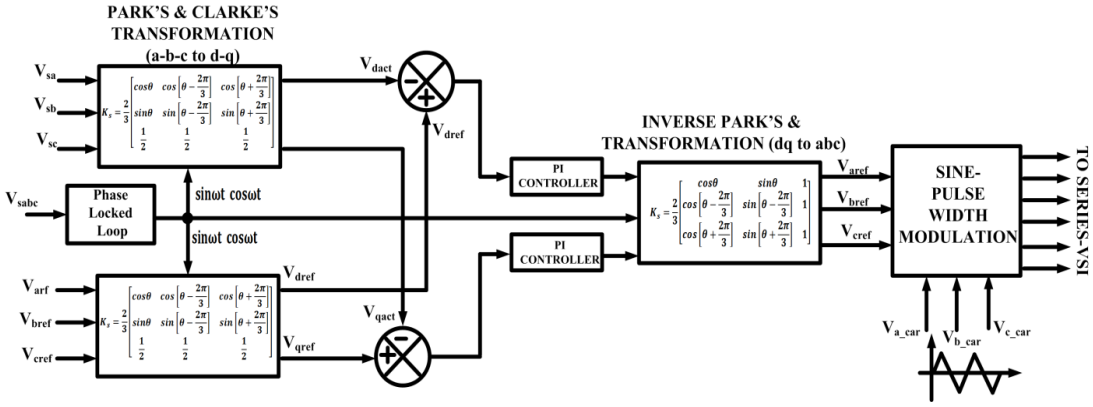


Fig.3 Schematic Configuration of Dual-SRFT Based Control Scheme for Series-VSI of MF-UPQC Device

A well-performed control objective is the optimal selection for supelative operating charactersitics of serie-VSI of MF-UPQC device, based on contro analogy of respective load voltage with measured feeder voltage.The received error sequences are dynamically resolved by differentiating the reference and desired voltage vectors. The desired unit-sinusoidal vector functions are generated by using Phase-Locked Loop (PLL) which is acts as in-phase condition of main source voltage [13]. The desired load voltages of feeder-1 and feeder-2 ($V_{L12-abc}$) are transformed into analogous $dq0$ quantities as ($V_{dq012-act}$) by using Park's transformation procedures.

$$\begin{bmatrix} V_{d12-act} \\ V_{q12-act} \\ V_0 \end{bmatrix} = \frac{2}{3}\begin{bmatrix} cos\theta & cos\left[\theta-\frac{2\pi}{3}\right] & cos\left[\theta+\frac{2\pi}{3}\right] \\ sin\theta & sin\left[\theta-\frac{2\pi}{3}\right] & sin\left[\theta+\frac{2\pi}{3}\right] \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}\begin{bmatrix} V_{L12-a} \\ V_{L12-b} \\ V_{L12-c} \end{bmatrix} \quad (13)$$

The abgular velocity "ω" and their displacement factor θ is accomodated by

$$\theta = \int \omega dt \quad (14)$$

The controller function of series-VSI of MF-UPQC experiences the *abc* to *dq0* transformation procedure of both desired and reference voltages. The reference voltages in *dq0* frame is illustrated in below Eqn. (15),

$$\begin{bmatrix} V_{d12-ref} \\ V_{q12-ref} \\ V_0 \end{bmatrix} = \frac{2}{3}\begin{bmatrix} cos\theta & cos\left[\theta-\frac{2\pi}{3}\right] & cos\left[\theta+\frac{2\pi}{3}\right] \\ sin\theta & sin\left[\theta-\frac{2\pi}{3}\right] & sin\left[\theta+\frac{2\pi}{3}\right] \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}\begin{bmatrix} V_{S12-a} \\ V_{S12-b} \\ V_{S12-c} \end{bmatrix} \quad (15)$$

The outcome responses of transfomation procedures such as ($V_{dq12-act}$) is differentiated to reference voltages in *dq* frame is ($V_{dq12-ref}$) produces some error sequences which are minimized by PI controller.

$$V^*_{dq12-er} = V_{dq12-ref} - V_{dq12-act} \quad (16)$$

$$\Delta V^*_{dq12} = \Delta_{Vdq12-er} - K_{pg} * \left(V_{dq12-ref}(n) - Vdq12-ref(n-1) + Kig * Vdq12-ref(n)\right) \quad (17)$$

Where, k_{pg} represents the proportional gain factor and k_{ig} represents the integral-gain factor of PI controller values evluated by using trial-error method. Hence, the error coming from differentiation process is eradicated by PI controller and produces the reference voltage voltage in *dq0* frame $V^*_{dq12-ref}$ which is re-transfomed to *abc* frame $V^*_{abc12-ref}$ for generation of feasible switching states to series-VSI of MF-UPQCs in MF-distribution system.

$$\begin{bmatrix} V_{a12-ref} \\ V_{b12-ref} \\ V_{c12-ref} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} cos\theta & sin\theta & 1 \\ cos\left[\theta - \frac{2\pi}{3}\right] & sin\left[\theta - \frac{2\pi}{3}\right] & 1 \\ cos\left[\theta + \frac{2\pi}{3}\right] & sin\left[\theta + \frac{2\pi}{3}\right] & 1 \end{bmatrix}\begin{bmatrix} V^*_{d12-ref} \\ V^*_{q12-ref} \end{bmatrix} \quad (18)$$

The final reference voltage vector in *abc* frame $V^*_{abc12-ref}$ is forwarded to Sinuoidal Pulse-Width Modulation (SPWM), in that reference voltage vector is compared to high switching frequency trainagular carrier vector for generation of swithing states to series-VSI of MF-UPQC. The schematic configuration of control scheme for series-VSI of MF-UPQC is depicted in Fig.3.

IV. SIMULATION RESULTS

The simulation analysis is evaluated under various case studies for validating the proposed MF-UPQC performance by using Matlab/Simulink tool, results are illustrated with improved PQ features. In feeder-1 is affected by voltage interruptions, voltage-harmonics, voltage sag-swell issues defined by controlled voltage source and compensated these voltage issues by using series-VSI of MF-UPQC in feeder-1. In feeder-2, current harmonics, reactive power control, power-factor correction, voltage sag-swell are the key issues and compensated by shunt-series formed VSIs of MF-UPQC using certain parameters. The operating parameters of proposed MF-UPQC are taken as generalized values from various literatures for PQ enhancements are depicted in Table.1.

Table.1 Operating Parameters of Proposed MF-UPQC for PQ Enhancement

S. No	Parameters	Values	
		Feeder-1	Feeder-2
1	Source Voltage (V_{rms})	V_{s1}-415V, 50Hz	V_{s2}-415V, 50Hz
2	Source Impedance	R_{s1}=0.15Ω, L_{s1}-0.9mH	R_{s1}=0.15Ω, L_{s1}-0.9mH
3	Load Impedance	R_L=30 Ω, L_L-20 mH (NL-Load)	V_L=415V, 50Hz, P_L=10KW, Q_L=5KVar (Critical Load)
4	Line Integrated (1:1) Linear Transformer	415V, 50Hz, 5KVA, Linear Model, 10% Leakage Reactance	415V, 50Hz, 5KVA, Linear Model, 10% Leakage Reactance
5	Series-VSI Filter Module	L_{se}-3 mH, C_{se}-100µF	L_{se}-3 mH, C_{se}-100µF
6	Shunt-VSI Filter Module	--	R_{sh}= 0.001 Ω, L_{sh}-10 mH
7	DC-Link Capacitor	V_{dca}= 880V, C_{dca} =1500µF	

A. Performance Analysis of Series-VSI of MF-UPQC in Feeder-1

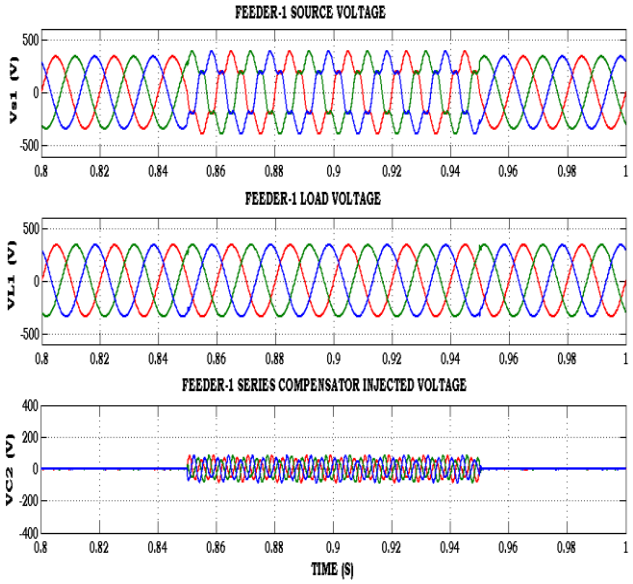
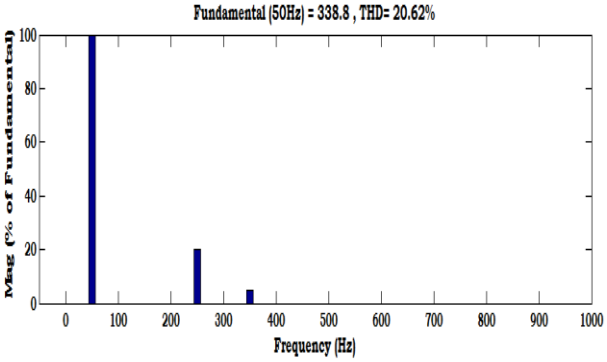
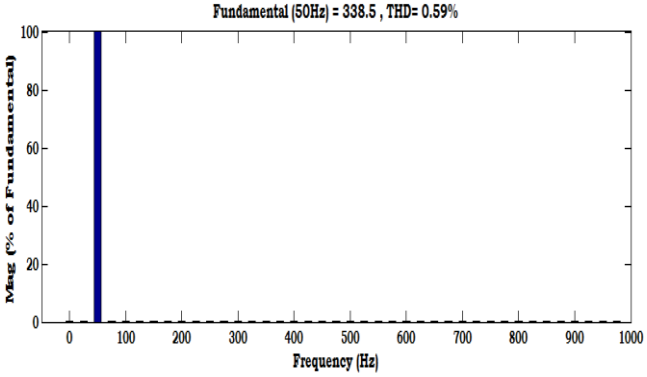


Fig.4 Performance Analysis of Series-VSI of MF-UPQC in Feeder-1 under Voltage Harmonics



(a) THD Analysis of Source Voltage



(b) THD Analysis of Load Voltage

Fig.5 Harmonic Analysis of Source & Load Voltages in Feeder-1 during Presence of Harmonics

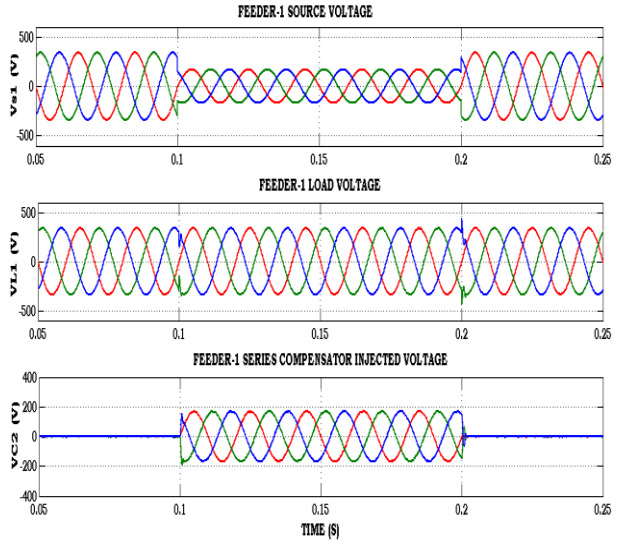


Fig.6 Performance Analysis of Series-VSI of MF-UPQC in Feeder-1 under Voltage Sag

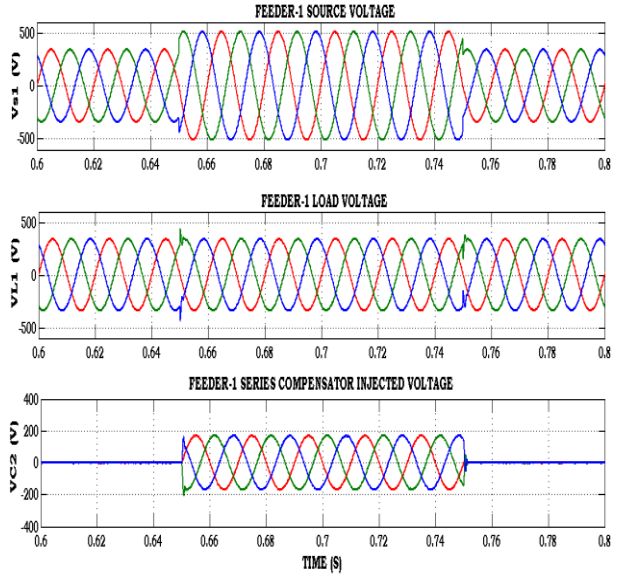


Fig.7 Performance Analysis of Series-VSI of MF-UPQC in Feeder-1 under Voltage Swell

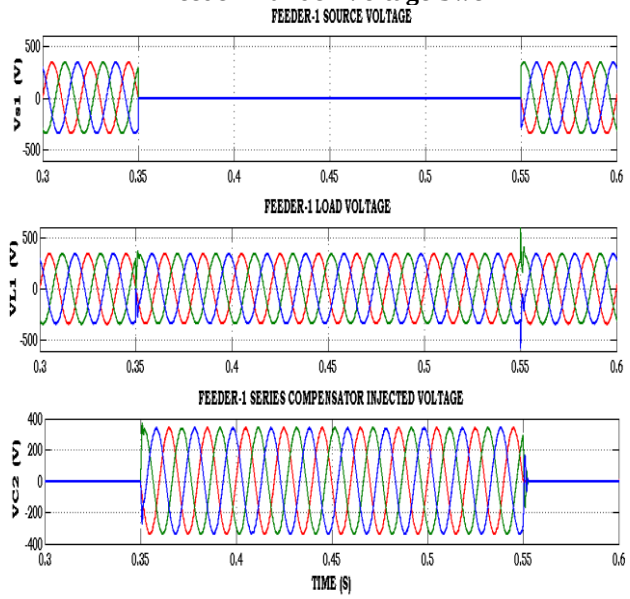


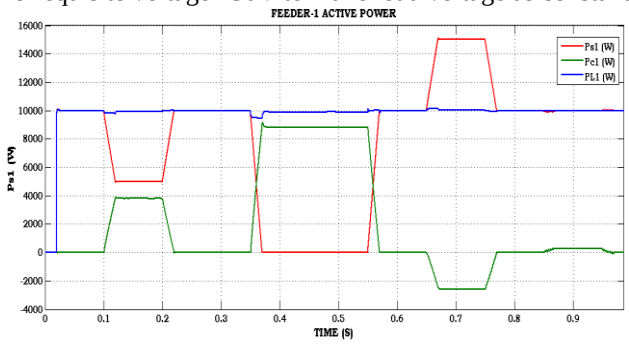
Fig.8 Performance Analysis of Series-VSI of MF-UPQC in Feeder-1 under Voltage Interruptions

The performance analysis of series-VSI of MF-UPQC in Feeder-1 is verified under voltage harmonics as depicted in Fig.4. This feeder-1 is powered by 415V rms, 50Hz supply system for achieve the critical load system, during voltage harmonics at a time instant between 0.85 sec<t<0.95 sec source voltage is affected due to 5^{th} order & 7^{th} order harmonics presented in source voltage and creates serious problem in feede-1. In this period, series-VSI of MF-UPQC in feeder-1 is injected some voltage based on in-phase opposition principle to compensate voltage harmonics in load voltage and maintains sinusoidal & harmonic-free response. In Fig.5, harmonic analysis is presented, the THD analysis of source voltage during harmonic presence attains 20.62% and during harmonic elimination attains 0.59%, and it is well within IEEE-519 standards compensated by series-VSI of MF-UPQC.

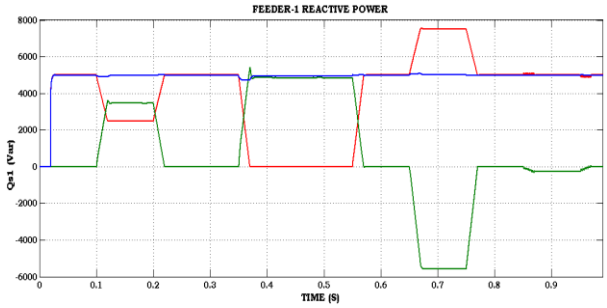
The performance analysis of series-VSI of MF-UPQC in Feeder-1 is verified under voltage-sag as depicted in Fig.6. At pre-sag condition before 0.1 sec source voltage is maintained as constant with a value of 340V, because of non-presence of voltage sag in feeder-1. During voltage sag is applied between 0.1 sec<t<0.2 sec in feeder-1, due to sag in the source voltage slightly decreased to 170V. But, the load voltage is maintained constant 340V because of series-VSI of feeder-1 injects required voltage 170V to make load voltage as constant.

The performance analysis of series-VSI of MF-UPQC in Feeder-1 is verified under voltage-swell as depicted in Fig.7. At pre-swell condition before 0.65 sec source voltage is maintained as constant with a value of 340V, because of non-presence of voltage swell in feeder-1. During voltage swell is applied between 0.65 sec<t<0.75 sec in feeder-1, due to swell in the source voltage increasing to 510V. But, the load voltage is maintained constant 340V because of series-VSI of feeder-1 injects/absorbs the additional voltage 170V to make load voltage as constant.

The performance analysis of series-VSI of MF-UPQC in Feeder-1 is verified under voltage-interruptions as depicted in Fig.8. At pre-interrupted condition before 0.35 sec source voltage is maintained as constant with a value of 340V, because of non-presence of voltage interruptions in feeder-1. During voltage interruptions is applied between 0.35 sec<t<0.55 sec in feeder-1, due to these interruptions source voltage decreasing to 0V and affects the load voltage when compensator is not there. But, the load voltage is maintained constant 340V because of series-VSI of feeder-1 injects the pre-requisite voltage 430V to make load voltage as constant.



(a) Active Power



(b) Reactive Power

Fig.9 Active power & Reactive Power of Source, Load, Compensator in Feeder-1 of MF-UPQC during various case studies

At pre-sag condition before 0.1 sec, the active power of source is maintained constant with a value of 10KW, during voltage sag applied between 0.1 sec<t<0.2 sec in feeder-1, the source active power is slightly decreased to 5KW because of sag condition. In that situation, the series-VSI of MF-UPQC injects required active power to load as 5KW to make load active power is constant 10KW as depicted in Fig.9 (a). As well as, the reactive power of source is maintained constant with a value of 5KVar during pre-sag condition. During sag condition, the reactive power of source is decreased to 2.5KVar; the series-VSI of MF-UPQC injects the additional reactive power 2.5KVar to load to maintain load reactive power as constant with a value of 5KVar as depicted in Fig.9 (b). Likewise, all the above cases the active power and reactive powers are maintained constant by using series-VSI of MF-UPQC for enhancing greater PQ features in feeder-1 distribution system.

B. Performance Analysis of Series-VSI/Shunt-VSI of MF-UPQC in Feeder-2

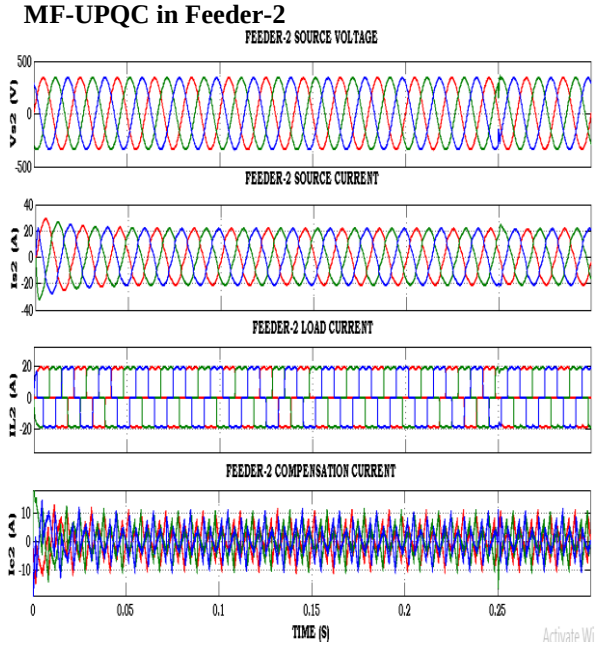
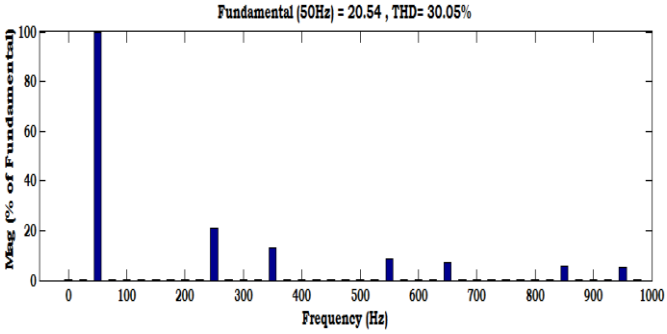
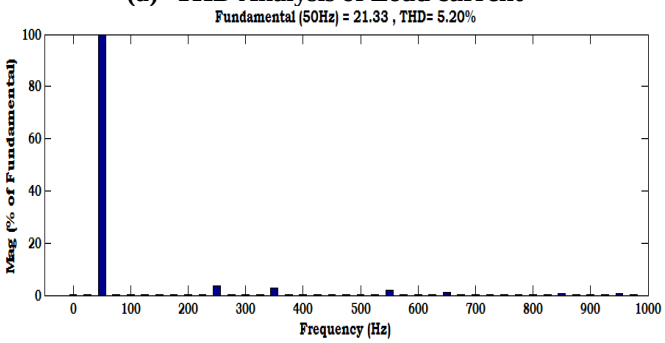


Fig.10 Performance Analysis of Series-VSI/Shunt-VSI of MF-UPQC in Feeder-2 under Current Harmonic Distortions

The performance analysis of series-VSI/shunt-VSI of MF-UPQC in feeder-2 under current harmonic distortions is depicted in Fig.10. The feeder-2 is powering the three-phase non-linear DBR load with 415V, 50Hz supply system. Due to non-linear load loads, the source current is harmonized and creates major issue in feeder-2 like more heat loss; high current flow over the rated current damages the entire load system. For elimination of harmonics coming from NL-load is counteracted by utilizing shunt-VSI of MF-UPQC using attractive control scheme. The proposed shunt-VSI of MF-UPQC compensates all harmonics distortions as in-phase opposition principle and provides pure-sinusoidal voltage with balanced nature. In Fig.11, harmonic analysis is presented, the THD analysis of load current due to non-linear load attains 30.05%% and eliminates the harmonic distortions in source current with a value of 5.20%, and it is well within IEEE-519 standards compensated by shunt-VSI of MF-UPQC.



(a) THD Analysis of Load current



(b) THD Analysis of Source current

Fig.11 Harmonic Analysis of Source & Load Current in Feeder-2 during Presence of Current Harmonics

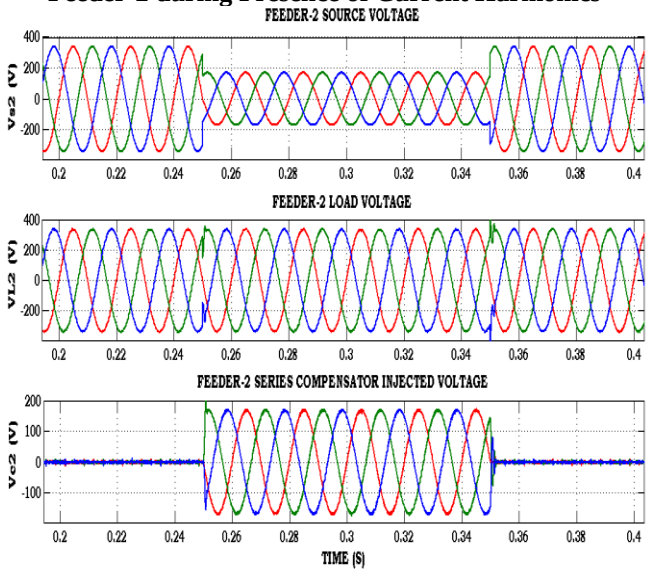


Fig.12 Performance Analysis of Series-VSI of MF-UPQC in Feeder-2 under Voltage Sag

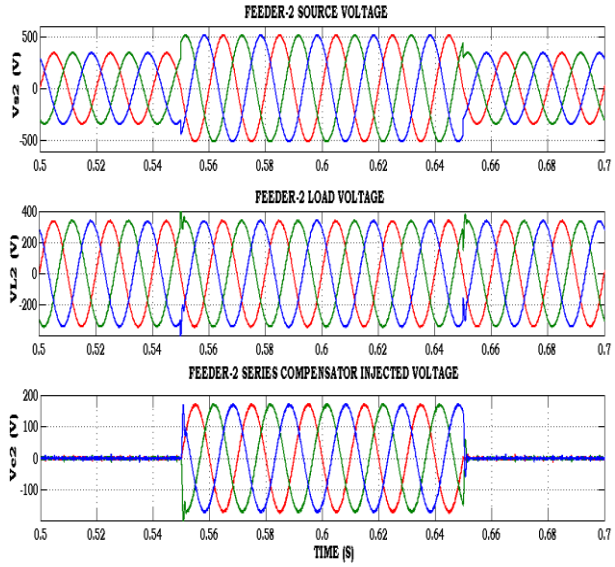


Fig.13 Performance Analysis of Series-VSI of MF-UPQC in Feeder-2 under Voltage Swell

The performance analysis of series-VSI of MF-UPQC in Feeder-2 is verified under voltage-sag as depicted in Fig.12. At pre-sag condition before 0.25 sec source voltage is maintained as constant with a value of 340V, because of non-presence of voltage sag in feeder-2. During voltage sag is applied between 0.25 sec<t<0.35 sec in feeder-2, due to sag in the source voltage slightly decreased to 170V. But, the load voltage is maintained constant 340V because of series-VSI of feeder-2 injects required voltage 170V to make load voltage as constant.

The performance analysis of series-VSI of MF-UPQC in Feeder-2 is verified under voltage-swell as depicted in Fig.13. At pre-swell condition before 0.55 sec source voltage is maintained as constant with a value of 340V, because of non-presence of voltage swell in feeder-2. During voltage swell is applied between 0.55 sec<t<0.65 sec in feeder-2, due to swell in the source voltage increasing to 510V. But, the load voltage is maintained constant 340V because of series-VSI of feeder-2 injects/absorbs the additional voltage 170V to make load voltage as constant. The DC-link voltage of capacitor is maintained constant with a value of 880V with the help of DC-link controller and makes PCC voltage as constant as depicted in Fg.14. The source voltage is in-phase with source current to represent ideal power-factor as depicted in Fig.15.

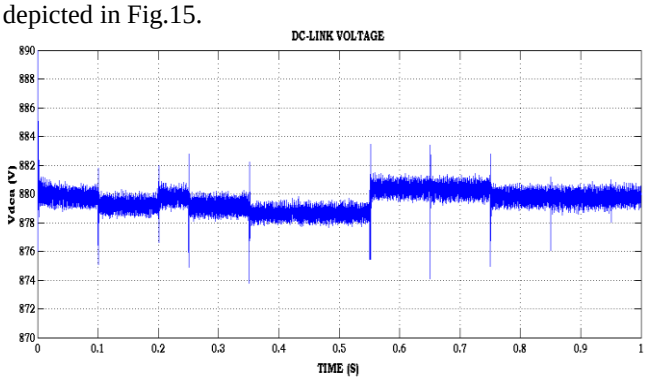


Fig.14 DC-Link Voltage

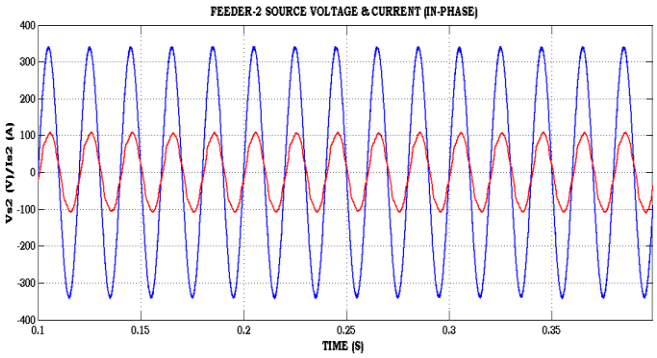
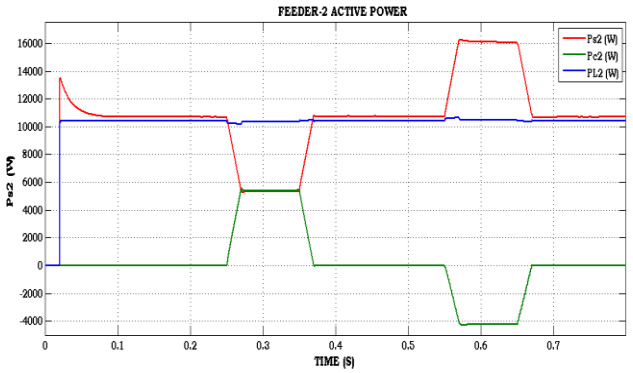
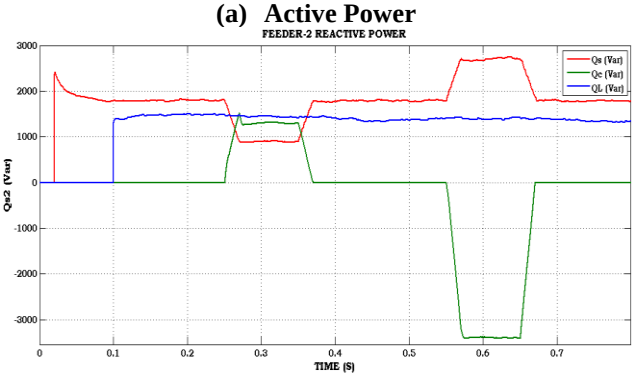


Fig.15 Source Voltage & Current (Unity-Power Factor)



(a) Active Power



(b) Reactive Power

Fig.16 Active power & Reactive Power of Source, Load, Compensator in Feeder-2 of MF-UPQC during various case studies

At pre-sag condition before 0.2 sec, the active power of source is maintained constant with a value of 10.6KW, during voltage sag applied between 0.25 sec<t<0.35 sec in feeder-2, the source active power is slightly decreased to 5.2KW because of sag condition. In that situation, the series-VSI of MF-UPQC injects required active power to load as 5.4KW to make load active power is constant 10.6KW as depicted in Fig.16 (a). As well as, the reactive power of source is maintained constant with a value of 1.8KVar during pre-sag condition. During sag condition, the reactive power of source is decreased to 0.9KVar; the series-VSI of MF-UPQC injects the additional reactive power 0.9KVar to load to maintain load reactive power as constant with a value of 1.8Kvar as depicted in Fig.16 (b). Likewise, all the above cases the active power and reactive powers are maintained constant by using series-VSI/shunt-VSI of MF-UPQC for enhancing greater PQ features in feeder-2 distribution system.

V.CONCLUSION

The comprehensive analysis of MF-UPQC in two-feeder distribution is evaluated under various case studies and offers various benefits over other MF-compensation schemes. The proposed MF-UPQC mitigates all voltage and current related PQ issues in multi-feeder distribution system by utilizing series-shunt VSI topologies with attractive control functions. It compensates voltage-harmonics, voltage-sag, voltage-swell and voltage interruptions coming in Feeder-1 and current harmonics, voltage sag/swell in Feeder-2. Ultimately for above-mentioned issues, a new MF-UPQC topology is developed with attractive operating functions evaluated by using Matlab/Simulink tool, results are presented with improved PQ features. The THD analysis of source current and load voltage values are well within IEEE limits to represent greater PQ standards. The additional advantages of this MF-distribution system is load sharing between main and neighboring feeders which reduces power-shortages, block-outs, etc. The further recommendations are carried on review of novel voltage and current controllers for providing effective performance of proposed MF-UPQC device in MF-distribution systems.

REFERENCES

1. G. Papaefthymiou, M. Houwing, M.P.C. Weijnen, L. van der Sluis, "Distributed Generation vs Bulk Power Transmission", *Infrastructure Systems and Services: Building Networks for a Brighter Future (INFRA) 2008 First International Conference on*, Nov. 2008.
2. J. H. Eto, K. H. LaCommare, "A quantitative assessment of utility reporting practices for reporting electric power distribution events", *Proc. 2012 IEEE Power & Energy Soc. General Meeting*, Jul. 22–26, 2012.
3. L. F. de Oliveira Costa, J. M. de Carvalho Filho, "Electrical power quality and the challenges faced by power assemblies applications in petrochemical industry", *IEEE Trans. Ind. Appl.*, vol. 52, no. 5, pp. 4495-4502, Sep. 2016.
4. B. Singh, A. Chandra, K. Al. Haddad. Power Quality Problems and Mitigation Techniques. Hoboken, NJ, USA: Wiley Publishers, 2015. J. C. Das, “Passive filters-potentialities and limitations,” IEEE Trans. Ind. Appli., vol. 40, no. 1, pp. 232–241, Jan. 200
5. D. Rivas, L. Morán, J.W. Dixon et al., "Improving passive filter compensation performance with active techniques", *IEEE Trans. Ind. Electron.*, vol. 50, no. 1, pp. 161-170, 2003.
6. A. Sahoo and T. Thyagarajan, "Modeling of facts and custom power devices in distribution network to improve power quality," in Power Systems, 2009. ICPS '09. International Conference on, Dec. 2009, pp. 1 -7
7. M. Farhoodnea, A. Mohamed, H. Shareef, "A comparative study on the performance of custom power devices for power quality improvement", Proc. IEEE Innovative Smart Grid Technologies, pp. 153-157, 2014
8. V. Khadkikar, "Enhancing electric power quality using UPQC: A comprehensive overview", IEEE Trans. Power Electron., vol. 27, no. 5, pp. 2284-2297, May 2012.
9. M. Shahabadini and H. Iman-Eini, "Improving the Performance of a Cascaded H-Bridge-Based Interline Dynamic Voltage Restorer," in *IEEE Transactions on Power Delivery*, vol. 31, no. 3, pp. 1160-1167, June 2016.
10. J. Muruganandham, K. Arun, K. Thangaraj and V. Malarselvam, "Performance analysis of interline unified power flow controller for parallel transmission lines," *2015 IEEE International Conference on Electrical, Computer and Communication Technologies (ICECCT)*, Coimbatore, 2015, pp. 1-8.
11. S. S. Bhosale, Y. N. Bhosale, U. M. Chavan and S. A. Malvekar, "Power Quality Improvement by Using UPQC: A Review," *2018 International Conference on Control, Power, Communication and Computing Technologies (ICCPCCT)*, Kannur, 2018, pp. 375-380.
12. K. Palanisamy, J. S. Mishra, I. J. Raglend, D. P. Kothari, "Instantaneous power theory based unified power quality conditioner (UPQC)", *Proc. Int. Conf. Power Electron. Drives Energy Syst.*, pp. 1-5, 2010-Dec.
13. M. Kesler, E. Ozdemir, "Synchronous-reference-frame-based control method for UPQC under unbalanced and distorted load conditions", IEEE Transactions on Industrial Electronics, vol. 58, no. 9, pp. 3967-3975, Sept. 2011