# Low Glitch & Low Power Dual Edge Triggered D-Type Flip Flops for Integrated Applications

**Viresh Pandey, Pramod Kumar Jain, Devendra Singh Ajnar**

*Abstract— This paper presents Dual Edge Triggered (DET) master slave D-Type flip flops for glitch free, low power, low delay, low silicon area and low Power Delay Product (PDP). This DET master slave D-Type flip flops are compared against the existing DET flip flops using 45nm & 180nm CMOS technology which has been simulated using Cadence Virtuoso. The proposed DET master slave D-Type flip flops has reduced the number of transistors in use for operation, which leads to low glitch, low power and low delay design. Paper consist glitch free DET master slave D-Type flip flops analysis for power, delay and PDP. The proposed DET flip flop is also simulated and implemented for 18nm Fin-FET in Cadence Tool.*

*Index Terms— Dual Edge Triggered (DET), master slave, D-Type flip flop, glitch, clock signal, power, delay, Power Delay Product (PDP).*

## I. INTRODUCTION

Flip flop is a timing element in a digital circuit, which impact on speed and power element of circuit. Its performance is an important element to evaluate the performance of the complete synchronous circuit [9]. Dual Edge Triggered (DET) synchronous operation is a very interesting option for low power, low delay and high performance in designing of flip flop [2]. DET flip flop is able to provide the same result at the half of clock frequency in comparison to single edge triggered (SET) flip flop [6], which leads to notable power saving of clock signal. Clock signal is one of the big contributors in total power of circuit. Flip flop is likely used for storing the information. DET flip flop is one of the recognize application for reducing the clock power. With triggering data on both rising edge and falling edge of the clock signal, frequency of clock signal reduces by 50% without changing the circuit output. This leads to overall impactful circuit power saving, because it reduces the power consumption of clock signal into half from the regular one. DET flip flop is more complex and usually large from SET flip flop but they can be designed to become more energy efficient [1][3],

which leads to additional power saving in the circuit.Performance and fault forbearance capability of device is quite affected by flip flop delay, power and reliability. Therefore, it's required to design flip flop for least power consumption & dissipation, least delay, least chip size or area, glitch free and high reliability with highest fault forbearance capability [6].

When particle touches the drain of the MOSFET, electron hole merger takes place [6], which leads to a drift transient current due to opposite biased electric field induction. Thus, voltage transient due to a collected charge is known as transient fault. This transient faults formed due to the preliminary combinational circuit glitches. In recent studies of digital VLSI design, it's predicted that scaling of device reduce the supply voltage and device capacitances, which leads to more sensitive circuit to glitches [6]. The design of energy efficient circuit is the first priority in the field of digital integrated circuits. Power consumption can be manipulated by manipulating supply voltage scaling. Power consumption caused by the glitch can't be skipped, because power consumption portion of glitch in total power consumption differ from 9% to 38%, which is very significant amount of variation in power consumption. Major portion of the power dissipation in VLSI design is imputed to clock signal [16][3]. It consumes 45% of the total circuit power consumption. Charging and discharging of clock signal has parasitic capacitors for each cycle, which leads to power dissipation that is directly proportional to clock frequency [16][3]. This is one of the main reasons which effects at different parameters among the various applications. In CMOS design there are total three reasons for power dissipation. First is signal transition, second is short circuit current due to direct flow of current from supply to ground and third is leakage current [11]. As the technology of circuit design scale decreases the chance of power dissipation increases. This paper is organized from here as follows: Section II contains the existing DET flip flops which are going to be compared with proposed DET flip flops in two different technologies. Section III contains the proposed methodology of DET flip flops Negative Phase Clock Dual Edge Triggered master slave d-type Flip Flop (NPCDETFF) and Positive Phase Clock Dual Edge Triggered master slave d-type Flip Flop (PPCDETFF). The proposed DET flip flops are designed in three different technologies, which are 180nm CMOS technology, 45nm CMOS technology and 18nm Fin-FET technology. Section IV contains simulation results and comparison of simulated results with DET flip flops of section II. Some important parameters like power and delay variations with respect to variation in frequency of input clock signal are analyzed.

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Section V contains the conclusion of proposed DET flip flop where merit and demerit of proposed DET flip flop is described.

## II. DET FLIP FLOP DESIGNS

There are many DET flip flops designed till present, every DET flip flop has its merit and demerit. Some of DET flip flops are described in this section which are going to be compared with proposed design for DET flip flop.

First DET flip flop described in this section is Dual Edge Triggered Static Pulsed Flip Flop (DETSPFF). Desari Bhargavaram et al. [2] introduced this DET flip flop shown in Fig.1.
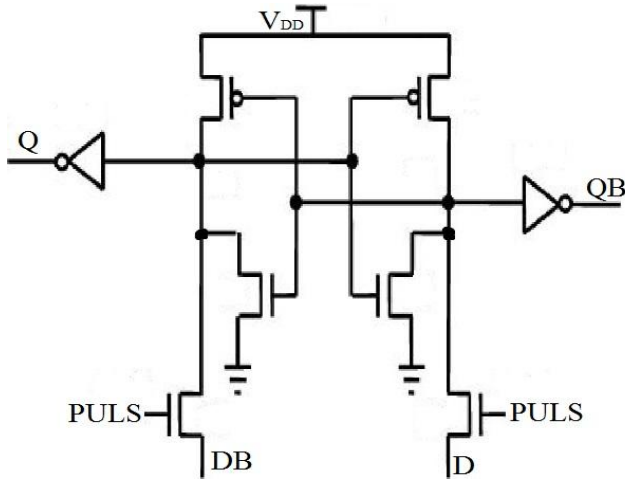


**Fig.1 Schematic diagram of DETSPFF**

The undeviating feature of DETSPFF is that, it eliminates the unnecessary transistors. It has some demerits as well. Its latency degraded due to the high capacitive load at nodes. When N3 and N4 are in off condition, there is high voltage drop across either N3 or N4 transistor. Due to this DETSPFF has high leakage current.

Second DET flip flop described in this section is Dual Edge Triggered Pulsed Flip Flop (DETPFF). Dasari Bhargavaram et al. [2] introduced this DET flip flop which is shown in Fig.2.
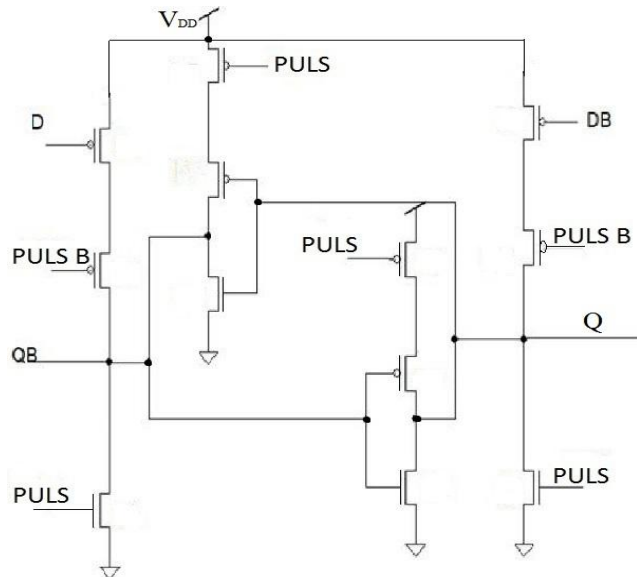


**Fig.2 Schematic diagram of DETPFF**

In this DET flip flop power consumption is reduced because when pulse is high at that time transistors of inverter section are in off condition and when pulse is low at that time only inverter section is turned on, rest of the circuit is goes in off condition. This leads to increase in speed as well.

Third DET flip flop described in this section is Dual Edge Triggered NAND keeper Flip Flop (DETNFF). Desari Bhargavaram et al. [2] introduced this DET flip flop shown in Fig.3.
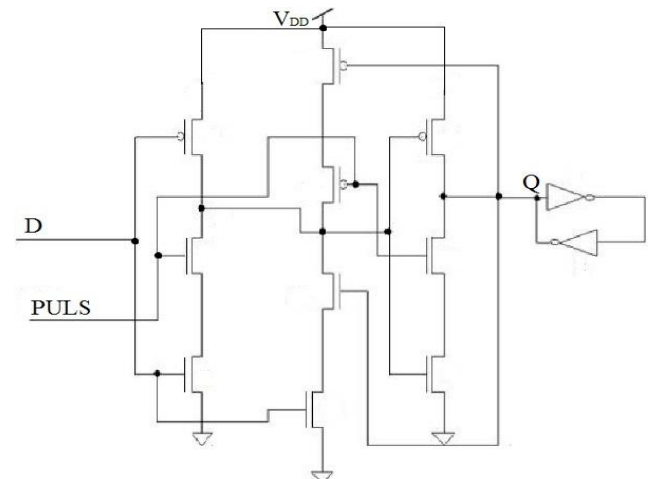


**Fig.3 Schematic diagram of DETNFF**

In this DET flip flop PMOS acts as a keeper in keeper circuit for the output, which is in high state making the gate static instead of dynamic. During pre-charge keeper is off, during the evaluation output goes low and switch on the keeper for output that remains high.

Fourth DET flip flop described in this section is Dual Edge Triggered Transmission Gate Latch MUX Flip Flop (DETTGLMFF) [3] which is shown in Fig.4.
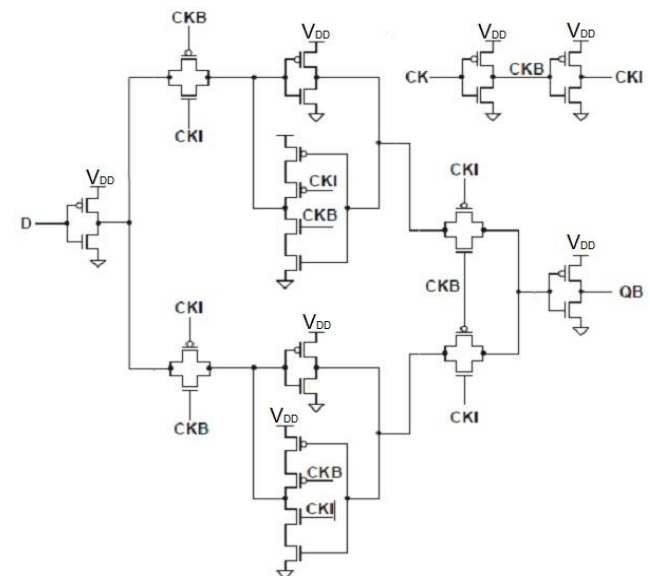


**Fig.4 Schematic diagram of DETTGLMFF**

DETTGLMFF is one of the most efficient DET flip flop. It has very low clock to Q (output) delay. This is a key feature which makes DET flip flop suitable for high frequency applications.

The major drawback of this DET flip flop is clock overlap failure. When clock overlap is large, at that time voltage stored in one latch overwrite the value stored in other latch, which leads to storage failure.

Fifth DET flip flop described in this section is Dual Edge Triggered $C^2$MOS Latch MUX Flip Flop (DETC$^2$MLMFF). A. Gago et al. [4] introduced this DET flip flop which is shown in Fig.5.
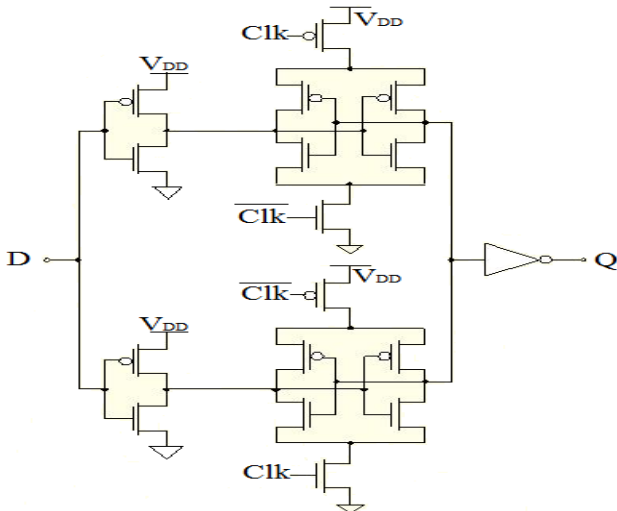


**Fig.5 Schematic diagram of DETC$^2$MLMFF**

In this DET flip flop delay is very low, because new output for every clock edge has to go through only one transistor to arrive the output port. This DET flip flop avoids charge sharing and has small transmission width. One demerit of this DET flip flop is race problem which is caused due to skew in between two clock phases.

Sixth DET flip flop described in this section is Dual Edge Triggered True Single Phase Clock Flip Flop (DETTSPCFF). Andrea Bonetti et al.[5] introduced this DET flip flop which is shown in Fig.6.
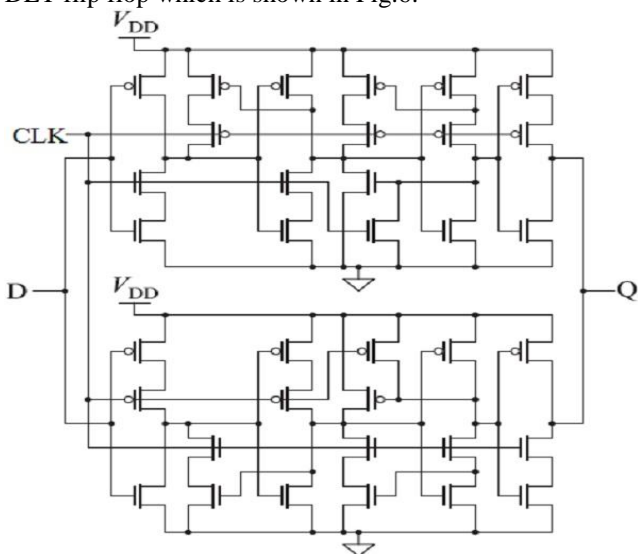


**Fig.6 Schematic diagram of DETTSPCFF**

This DET flip flop is designed to control the clock overlap problem and suitability for operation on sub threshold voltage. To overcome the clock overlap problem TSPC circuit and an internal two fold feedback circuit is used in place of an inverted clock in this DET flip flop. One demerit of this DET flip flop is that it has greater number of

transistors as compare to other DET flip flops, which leads to large area of chip size.

## III. PROPOSED DET FLIP FLOP DESIGNS

Presently, there are various techniques which are considered by researchers in VLSI design to reduce the area, delay & power for their circuit design. Proposed circuit design for DET flip flop is based on master slave D-Type flip flop. As in single edge triggered flip flops, there are two types of circuit design are there based on edge they trigger the output, same way here in this paper two types of DET master slave D-type flip flops are designed. First is Negative Phase Clock DET Flip Flop (NPCDETFF) shown in Fig.7 and second is Positive Phase Clock DET Flip Flop (PPCDETFF) shown in Fig.8. In NPCDETFF, when clock goes low then master latch turns into a memory with new state of input and slave latch produces present state of input, when clock goes high master latch turns into memory with new state of input and slave produces present state of input. It only trigger at negative edge of clock initially.
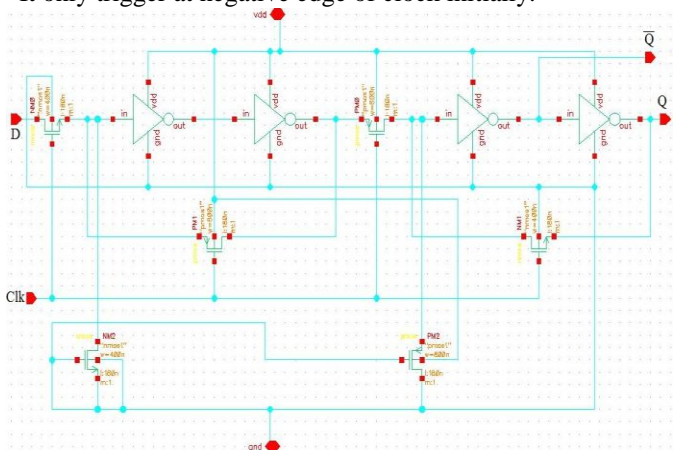


**Fig.7 Schematic diagram of NPCDETFF**

In PPCDETFF, initially when clock goes high then master latch turns into memory with new state of input and slave latch produces present state of input, when clock goes low then master latch turns into memory with new state of input and slave latch produces present state of input.
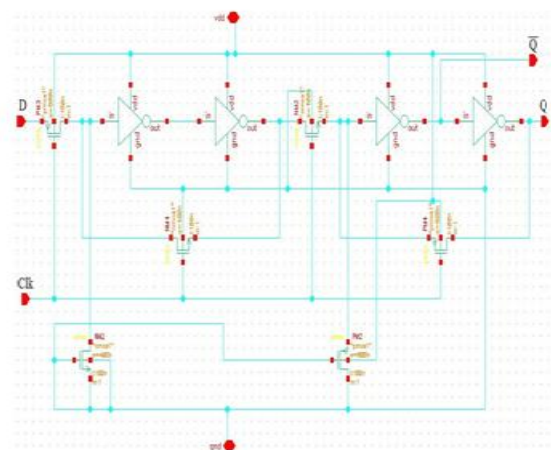


**Fig.8 Schematic diagram of PPCDETFF**

This DET flip flops are designed using only 14 transistors, which means low chip area, which leads to low power consumption.

## IV.     SIMULATION RESULTS & COMPARISION

The proposed two circuits of DET flip flops are performed through spectre pre layout and post layout simulations to verify the design at 180nm & 45nm CMOS technology and 18nm Fin-FET technology [15]. Firstly we see the simulation results for 180nm CMOS technology and its comparison with different DET flip flops, which were tested in same 180nm CMOS technology. The proposed design was simulated on same test bench as the compared DET flip flops were simulated. The compared DET flip flops simulation is applied to 180nm CMOS technology with $V_{DD}$ of 1.8V at $27^0$C and frequency of input clock signal is 600MHz. Simulation results for above mentioned values on both proposed DET flip flops and comparison with other DET flip flops in 180nm CMOS technology are shown in Table I.

**Table I Simulation Results & Comparison**

|  | Power (µW) | Delay (ps) | PDP (fJ) | No. of Transistors |
|---|---|---|---|---|
| NPCDETFF | 56.56 | 27.45 | 1.552 | 14 |
| PPCDETFF | 37.32 | 43.56 | 1.625 | 14 |
| DETSPFF [2] | 1990 | 4000 | 7960 | 18 |
| DETPFF [2] | 140 | 7300 | 1022 | 20 |
| DETNFF [2] | 347 | 5200 | 1804 | 22 |

Proposed design in 180nm CMOS technology is highly efficient as compared to other DET flip flops as shown in above table. The PDP of compared DET flip flop with proposed DET flip flops is shown in Fig.9.
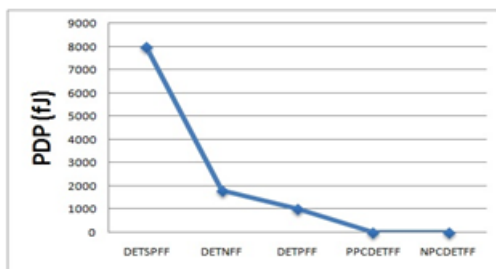


**Fig.9 PDP comparison of DET flip flops**

Variation in power and delay due to variation in frequency of input clock signal is shown in Fig.10 and Fig.11 respectively.
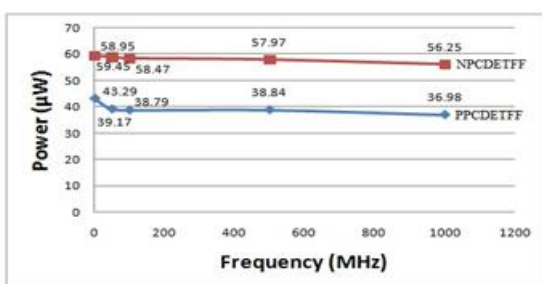


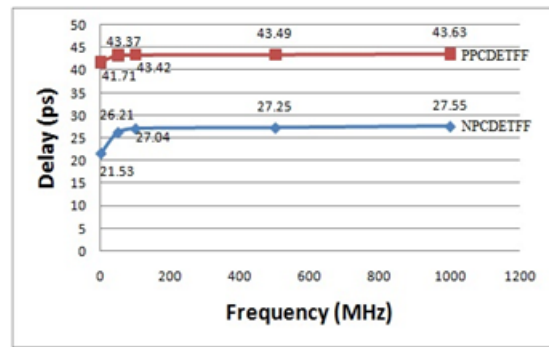**Fig.10 Power analysis at different frequencies for NPCDETFF & PPCDETFF**



**Fig.11 Delay analysis at different frequencies for NPCDETFF & PPCDETFF**

The layout of proposed NPCDETFF and PPCDETFF are designed in cadence virtuoso layout editor shown in Fig.12 and Fig.13 respectively. Area of the designed layout for NPCDETFF is $185.2455µm^2$ and for PPCDETFF is $189.20065µm^2$.
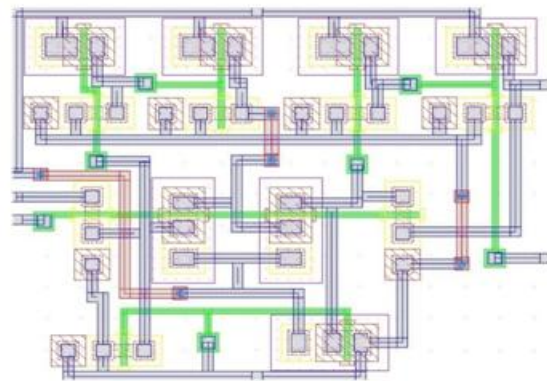


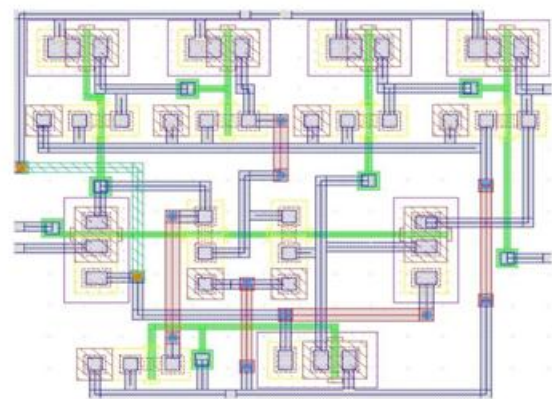**Fig.12 Layout of NPCDETFF**



**Fig.13 Layout of PPCDETFF**

The proposed NPCDETFF and PPCDETFF are simulated in 45nm CMOS technology and its results are compared with other DET flip flops, which were simulated in 40nm CMOS technology with $V_{DD}$ of 0.5V at $25^0$C and frequency of input clock signal at 500MHz.

The proposed NPCDETFF and PPCDETFF design are simulated in 45nm CMOS technology with $V_{DD}$ of 0.62V at $25^0$C and frequency of input clock signal at 500MHz to match the test bench of other compared DET flip flop as possible as close, so the comparison will be fair. Simulation results of NPCDETFF and PPCDETFF for above mentioned values in 45nm CMOS technology and comparison with other DET flip flop are shown in Table II.

**Table II Simulation Results & Comparison**

|  | Power (nW) | Delay (ps) | PDP (aJ) | No. of Transistor |
|---|---|---|---|---|
| NPCDETFF | 431.1 | 2037 | 878.1 | 14 |
| PPCDETFF | 7.75 | 7164 | 55.5 | 14 |
| DETC$^2$MLMFF [3] | 495.3 | 395.3 | 196.8 | 22 |
| DETTGLMFF [4] | 431.6 | 230.9 | 99.7 | 30 |
| DETTSPCFF [5] | 449.9 | 149.9 | 67.5 | 38 |

Proposed NPCDETFF and PPCDETFF design in 45nm CMOS technology is highly efficient compared to other DET flip flops in above table. The PDP of compared DET flip flop with proposed DET flip flops are shown in Fig.14.
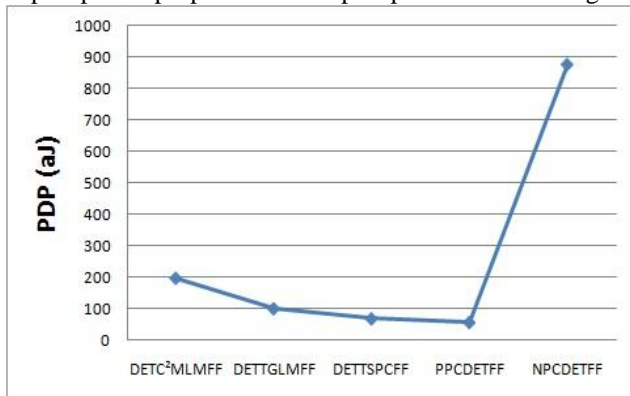


**Fig.14 PDP comparison of DET flip flops**

Variation of power and delay due to variation in frequency of input clock signal is shown in Fig.15 and Fig.16 respectively.
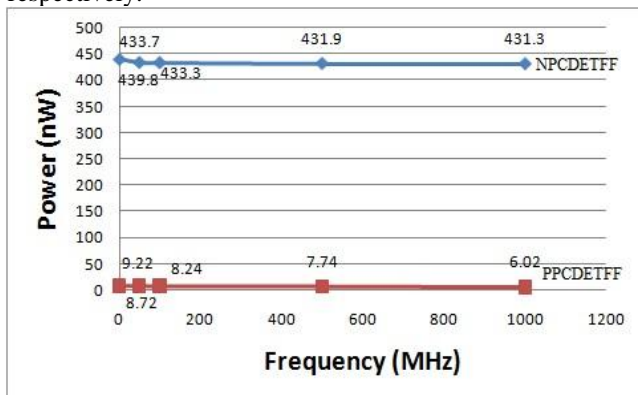


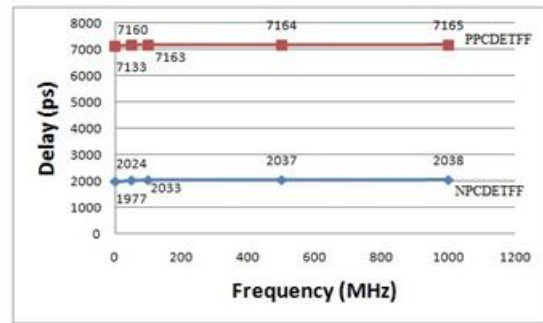**Fig.15 Power at different frequencies for NPCDETFF & PPCDETFF**



**Fig.16 Delay at different frequencies for NPCDETFF & PPCDETFF**

The layout of proposed NPCDETFF and PPCDETFF are designed in cadence virtuoso layout editor is shown in Fig.17 and Fig.18 respectively. Area of designed layout for NPCDETFF is 12.5421µm$^2$ and for PPCDETFF is 13.068µm$^2$.
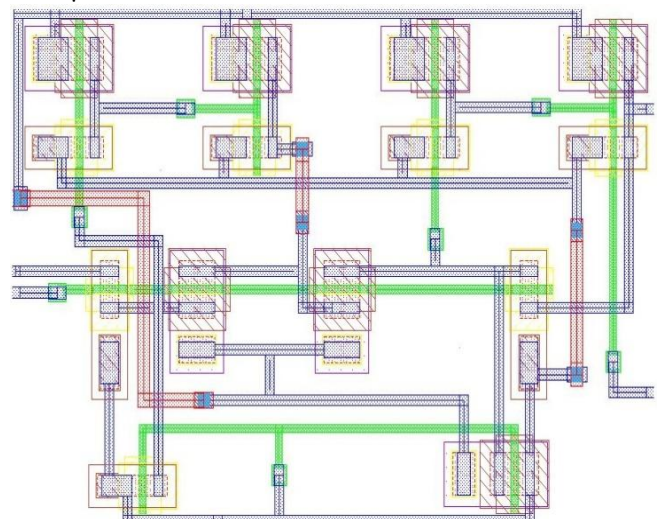


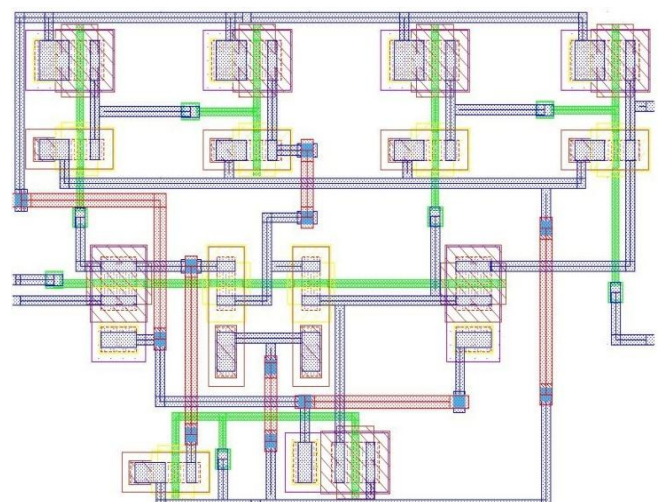**Fig.17 Layout of NPCDETFF**



**Fig.18 Layout of PPCDETFF**

The proposed design for NPCDETFF and PPCDETFF are simulated in 18nm Fin-FET technology. The simulation were applied to 18nm Fin-FET with $V_{DD}$ of 0.38V at $25^0$C and frequency for input clock signal is 500MHz.

Simulation results for above mention values on both proposed DET flip flops are shown in Table III.

**Table III Simulation Results**

|  | Power (nW) | Delay (ps) | PDP (aJ) | No. of Transistors |
|---|---|---|---|---|
| NPCDETFF | 86.78 | 46.3 | 4.017 | 14 |
| PPCDETFF | 7.04 | 390.5 | 2.749 | 14 |

Proposed DET flip flops are tested in full exhaustive method so we can check its max power at full clock use. Fin-FET is the latest method in VLSI design which requires different aspect in circuit designing then CMOS technology. Fin-FET is a double gate MOSFET. Transient analysis of proposed NPCDETFF and PPCDETFF design in 18nm Fin-FET technology is shown in Fig.19 & Fig.20 respectively.
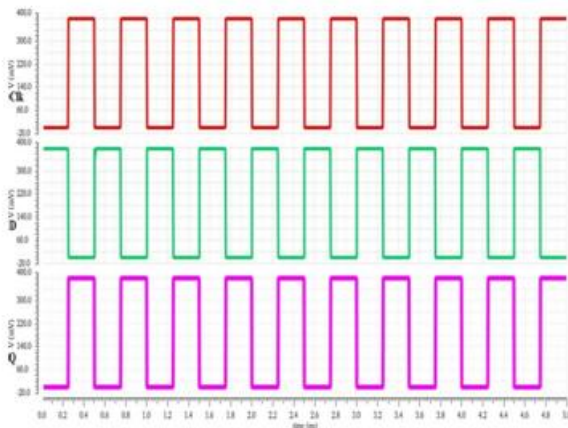


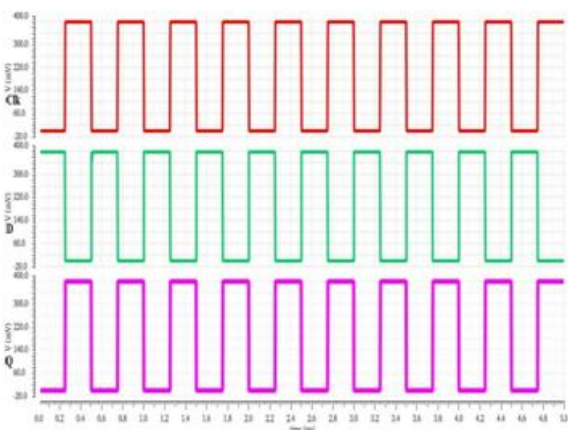**Fig.19 Transient analysis of NPCDETFF**



**Fig.20 Transient analysis of PPCDETFF**

Variation of power and delay with variation in frequency of input clock signal is shown in Fig.21 and Fig.22 respectively.
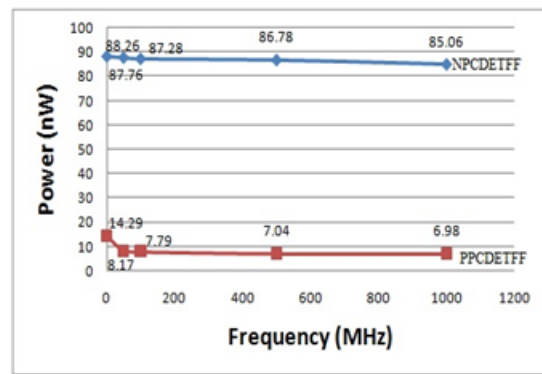


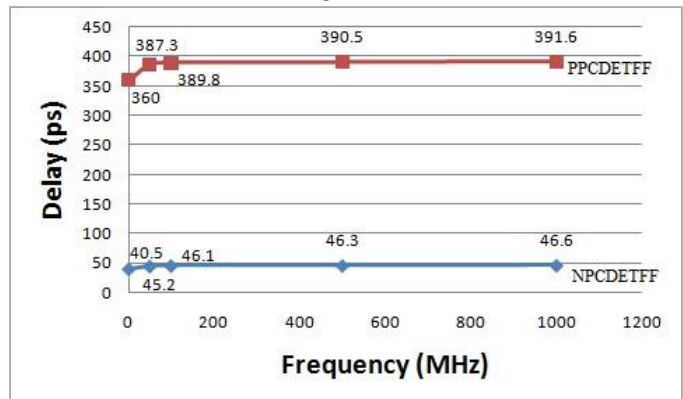**Fig.19 Power at different frequencies for NPCDETFF & PPCDETFF**



**Fig.20 Delay at different frequencies for NPCDETFF & PPCDETFF**

## V.    CONCLUSION

The proposed design for DET flip flop as NPCDETFF and PPCDETFF are very efficient from the compared DET flip flops. It reduces all major parameters of a VLSI design like area, power and delay from the compared DET flip flop. In between proposed DET flip flops NPCDETFF has low delay as compare to PPCDETFF and PPCDETFF has low power consumption as compare to NPCDETFF. Both have an edge over each other at some particular aspect with some tradeoff to another aspect of parameter. The main positive thing of the proposed DET flip flop is lowest transistor count compared to existing DET flip flops. In 180nm CMOS technology this designed DET flip flop NPCDETFF and PPCDETFF are proved better then compared DET flip flip as they reduces transistor count by 23% and PDP by 99%. In 45nm CMOS technology as well designed DET flip flop NPCDETFF and PPCDETFF are proved better then compared DET flip flop as they reduces transistor count by 37% and PDP by 18%. In 18nm Fin-FET technology designed DET flip flops NPCDETFF and PPCDETFF are test in full utilization of clock signal so it can give the max power consumption of designed DET flip flop at full scale operation.

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