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Dynamic Power Optimization of 32 Bit MIPS Processor using Clock Gating for Low Power Applications

V.Prasanth, K.Babulu, M.Kamaraju

Abstract*: The demand for low power processor is increasing day by day in mobile application for video, audio, mixed signal processing, gaming console and battery-operated electronic devices. Power consumption is the main issue in batter operated devices which constantly reduces battery life. Compared to static power Dynamic power yields more power consumption in digital design. Clock power is one of the major factors in total power consumption which results in high dynamic power consumption. In this paper, a 32-bit MIPS processor is designed to maximize the performance while considering the battery life of the device. Clock gating and data gating method is adopted in this paper and to reduce dynamic power. This design is implemented on 28nm kintex-7 FPGA Board and power is analyzed

Index Terms*: MIPS, power consumption, dynamic power, clock gating, switching activity.

I. INTRODUCTION

MIPS architecture is the most efficient RISC architecture which delivers best performance with low power consumption in a given silicon area. MIPS is one of the three CPU architectures which provide great support to Android base devices, linux and RTOS, it is best rated among google android devices. MIPS is generally designed for high performance application with low power consumption. Electronic devices with high performance release a large amount of heat which is a practical limitation to enhance the performance of system. Designers need to consider the factors which influence the system performance and also should consider time to market. FPGA devices are the best solution for better time to market because of re-programmability feature in FPGA.

In recent year, number of researchers are implementing various microprocessors using FPGA with high performance, low power and cost for portable devices. In digital design speed of the processor is major concern to improve performance of the device and as speed is inversely proportional to power so trade-off is required between speed and power. As the design size increases switching activity in MIPS processor will result in more dynamic power. With the scaling of technology, power-density is increased. In CMOS technology the real challenge is to scale voltage and frequency beyond 65nm, because with decrease in nano meter technology results in higher dynamic and leakage current density with minimal improvement in speed. In Modern design both in logic and memory static and dynamic power is increasing drastically. Clock power is the dominant power which consumes 50-60 percent of total power and it increases significantly with improvements to the next generation of designs at 90nm and below [6]. As a fact that power is directly proportional to voltage (V) and the frequency of the clock(F) as shown in the following equation

$$P = CV^2f$$

Clock gating is most effective method for reducing dynamic power by limiting switching which saves clock power[2]. Clock gating is generally implemented at gate-level synthesis tool. The main challenge in chip design for optimizing power is to know where and when to insert clock gating.

II. MIPS ARCHITECTURE

The MIPS architecture is created from research on efficient processor organization and VLSI integration at Standford University; it is designed with five stage execution pipeline and cache controller on a single silicon chip. MIPS architecture has five stages: fetch, decode, execute, memory-access, write back.

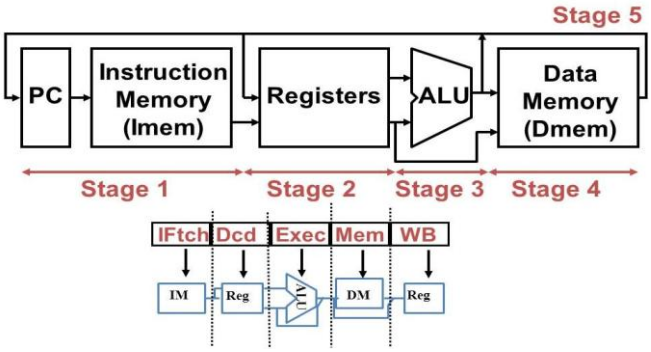

Fig 1: MIPS five-stage

The key concepts of MIPS architecture are

- Five-Stage Execution
- 32 bit instruction set
- 3 operand logic and arithmetical instruction
- Thirty-two, 32 bit

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* Correspondence Author
V.Prasanth*, Ph.D Scholar, Jawaharlal Nehru technological University, Kakinada, Andhra Pradesh, India.
K.Babulu, Professor of ECE, Jawaharlal Nehru technological University/ Kakinada, Andhra Pradesh, India
M.Kamaraju,Professor, Electronics and communication Engineering Gudlavalleru Engineering College, Gudlavalleru, Andhra Pradesh, India.

general purpose register

- Only load and store instruction access memory

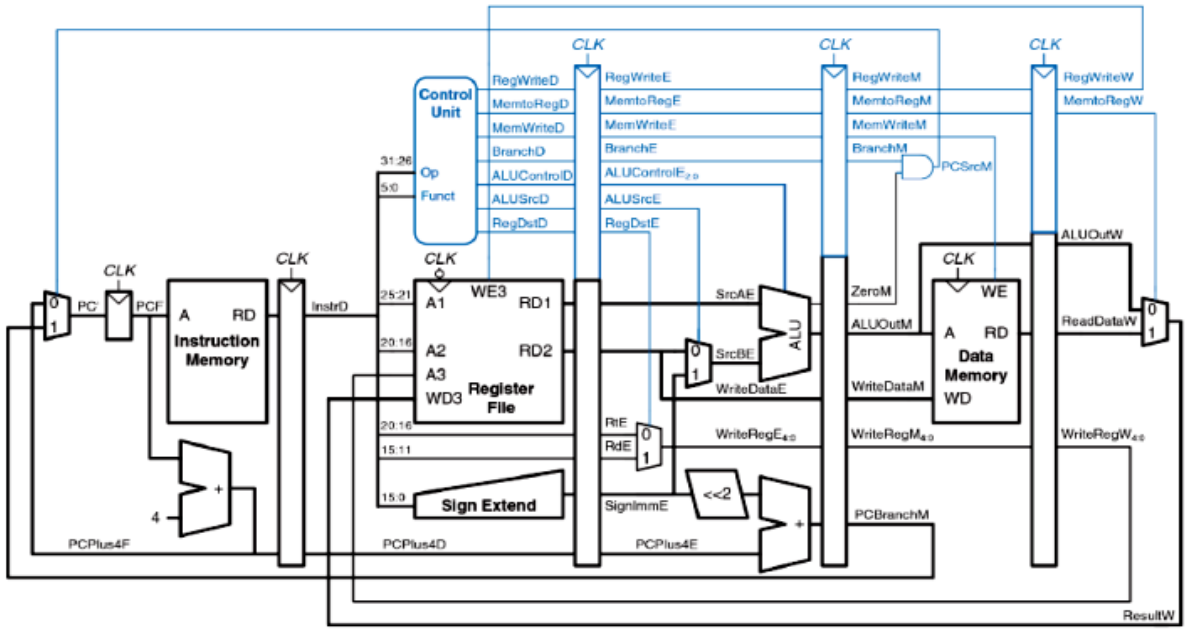


Fig 2: Architecture of Multi cycle 5-stage pipelined MIPS Processor

In five-stage pipelining, first stage is INSTRUCTION FETCH, from instruction memory next instruction is loaded to FE/DE register. DECODE is the second stage which decodes instruction fetched from instruction memory to be processed in place in data registers[1]. Immediate value is used with sign extension or zero filled. The stage that controls the signals for running the instruction are write to memory and register file and signal select foe multiplexer and ALU operations are generated[9]. In EXECUTE stage, Data extracted from previous the desired operation is performed. In MEMORY stage based on the instruction, either value is written into memory location or contents on memory location is read. WRITE BACK stage writes computed value in to register file[4].

MIPS pipelined architecture is used to reduce the power consumption as number of clock cycles required for processing 5 stages will be reduced. In conventional method, when more number of instruction are executed number of clock cycles will increase drastically resulting in clock power. To execute 5 instruction 20 clock cycles are required but using pipelining only 9 clock cycles required resulting 50% less power consumption.

Instruc. No.	Pipeline Stage								
1	IF	ID	EX	ME	WB				
2		IF	ID	EX	ME	WB			
3			IF	ID	EX	ME	WB		
4				IF	ID	EX	ME	WB	
5					IF	ID	EX	ME	WB
Clk Cycle	1	2	3	4	5	6	7	8	9

Fig 3: Stage pipeline structure

In pipelining at datapath, when instruction is the end of write back stage and if FE/DE already contains the

instruction of destination register of successive register and to avoid load the wrong data to register, during various execution steps of load instruction of destination register is transferred from FE/DE to DE/EX, to EX/ME and lastly to ME/WB to tbe used to address correct register at write back

III. MIPS INSTRUCTION SET

MIPS(Microprocessor without interlocked pipeline stages) is a load-store architecture which performs only arithmetic and logic operations between CPU registers, requiring load store instruction to access memory[3]. Since 1985 there is lot of research on MIPS and introduced different instruction sets namely MIPS I, MIPS II, MIPS III, MIPS IV, MIPS V and present version is MIPS V which is used for 64 bit design and with each revision architecture redefines with superset and improved its contribution towards embedded markets which is 3rd largest market in electronic industry. MIPS VI is used in the design with minimal instructions in Arithmetic, Logic, Data transfer, conditional branch and unconditional jump. The instruction format is as below

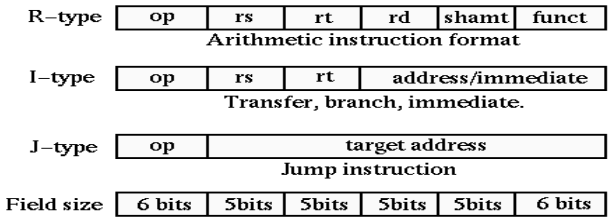


Fig 4: MIPS Instruction format

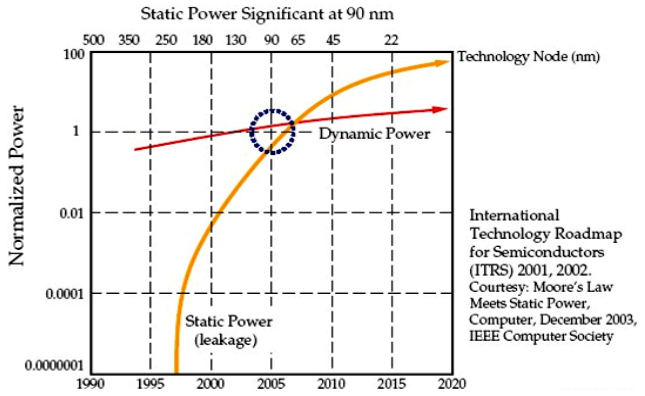
The 3 types of Instruction format used in MIPS processor are Register-Type, Immediate-type and jump-type.

IV. DYNAMIC POWER REDUCTION TECHNIQUES

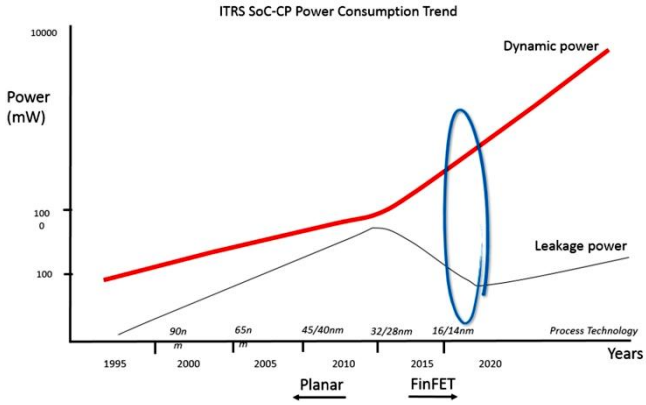
Power is the major concern in CMOS digital designs and many power reductions techniques are used in the system design reduce power consumption.

There three major types of power consumption a) Dynamic power consumption b) static power consumption c) leakage power consumption. But for larger designs with higher frequency and switching activity the static power and leakage power is very small whereas dynamic power increases drastically [2]. To obtain power-performance trade-offs different voltage domain are considered CMOS VLSI systems.. Significant increase in dynamic resulted with higher voltages when speed factor is improved (1/2 C V^2f). As power is directly proportional to square of the voltage, appropriate choice of voltage levels will yield less dynamic power consumption.

Activity in the design is main cause of dynamic power. The design with more work ends up needing more energy. To improve the speed of the design clock frequency is increased thus power required for design increases. dynamic power can be saved , either by slowing down the design (reduce clock speeds), reducing the voltages, or minimizing the switching activity in the design.



As per the ITRS prediction for 180nm dynamic power consumption amounts to 90% on total power and with increase in technology the static power also high comparable to dynamic power consumption.



As designs migrated to FinFET technology, compared to static power dynamic power became more concerned factor for the designers with high activity designs.

So to reduce the Dynamic power RTL designers has to change their designs to coarse-grained (micro-architectural) level. Designer can employ clock gating, instead of register ca use buffered network, gate memories and perform retiming,. These techniques cut down dynamic power significantly.

The methods employed to reduce dynamic power gating are Guarded Evaluation, pre-computation, operand isolation, operation reduction, pipelining and parallelism, register re-timing, Gated clock FSM, Clock gating, FSM Encoding, FSM Partitioning, Multi supply voltage design, bus encoding, dynamic voltage and Frequency scaling.

The most prominent and successful method to reduce dynamic power is clock gating as clock power is the dominant power in total dynamic power.

V. CLOCK GATING

In Low-power techniques Clock gating is very efficient in reducing the power consumption in CMOS digital circuits. This technique main goal is to cut-off transitions from propagating to parts of the clock path (i.e., flip-flops, clock network, and logic). The power savings can be achieved by reducing switching capacitance in the clock network during unnecessary transitions by disabling the clock. RTL clock gating groups flipflops which share a common enable control signal and disables then when no activity is present. Therefore, implementation of RTL clock gating can be achieved if common enable term is shared by bank of flip-flops, will result in zero consumption of dynamic power in flip-flops as long as this enable signal is inactive. The state transition from 0 to and 1 to 0 is main cause of dynamic power which results in more switching activity.

clock gating methods used in most design are:

1. Latch-free based design. (Gate based clock gating)
2. Latch-based design.
3. Intelligent clock gating optimizing option available in synthesis tool like Xilinx, Altera, Cadence,etc.
4. Synthesis based clock gating
5. Data driven clock gating
6. Auto gated clock gating
7. Look ahead based clock gating

LATCH-FREE BASED CLOCK GATING DESIGN

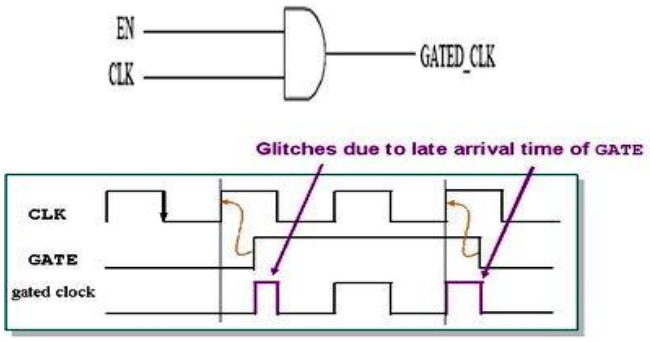


Fig 5: Latch-free based clock gating

The latch-free clock gating method uses a simple AND or OR gate, when enable signal goes inactive in between the clock pulse then gated clock output either can terminate prematurely[8]. The main disadvantage of this designs glitches arrive at frequent intervals which result in problem in test results.

LATCH-BASED CLOCK GATING DESIGN

a level-sensitive latch is added to the design in latch-based clock gating which holds the enable signal from active until clock signal is inactive[2] . The state of the enable signal is captured by latch and holds it till total cycle is completed[8]

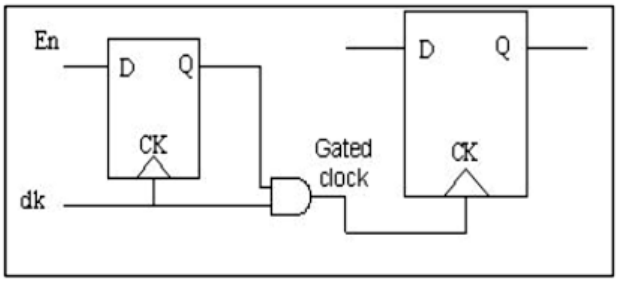


Fig 6:Latch-based clock gating

INTELLIGENT CLOCK GATING

Lately, in many industry like Cadence, Altera, Xilinx etc to optimize the power of the design intelligent clock gating option has been included in the design[7]. This option may not be helpful in power consumption and has to incorporate possible clock gating methods at RTL level to further reduce the dynamic power consumption of the circuit.

SYNTHESIS BASED CLOCK GATING

Synthesis-based clock gating method used by EDA tools which decreases clock pulse usage to reduce power consumption. For a particular functional block switching activity in the systems clock is redundant which as a result more power is consumed. To reduce the above redundancy problem in synthesis based clock gating, a method called data driven clock gating method was introduced [5]

DATA DRIVEN BASED CLOCK GATING

In this method design of flip-flop can be done without using latch, OR gate output is stored for a complete cycle which removes glitch problem[5]. Because of both latches are designed in D-FF are gated less power is consumed data drive flip flop when comparing with AGFF. By XOR'ing Flip flop present input and output of flip flop the output is present at next cycle. To avoid glitches outputs of k XOR gates are ORed to generate a combined gating signal for k FFs and they are latched together. AND gate combined with latch is called Integrated Clock Gate (ICG)[5]. Ultra low power design this data driven gating is used to reduce the area.

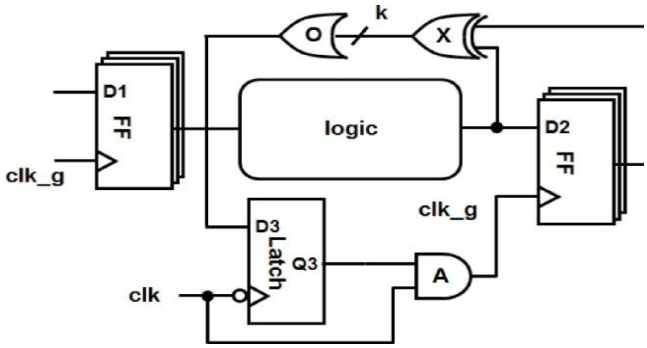


Fig 7: Data driven based clock gating

AUTOGATED CLOCK GATING

In Auto gated flip-flop master latch becomes active for falling edge of the clock and before arrival of rising edge the output. XOR gate determines, whether state should ne changed are remain same in slave latch when the master latch becomes transparent. Clock pulse will either stopped a passed when slave latch remain in same state.

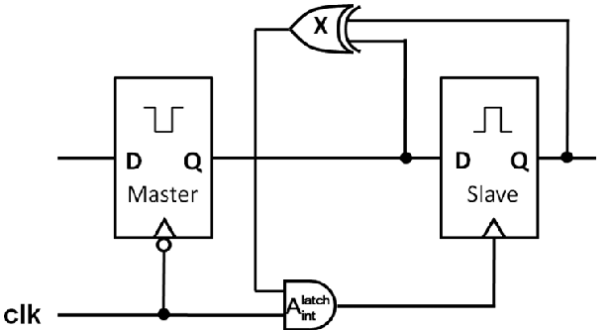


Fig 8: Automated clock gating

LOOKAHEAD BASED CLOCK GATING

Look Ahead Clock Gating (LACG) computes FF one cycle ahead of time by enabling clock signals, taking data of those FFs for which it depends. Compared to AGFF and data-driven it avoids the tight timing constraints of by enabling signals for full clock cycle for the data driven gating optimization requires the acknowledgement of flip-flops data toggling vectors in the functional block, whereas LACG is independent of those FFs knowledge[5]. clock switching power is very less in LACG when compared to other techniques.

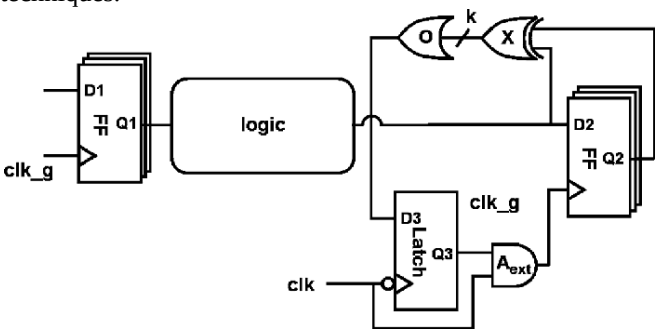


Fig 9: Look ahead based clock gating

VI. IMPLEMENTATION AND RESULTS

Pipelines MIPS 32 bit processor is designed using verilog HDL on Kintex-7 FPGA which 28nm technology. The design is synthesized and simulated on VIVADO HDL. MIPS 32 is designed and implemented with 500MHz clock speed which resulted in 109mw power. Latch free based clock gating is implemented on MIPS32 design by connecting gated clocks to all Flip-Flops in the design resulted in 20% power reduction to total dynamic power i.e. 89mw power. The designed is further improved with latch based clock gating with adding the concept of data driven clock gating XOR'ing all flip flops with present input to flip output to the design resulted in 50% of less dynamic power consumption to overall dynamic power i.e 52mw . The design is optimized with using the optimization tool in VIVADO HDL where more than 90% of flip-flop and registers are gated when activity of design is not useful.

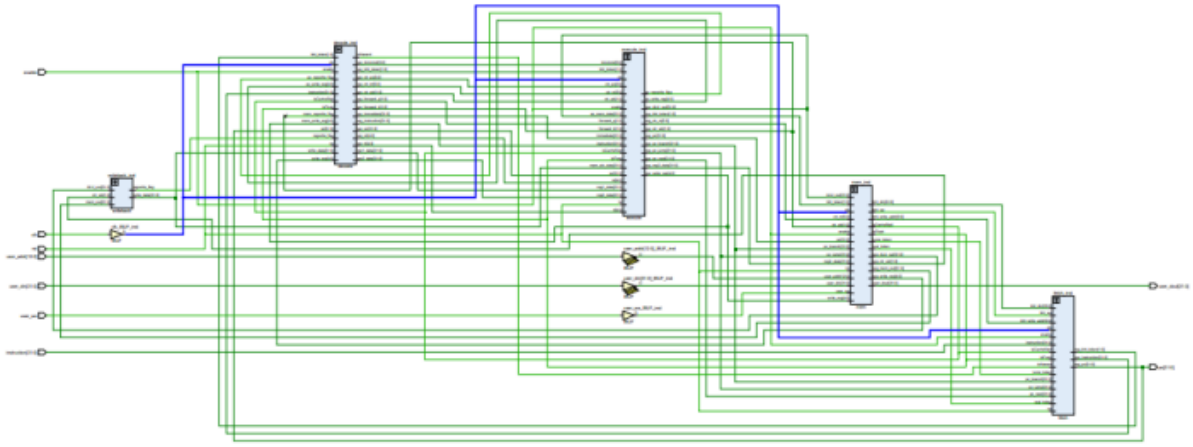


Fig 10: RTL Schematic of 5 stage pipelined MIPS 32 processor using clock gating

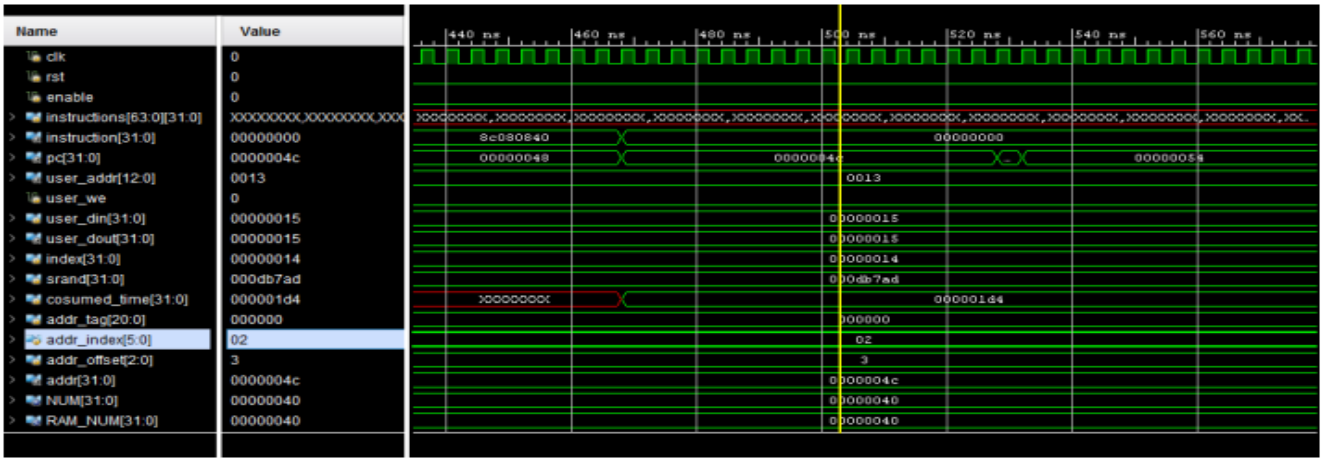


Fig 11: Simulation Result of 32 bit MIPS processor

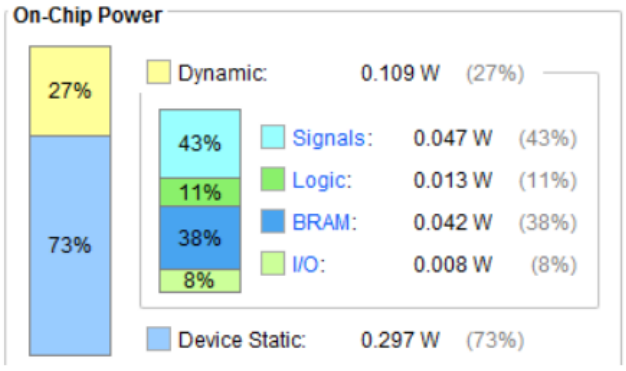


Fig 12: Power consumption of MIPS 32 architecture

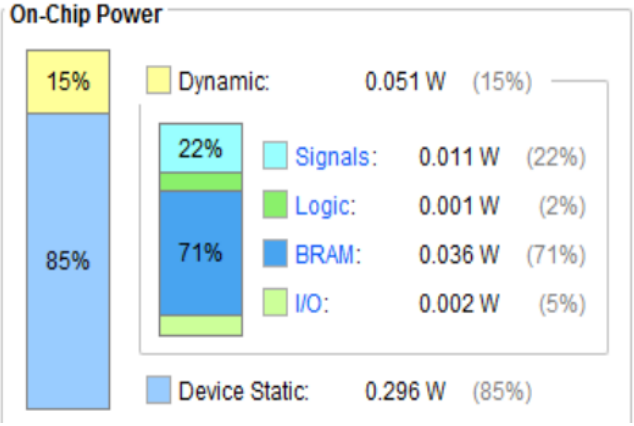


Fig 13: Power consumption of MIPS 32 architecture using latch based data driven clock gating

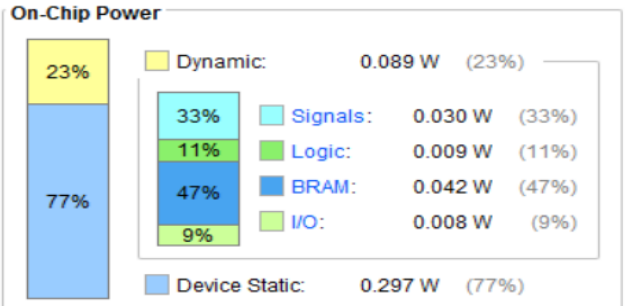


Fig 12: Power consumption of MIPS 32 architecture using latch free clock gating

Table 1: Power comparison on MIPS 32 bit Processor

Method used	Power consumption	100MHz	200MHz	500MHz	1GHz
MIPS 32 without clock gating	Total power(mw)	313	338	405	485
	Static power(mw)	296	296	296	297
	Dynamic Power(mw)	17	42	109	188
MIPS 32 with clock gating	Total power(mw)	311	330	385	452
	Static power(mw)	296	296	296	297
	Dynamic Power(mw)	15	34	89	155
MIPS 32 with clock gating and data gating	Total power(mw)	309	321	348	396
	Static power(mw)	296	297	297	298
	Dynamic Power(mw)	13	24	51	98

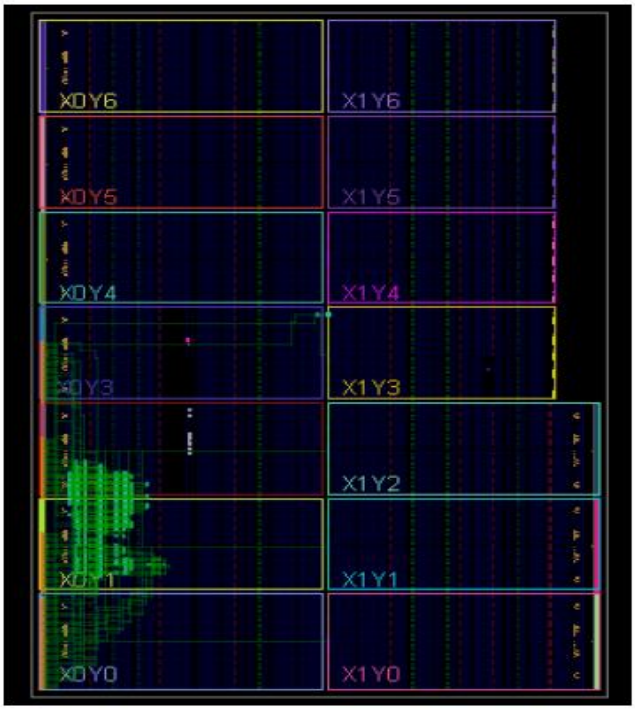


Fig 14: Implemented design on FPGA

VII. CONCLUSION

We have implemented and presented in-depth analysis on 32 bit MIPS processor and power is analyzed. Clock is the major constraint in power consumption and to reduce the usage of clock, enable signal is used. We implemented the conventional clock gating method ANDing clock and enable signal. The result shows a small amount of dynamic power is reduced using this method. But this method has glitch problem which may affect design performance. The same design is implemented with latch based data driven clock gating resulted in 51% of power reduction to dynamic power 15% power reduction to total chip power. In future work the design can be further implemented with look ahead based clock gating which better compared to other techniques.

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AUTHORS PROFILE

V.PRASANTH is an Associate professor of Electronics and communication engineering in Pragati Engineering College, Andhra Pradesh, India. He has 14 year of Teaching Experience. He is a Ph.D Scholar of JNTUK, Kakinada, Andhra Pradesh, India. He completed Masters in VLSI System Design. His area of Interest is Low power VLSI and Embedded Systems. He published total of 14 Papers.

K.BABULU has obtained graduation from GITAM Engineering College, Visakhapatnam affiliated to Andhra University in the Department of Electronics and Communication Engineering and Masters Degree in Electronic Instrumentation from REC, Warangal, Andhra Pradesh. He did Doctoral Degree in the field of VLSI & Embedded Systems from JNT University, Anantapur. He is currently working as professor in Department of ECE, University college of Engineering, JNTU Kakinada. He has published more than 32 research papers in reputed national and international Journals. He shared his research experience on about 45 national and international conferences, workshops, seminars and symposia. His total teaching and Research experience is 25 years. His interested areas are VLSI & Embedded systems.

M. KAMARAJU has obtained B.E. (ECE) and ME (EI) from Andhra University, Ph.D. (Low Power VLSI Design) from JNTUH, Hyderabad. He has an experience of 25 years in the field of teaching, and research experience of 5 years in the field of VLSI design. He has been published 112 Research/technical papers in various journals: National and International, and participated in national and international conferences. Editorial board member of International Journal of VLSI Design and Communication Systems (IJVLSICS) and Reviewer for number of International Journals and various IEEE international conferences organized outside INDIA. JNTUK, Kakinada awarded "Certificate of Appreciation" towards teaching methodologies. His Professional Memberships are FIETE, FIE and LISTE, also MVSI and Member of IEEE.