Asic Implementation of 12-Bit Radix-8 Booth Multiplier

U.Geetalakshmi, M.V.Nageswara Rao

Abstract: Multipliers are playing a vital role in DSP and Neural Networks applications. Many methods have been introduced to work on multipliers that offer high speed, less power consumption and reduced area. Booth Algorithm demonstrates an efficient way of signed binary multiplication. In this paper, physical design of 12-bit radix-8 booth multiplier for signed multiplication is presented with an aim to improve the performance metrics such as power, area and delay. The performance of 12-bit radix-8 booth multiplier is compared with the 64-bit radix-16 booth multiplier.

Index Terms: modified booth re-coding, partial products, radix-8.

I. INTRODUCTION

Binary multiplier is a combinational logic circuit to perform multiplication of two binary numbers. The two binary numbers are more explicitly known as multiplicand and multiplier and the outcome is known as a product. The multiplicand and multiplier can be available in variety of bit sizes. The number of bits required to represent product can be estimated depending on the bit sizes required for the multiplicand and multiplier. The addition of the bit sizes of multiplicand and multiplier is equal to the total bit size of the product. Binary multiplication involves following steps:

1. Re-coding of the bits in a multiplier within a particular number configuration.
2. The multiplication of every bit in a multiplier can be multiplied with the multiplicand, producing no. of products.
3. Reduce the partial product range using multi operand accumulation technique.
4. The two operands can be added by using carry propagate adder to get the ultimate result.

Elisardo Antelo et.al suggested the methods to improve the above and to achieve reduction in area, delay, power consumption and MBE multipliers. Recoding method is used to determine the no. of partial products. The re-coding process recodes binary information into signed bit information. The partial products generated for conversion modified booth encoding is n/2+1 instead of n/2. Addition of extra 1bit at the LSB of partial product. This leads to unequal partial product array. In radix-q (q=2m) the binary operand is collected of unnecessary radix-q digits. Radix-4 is a commonly used modified booth re-coding method that recodes operands into set {-2,-1, 0, 1, 2}. This is a widely used re-coding because it requires simple shifts and complementation to get partial products. Higher radix booth re-coding is not widely used. Since in higher radix, multiplicand need odd multiples which can’t be obtained by easy shifts and complementation and thus it requires carry propagate additions [1].

II. MODIFIED BOOTH MULTIPLIER

The modified booth encoding is a method used for decreasing the no. of partial products. Consider the multiplication of two’s complement representation of N-bit numbers of A and B

$$A = -a_{N-1} + \sum_{j=1}^{N-1} a_{N-j-1} 2^{-j}$$

$$B = -b_{N-1} + \sum_{j=1}^{N-1} b_{N-j-1} 2^{-j}$$

(1)

For modified booth encoding zero must be padded at the LSB side of B and N must be even. Kyung-Ju Cho et al. suggested the modified booth encoding, B can be defined as [2, 3],

$$B = \sum_{j=0}^{N/2-1} b_{N/2-1-j} 2^{-(2j+1)}$$

(2)

$$b_j = -2b_{2j+1} + b_{2j} + b_{2j-1}$$

(3)

By modified booth encoding those re-coded bits are grouped into triplets. Table 1 shows the Modified Booth Encoding operation refers to (3).

F. Lamberti et al. suggested the below Table 1 shows the Modified Booth Encoding for commonly used radix-4 booth multiplier [4]. The 2A in top table represents left shift of A by one bit. For negative function every A bit is complemented and add additional “1” bit binary value to the LSB bit of subsequent partial product row. Jiun-Ping Wang et.al suggested an additional “1” bit can be taken as correction bit cor, it describes pp, partial product row is positive when cor= zero and is negative when cor=one. Each partial product row pp, can be represented in its two’s complement form so that the sign bit of pp, have to be extensive to (2n-1) th bit location [5].

<table>
<thead>
<tr>
<th>b_{2j+1}</th>
<th>b_{2j}</th>
<th>b_{2j-1}</th>
<th>b_1</th>
<th>Asol</th>
<th>2Asol</th>
<th>NEG</th>
<th>cor</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0</td>
<td>0 0 0</td>
<td>0 0 0</td>
<td>0 0 0</td>
<td>0 0 0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 0 1</td>
<td>+A 1 0</td>
<td>0 0 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 1 0</td>
<td>+A 1 0</td>
<td>0 0 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 1 1</td>
<td>+2A 0 1</td>
<td>0 0 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 0 0</td>
<td>+2A 0 1</td>
<td>1 1 1</td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 0 1</td>
<td>-A 0 1</td>
<td>0 1 1</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>1 1 0</td>
<td>-A 1 0</td>
<td>1 1 1</td>
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<tr>
<td>1 1 1</td>
<td>-0 0 1</td>
<td>0 1 0</td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

Table 1: Modified Booth Encoding Table for radix-4[3]

Fig.1 below represents the grouping of bits for commonly used radix-4 for N=8. Zero must be padded at the right side of
the multiplier operand. The 1st group of recoding digit is formed by padded bit and the remaining 2 bits are the 2 Least Significant Bits of the multiplier. The second group of recoding digit is formed by taking the starting bit as the MSB of 1st group and remaining 2 bits in LSB of multiplier.

For generation of error compensation, LP can be further separated into LPmajor, LPminor [8,9]. Fig.3 shows the partial products of modified 8x8 booth multiplier with sign extension methods. \( P_i \) denotes the jth bit of the partial product \( pp_i \) and \( s_j \) denotes the sign bit of partial product \( pp_i \).

### III. Radix-8 Booth Algorithm

In this Radix-8, the multiplier(y) bits can be grouped into 4-bits in use at a time. Zero must be padded at right side of the multiplier operand. The 1st group of recoding digit is formed by padded bit and the remaining 3 bits are the 3 Least Significant bits of multiplier. The second group of recoding digit is formed by taking the starting bit as the MSB of 1st group and remaining 3 bits of Least Significant bits of multiplier. Below Fig.4 shows the grouping of bits for \( N=12 \) in Radix-8 booth multiplier. The Radix-8 algorithm generates the partial products are n/8. Consider multiplicand as \( x \). Below Table 2 shows Modified booth encoding table for radix-8.

![Fig.4 Grouping of multiplier bits for N=12](image)

### IV. Full-Width Multiplier

Full width multiplier multiplies 2 N-bits of operand and gives N-bits of partial product. These multipliers are used to remove the one fraction of partial product array, to decrease the economy and make use of rectification functions. Here fixed width multipliers were taken to decrease the errors during multiplication. The Fig.5 shows the Partial product for modified 12x12 booth multiplication. Which implies, the operation can be performed with 12 bits of multiplicand and 12 bits of multiplier which produces 12 bit partial product. The result of this multiplication depends on the fixed width multiplier so that it gives 12-bit output. Truncation takes place at the MSB side produces 12-bit product. Fig.6 below shows the addition of partial products in 12-bit Radix-8 Booth Multiplication. Multiplier bit can be grouped into four digits and it generates one recoded bits.
This process continues all the multiplier bits can be grouped. In radix-8 for N=12 produces four recoded bits which are b0’, b1’, b2’, b3’. Multiply the multiplicand with these four recoded bits gives products. Wen-Quan He et al. suggested those partial products are added with the help of half adders (HA) and full adders (FA) and the carry of HA and FA will be propagated to next levels. All the sum and carry terms are added by the Vector Matrix Array (VMA). VMA is used to add all the values which are in the vector notation. The VMA generates partial products from P0 to P17. Final result will come after the truncation [10].

V. RESULTS AND DISCUSSION

The 12-bit Radix-8 Booth Multiplier is simulated and verified the results. The code for modified 12-bit Radix-8 booth multiplier is simulated using Cadence NC Launch tool. NC launch is a tool which helps to simulate the verilog and VHDL codes. Fig.7 refers to the simulation result for modified 12-bit Radix-8 Booth Multiplier. A radix-8 booth multiplier is elaborated, synthesized and verified in cadence tool. The technology library used is gpdk090 (90nm) synthesis of RTL design gives report on area, power and timing analysis. Physical verification gives the floor plan, placement and routing details.

A. Simulation Results

For checking the operation of booth multiplier, we implement a test bench. Here we gave different series of inputs to the Booth Multiplier which produces the output.
(CLA) etc, Vector Matrix Array (VMA) etc. and also the power consumption by every cell in the multiplier.

The area report consists of some parameters like Cells, Cell Area, Net Area and Total Area. Area report will give the summary of the area of the each cell in the current multiplier. And also this area report gives no. of gates and area sizes based on the specified technology library.

Timing analysis or Delay report consists of Fanout, load (LF), Slew rate(ps), Delay time (ps), arrival time (ps) as per the hierarchy given in the code. Arrival time contains rise time data. This report will give the slew rate and, delay time and arrival time of each cell of the multiplier. Below Table 3 gives the comparison table of the power, area and delay report of Radix-8 booth multiplier with Radix-16 booth multiplier in 90nm technology.

Table 3: Comparison table for Power, Area and Delay in 90nm technology

<table>
<thead>
<tr>
<th>S. No.</th>
<th>Parameters</th>
<th>64-bit Radix-16 Booth multiplier</th>
<th>12-bit Radix-8 Booth multiplier</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. No. of bits</td>
<td>64-bits</td>
<td>12-bits</td>
<td></td>
</tr>
<tr>
<td>2. Power</td>
<td>672000mW</td>
<td>124924mW</td>
<td></td>
</tr>
<tr>
<td>3. Area</td>
<td>42000 mm²</td>
<td>2500 mm²</td>
<td></td>
</tr>
<tr>
<td>4. Delay</td>
<td>967.5 ps</td>
<td>690.2 ps</td>
<td></td>
</tr>
</tbody>
</table>

C. Layout

The automated layout is generated by the Cadence SoC Encounter which contains the constraints like import design, Floor plan, placement and routing and netlist of the multiplier is generated in pre-layout steps. The final layout is generated after performing the routing is shown in below Fig.10.

![Fig.10 Layout of the Radix-8 Booth Multiplier using Cadence SoC Encounter](image)

VI. CONCLUSION

The 12-bit Radix-8 Booth Multiplier is implemented and its architecture is verified. Synthesis is performed using RTL compiler tool using slow and fast libraries. Results shows that 12-bit radix-8 booth multiplier needs less power, less area and less delay when compared with 64-bit radix-16 booth multiplier. Power consumed, area required and delay occurred by 12-bit radix-8 booth multiplier is 124924mW, 2500mm² and 690.2ps respectively. When compared with the 64-bit radix-16 booth multiplier the 12-bit radix-8 booth multiplier consumes less power by 5times , reduction in area by 18times and reduced delay by 0.7 times. Hence, 12-bit radix-8booth multiplier is suitable for applications such as DSP and Neural Networks.

REFERENCES


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