

# Design, Analysis and Implementation of a Novel Soft-Switched Bridgeless Interleaved Boost PFC Converter



Aishwarya. V, R. Seyezhai, Kaviya. R, Kavitha. C

**Abstract:** In the modern era, the electronic equipments are widely used and it is required to maintain the supply current harmonics within the standards specified by IEC. Efforts are taken to get better power factor of these supplies using Bridgeless Interleaved Boost Converter (IBC) topology. The efficiency and the power factor of the bridgeless converter is improved in contrast to the conventional PFC as the bridged structure is eliminated. Main objective of the paper is to propose a novel Zero Voltage Switched Bridgeless IBC. This bridgeless configuration is investigated by analyzing the attributes such as output power, mark-space ratio, source voltage, input current with each other. With zero-voltage switching, the voltage regulator can engage in soft switching, which helps to minimize switching losses and electromagnetic interference. This paper also compares performance parameters such as power factor, efficiency, THD and ripple with and without ZVS in a bridgeless IBC circuit. The results show that there is a considerable ripple reduction and power factor improvement with increase in efficiency on incorporating soft switching. Replication of the projected circuit is executed in simulation and the outputs are verified using hardware implementation.

**Index terms:** Bridgeless Interleaved Boost converter, Zero Voltage Switching (ZVS), Efficiency, PFC

## I. INTRODUCTION

The Bridgeless Interleaved Boost converter results in improved power factor and efficiency against the classical bridged Interleaved Boost converter. A detailed analysis of the projected novel IBC configuration has been carried out in [1]-[4]. With the increased demand for improving the efficiency of converters, various methods for reducing the losses in the converters have been analysed. By adopting resonant based switching techniques such as Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS), the switching loss of the converter is reduced drastically. During hard switching, the overlap that exists between the switch current and voltage leads to power losses.

However, this can be eliminated by adopting soft switching, where the power switch comes into conducting state only after the voltage reaches to zero (ZVS condition) and switched off after the current has decayed fully (ZCS condition). The application of ZVS and ZCS for the buck and boost converter has been explained in [5]-[7]. Analysis and implementation of ZVS for IBC is reported in [8]-[11]. Performance evaluation and hardware implementation of ZVS for Bridgeless IBC has been carried out. From the results, it is ascertained that the new projected IBC circuit results in increased efficiency, reduced output voltage and current ripple and improved power factor.

## II. PROPOSED ZVS BRIDGELESS IBC

Fig. 1 shows the drawing of the projected IBC configuration. The operation of the ZVS Bridgeless IBC is explained in two modes.

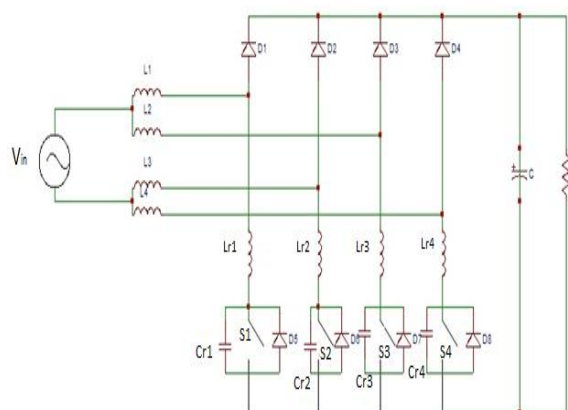


Fig. 1 Proposed ZVS Bridgeless IBC

**Mode 1:** Interval 1: In this positive half-cycle of interval, the switches  $S_1$  and  $S_2$  are forward biased resulting in the flow of current through  $L_1, L_{r1}, S_1, S_2, L_{r2}$  and  $L_2$ , returning to the line. The energy gets stored in the inductors. Inductors  $L_3$  and  $L_4$  is discharged, and current flows through  $L_3, D_3, C$ , body diode of  $S_4, L_4$  and then to the supply line. The resonant capacitor  $C_{r4}$  gets charged by this current. In the same mode of operation during interval 2, the switches  $S_3$  and  $S_4$  are conducting, with  $S_1$  and  $S_2$  in reverse biased condition.

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Therefore, the path of current flow is via  $L_3, L_{r3}, S_3, S_4, L_{r4}$  and  $L_4$ , and then goes back to the supply line. But inductors  $L_1$  and  $L_2$ , discharges when current flows through  $L_1, D_1, C$ , body diode of  $S_2, L_2$  and then to the supply line. The resonant capacitor  $C_{r2}$  gets charged by this current.

**Mode 2** :Interval 1: In this negative half-cycle of interval, the switches  $S_1$  and  $S_2$  are forward biased resulting in the flow of current through  $L_2, L_{r2}, S_2, S_1, L_{r1}$  and  $L_1$ , back to the supply line. Inductors  $L_3$  and  $L_4$ , is discharged when current flows through  $L_4, D_4, C$ , body diode of  $S_3, L_3$  and then to the supply line. The resonant capacitor  $C_{r3}$  gets charged by this current. In the same mode of operation during interval 2, the switches  $S_3$  and  $S_4$  are forward biased with  $S_1$  and  $S_2$  in reverse biased state resulting in the current flow through  $L_4, L_{r4}, S_4, S_3, L_{r3}$  and  $L_3$ , and then back to the supply line. Inductors  $L_1$  and  $L_2$ , discharges when current flows through  $L_2, D_2, C$ , body diode of  $S_1, L_1$  and then to the line. The resonant capacitor  $C_{r1}$  gets charged by this current. Resonance occurs due to resonant inductor and the resonant capacitor resulting in turning on of the main switch achieving ZVS/ZCS.

The conversion gain of the converter is given by

$$M = \frac{V_o}{V_{in}} \quad (1)$$

where,  $V_o$  represents the output voltage of the converter,  $V_{in}$  is the input voltage

The resonant frequency is given by

$$\omega_o = \frac{1}{\sqrt{L_r C_r}} \quad (2)$$

where,  $L_r$  represents the resonant inductance and  $C_r$  is the resonant capacitance

The ratio of resonant frequency  $f_r$  to the switching frequency  $f_s$  is  $f_{ns}$ .

$$f_{ns} = \frac{f_r}{f_s} \quad (3)$$

Q is given by,

$$Q = \frac{R_o}{\sqrt{L_r C_r}} \quad (4)$$

where,  $R_o$  is the load resistance

Finally, the value of the resonant capacitance and inductance is given by,

$$C_r = \frac{1}{(2\pi f_r)^2 \frac{R_o}{Q}} \quad (5)$$

$$L_r = C_r \left( \frac{R_o}{Q} \right)^2 \quad (6)$$

The expression for the inductor is specified as

$$L = \frac{V_{in} * D}{f_s * \Delta I} \quad (7)$$

where, D is the duty ratio and  $\Delta I$  is the output current ripple

The filter capacitor is expressed as

$$C = \frac{V_o * D}{R_o * f * \Delta V} \quad (8)$$

where,  $\Delta V$  is the output voltage ripple.

Using equations (1-8), the converter components are designed and the parameters are tabulated in Table 1.

**Table 1. Design values of ZVS Bridgeless IBC**

Parameter	Value
Input Voltage	24V
Duty Ratio	0.5
Switching Frequency	150kHz
Inductor	330uH
Capacitor	1000uF
Resonant Inductor	14uH
Resonant Capacitor	20nF

### A. Loss Calculation Of Ibc

The efficiency of the converter accounting the losses is expressed as

$$\eta = \frac{P_{out}}{P_{out} + P_{loss}} \quad (9)$$

where,  $P_{loss}$  is the power loss in the converter

The power losses of the proposed circuit are equal to the summation of inductor losses, switching losses and conduction losses of the main switch and freewheeling diode.

(i) Inductor loss

Power loss due to inductor is given by

$$P_{inductor} = R_o * \left( \frac{I_o}{1-D} \right)^2 \quad (10)$$

where,  $R_o$  is the equivalent resistance of the inductor,  $I_o$  is the output current and D is the duty ratio.

(ii) MOSFET loss

Loss in MOSFET is due to the sum of conduction loss and switching loss. In case of ZVS, the switching loss is zero.

$$P_{MOSFET} = P_{conduction} + P_{switching} \quad (11)$$

$$P_{conduction} = R_{on} * D * \left(\frac{I_{out}}{1-D}\right)^2 \tag{12}$$

$$P_{switching} = \frac{1}{2} * C_{oss} * V_{DS}^2 * f_s \tag{13}$$

where,  $R_{on}$  represents the on-state resistance of the device,  $I_{out}$  is the RMS value of output current,  $D$  is the duty cycle,  $C_{oss}$  is the output capacitance of the MOSFET,  $V_{DS}$  is the voltage across drain and source and  $f_s$  is the switching frequency.

(iii) Diode loss

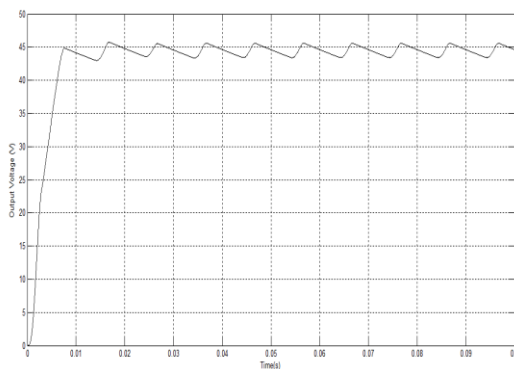
The power loss in the diode is given by

$$P_{diodes} = R_D * I_o^2 + V_F * I_o \tag{15}$$

where,  $R_D$  is the diode resistance and  $V_F$  represents the on-state voltage drop of the diode.

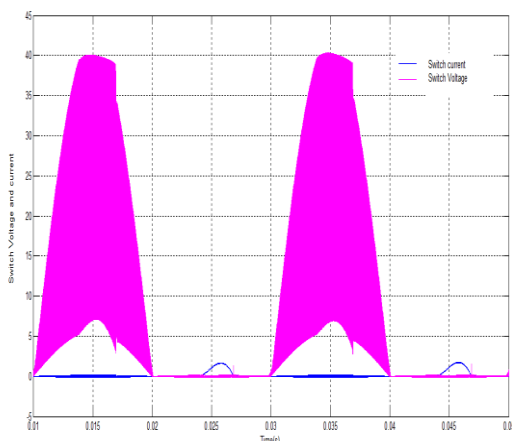
### III. SIMULATION RESULTS

The ZVS Bridgeless Interleaved Boost converter is studied in MATLAB/Simulink.



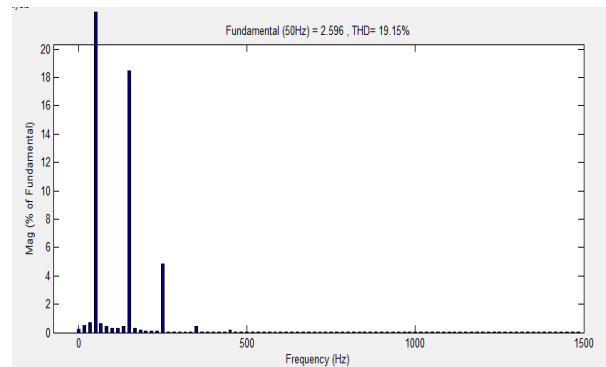
**Fig. 2 Output voltage waveform of bridgeless IBC with soft switching**

Fig.2 shows the output voltage waveform for bridgeless soft switched IBC. The output voltage obtained is 45V for the duty ratio of 0.5.



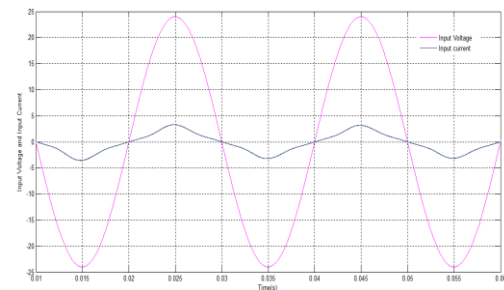
**Fig. 3 Switch voltage and current waveform of ZVS**

Fig. 3 shows the simulated zero voltage switching waveform and it can be observed that the switching occurs only when the voltage across the switch is zero.



**Fig. 4 THD of supply current**

Fig. 4 shows the FFT analysis of supply current of bridgeless IBC with ZVS. The THD obtained is 19.15%.

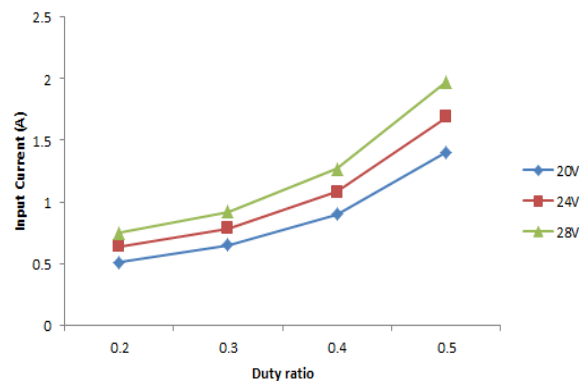


**Fig. 5 Input voltage and Input current waveform of bridgeless soft switched IBC**

Fig. 5 shows the input voltage and input current waveform for bridgeless interleaved boost converter with ZVS. It is observed that the supply current waveform is in phase with supply voltage with reduced harmonics.

#### (A) Analysis of Bridgeless IBC With ZVS

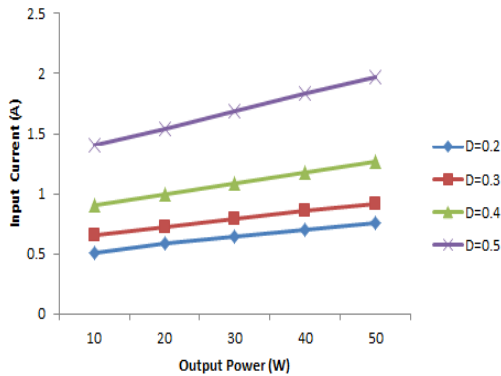
In this section, the ZVS Bridgeless Interleaved Boost converter has been analysed. The variation of parameters such as duty ratio, input current, input voltage, output power with each other has been analysed.



**Fig. 6 Input current versus Duty ratio**

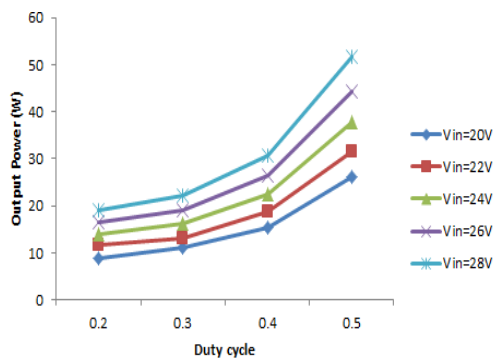
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Fig. 6 shows the input current versus duty ratio waveform of bridgeless interleaved boost converter with ZVS for various values of supply voltage. The input current varies linearly with duty ratio.



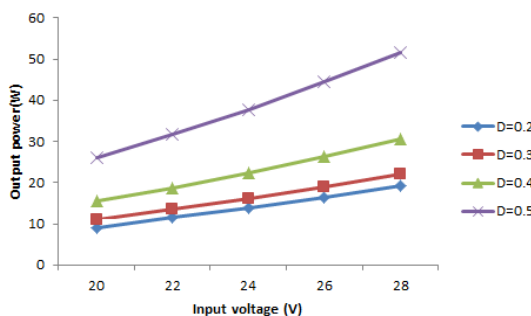
**Fig.7 Input current versus Output power**

Fig. 7 shows the input current versus output power waveform for bridgeless interleaved boost converter with ZVS for various mark space ratios. The output power increases with the increase in input current and the input current varies linearly with the rise in duty cycle.



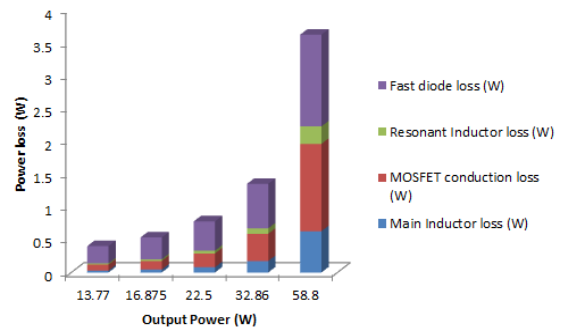
**Fig. 8 Output power versus Duty cycle**

Fig. 8 shows the output power versus duty cycle waveform for bridgeless interleaved boost converter with ZVS for various values of input voltage.



**Fig. 9 Output power versus Input voltage**

Fig.9 shows the output power versus input voltage waveform for bridgeless interleaved boost converter with ZVS for various duty cycles and it is a linear relationship.



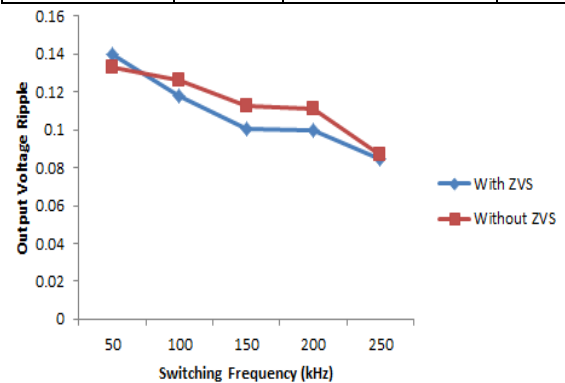
**Fig. 10 Computation of Power loss**

Fig. 10 shows the power losses for bridgeless interleaved boost converter with ZVS. This waveform shows that the sum of fast diode loss, resonant inductor loss, MOSFET conduction loss and main inductor loss gives the total power loss which increases with increase in output power.

## (B) Comparison of Performance Parameters

The parameters for the projected IBC topology is compared with the classical IBC without ZVS and the results are shown in Table 2.

Topology	THD %	Displacement factor	pf
Bridgeless IBC with ZVS	19.15	0.999	0.98
Bridgeless IBC without ZVS	31.33	0.98	



**Fig. 11 Output voltage ripple versus  $f_s$**

From Fig. 11, it can be observed that with increase in switching frequency, the output voltage ripple reduces. The ripple is also observed to be slightly reduced in the case of Bridgeless IBC with ZVS.



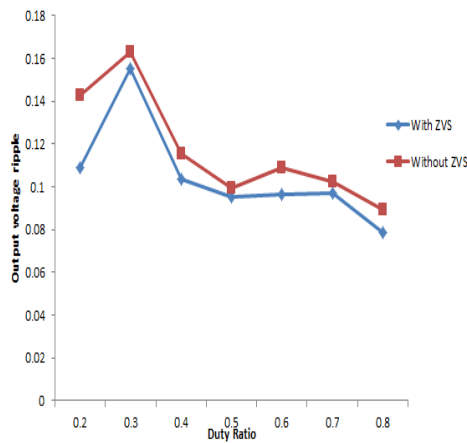


Fig.12 Output voltage ripple versus Duty ratio

Fig. 12 shows that the output voltage ripple of bridgeless IBC with ZVS is less compared to without ZVS for duty ratios ranging from 0.2 to 0.8.

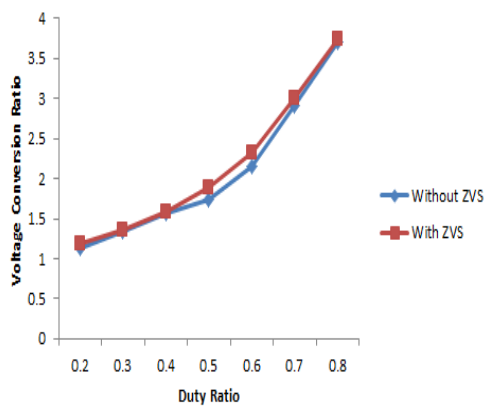


Fig. 13 Voltage gain versus Duty ratio

Fig. 13 shows that the gain of bridgeless IBC with ZVS is more than that without ZVS for various duty ratios.

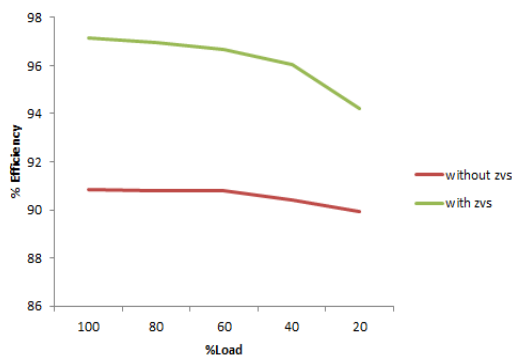


Fig. 14 Efficiency versus Percentage load

From Fig. 14, it can be inferred that % efficiency in bridgeless interleaved boost converter is greater with ZVS than that of bridgeless interleaved boost converter without ZVS for the same load.

#### IV. HARDWARE IMPLEMENTATION

A hardware prototype of the proposed ZVS bridgeless converter is constructed using power MOSFETs as switches and pulses are generated using Arduino board. The hardware model is shown in Fig.15. For an input of 6.5V, an output of

21.6V is obtained with resistive load. The simulation results are verified experimentally.



Fig.15 Hardware prototype of ZVS Bridgeless IBC

Hence, the proposed IBC configuration is a suitable and appropriate one for battery charging applications which is observed from the simulation and hardware results.

#### V. CONCLUSION

The bridgeless interleaved boost converter circuit was simulated with and without ZVS using MATLAB. Analysis of the output power, duty cycle, input voltage, input current with each other and power loss calculation has been carried out and comparison graphs have been plotted for these parameters. Performance parameters such as power factor, efficiency, THD and ripple with and without ZVS in a bridgeless IBC circuit has been compared. It was observed that there is a considerable ripple reduction, power factor improvement with the increase in efficiency on incorporating soft switching and the efficiency was found to be increasing with load. The results obtained from simulation are found to match with the hardware implementation.

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