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Low Voltage Full Swing Fin FET Hybrid Full Adder

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Abstract: ***In this research paper, CMOS and FinFET based hybrid Full Adders operating at low voltages with low power dissipation are proposed. The proposed CMOS based circuit is compared with few existing hybrid full adders in terms of average power dissipation and power-delay-product (PDP). The designed CMOS based hybrid adder achieves lower power dissipation and low PDP compared to other hybrid adders over a voltage range of 0.6V to 1V. The proposed CMOS implementation of hybrid full adder fails at 0.5V to produce full swing output. To solve this full swing problem, the proposed hybrid full adder is implemented using FinFETs which produce full output voltage, lower power and low PDP comparing with CMOS implementation. The circuits are designed with HSPICE tool in 32nm predictive technology model (PTM).***

Keywords: Delay, FinFET, Hybrid Full Adder (HFA), Conventional MOS (CMOS), Power-Delay-Product, Power Dissipation.

I. INTRODUCTION

Demand for smaller area, reduced power, and high operating speed is increasing in battery dependent portable devices like mobile phones, laptops, notebooks. Power consumption is the dominating challenge in battery operated devices [1-2]. Digital signal processing applications like Fast Fourier Transform, filters, signal, image, and video processing operations demand low power arithmetic units. Addition/subtraction is the most fundamental operation in arithmetic units [3-4]. Over the years researcher's key focus is on Full Adder design. Different logic design styles have been proposed, each having their own demerits and merits. Full Adder designs are classified into Dynamic style and Static style. Dynamic full adder design has an advantage of low delay, less static power consumption and full output voltage swing. Static full adder design has advantages of more reliability, simplicity and less energy requirement over dynamic design. But the chip area requirement for static full adder design is more. The major disadvantage of static type full adder is high power dissipation [5-6]. The primary sources of power dissipation are switching activity, node capacitances and transistor sizing. The power optimization can be achieved by reducing the size of transistors and operating voltage. The shrinkage of technology and scaling of operating voltage optimizes the power consumption of system which increases the delay, further effects the driving capabilities of system. Due to scaling high leakage currents and hot electron effects increase the power dissipation in conventional MOS transistors [7]. To further reduce the dissipation of power in circuits, FinFETs are remedy to conventional MOS(CMOS) Transistors. Based on output, full adder designs are classified into without full swing output and with full swing output. 8 Transistor, 9 Transistor and 10 Transistor full adders are of the first type without full swing output [8-12]. Conventional MOS (CMOS), Transmission Gate Full Adder (TGA), Transmission Function Full Adder (TFA), Complementary Pass Transistor Logic (CPL), 16 Transistor (16T) and 14 Transistor (14T) designs are of the type which produces full swing output voltage [13-17]. 28 Transistor Conventional CMOS full adder has flexibility in transistor sizing and scaling of supply voltage. The main disadvantage is large input capacitance and requirement of buffers. CPL consists of 32 transistors, has an advantage of good voltage swing [18]. The disadvantage is its high-power dissipation because of high switching activity at intermediate nodes. TFA design is consists of transmission gates which consumes less power. TGA design consists of transmission gates with 20 transistors overcome the voltage degradation problem of CPL [19]. The new way is to use more logic styles in design of full adder popularly known as Hybrid logic design. The performance of full adder can be enhanced by exploiting the features of different logic styles in hybrid logic design. Zhang et. al [20] proposed full adder with Hybrid pass logic with output CMOS driver (HPSC). The HPSC full adder produces full swing output by using XOR, XNOR modules designed by pass transistor modules with only six transistors and CMOS circuits at output. The major disadvantage of this design is increase in transistor requirement with less speed. Bhattacharyya [21] proposed a hybrid full adder with both Transmission gate logic and CMOS. This adder uses a modified XOR/XNOR module with a different arrangement which offers lower power and increase in speed.

It employs a carry generation module designed using transmission gates with

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less propagation delay. High performance hybrid full adder operatable at lower voltages was proposed with efficient modified internal logic by Kumar et al [22].

In this work, design of a new CMOS based hybrid full adder is proposed and the performance is compared with the existing hybrid full adder circuits concerning power dissipation, power-delay-product (PDP). This paper is organized as follows. The design of full adder circuits is presented in section 2. In section 3 the simulation environment used for testing is explained.

In section 4 and 5 the simulation results of proposed CMOS based and FinFET based full adder are presented. The conclusion of the work is given in Section 6.

II. DESIGN OF PROPOSED FULL ADDER

The circuit diagram of proposed full adder is shown in Fig. 1. It consists of 3 main blocks to generate sum and carry signals. The first block is XOR/XNOR block which produces the output signals (A⊙B) and (A⊕B). The second block is AND/OR block that produce outputs of A+B and A.B.
The third block is multiplexer which produces Sum and Carry signals. From full adder truth table, it is found that when C=0, Sum=(A⊕B) and when C=1, Sum=(A⊙B). Thus, by making use of multiplexer with input C the resultant output can be produced. In similar way, Carry=(A.B) when C=0 and when C=1, Carry=(A+B). C is used as input for the multiplexer to produce the desired output. Ref. [23] proposed an alternate logic to produce XOR/XNOR outputs making use of DPL logic and pass transistor logic to produce Sum output.

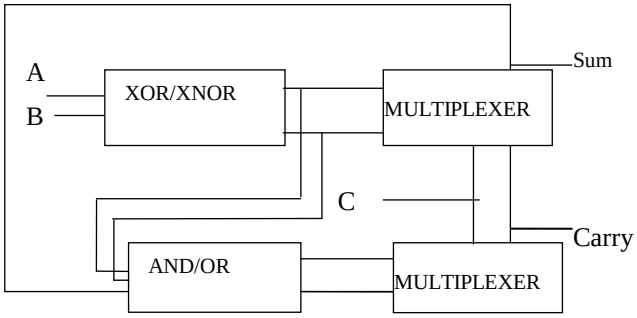

Figure 1: Logic scheme of full adder circuit design

A modified logic is proposed in this paper to produce AND and OR logic outputs. The full adder circuit with modified AND & OR logic is shown in Fig.2. The proposed AND gate has inputs of B' and (A⊕B) and the output is [B'+(A⊕B)]' which is Boolean equivalent to (A.B). The proposed OR gate has inputs of A' and (A⊙B) and the output is [A'. (A⊙B)]' which is Boolean equivalent to (A+B). Fig.3 shows the waveforms of proposed AND & OR logic circuits. The designed AND, OR gates produce a full swing output with less power dissipation. So, the designed full adder circuit achieves low power dissipation, low PDP compared to other designs. Fig. 4 shows the waveforms of the designed full adder at operating voltage of 0.9V.

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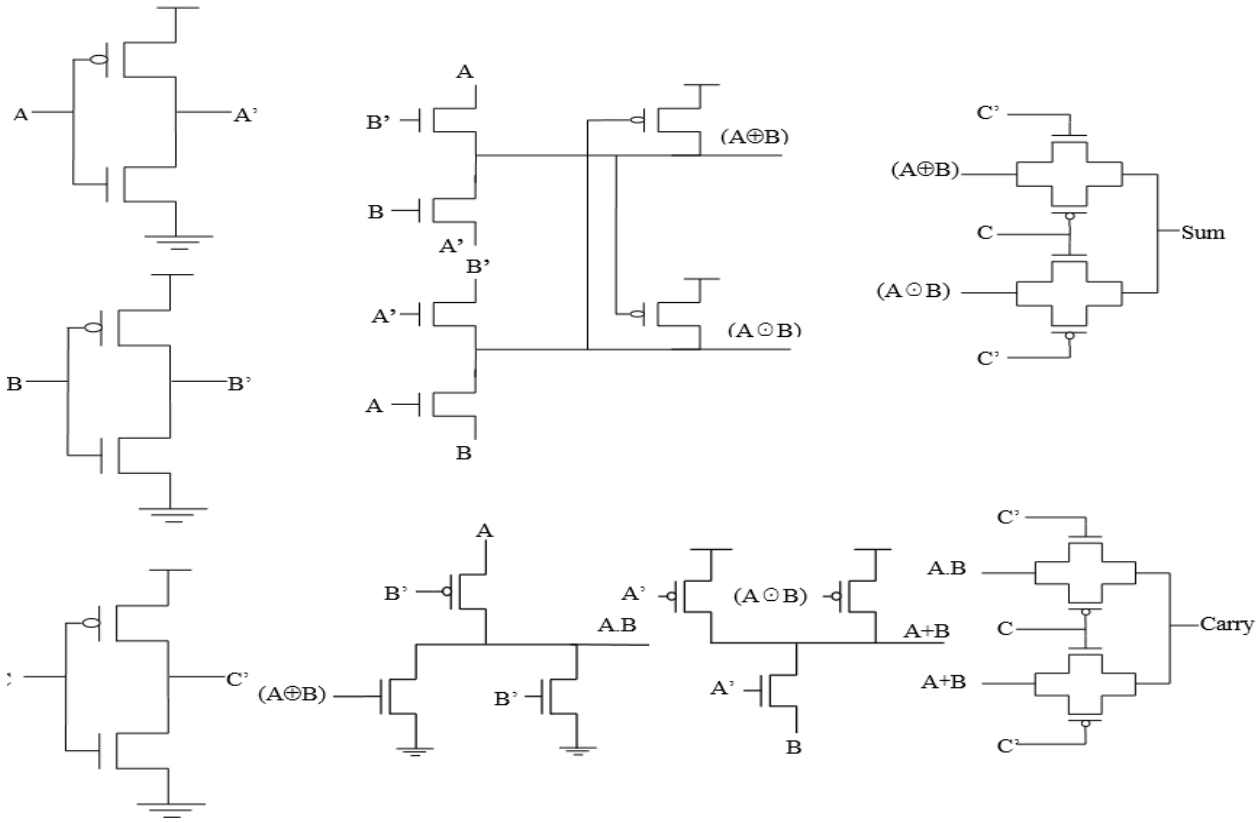

Figure 2: Internal logic circuit diagram of designed full adder

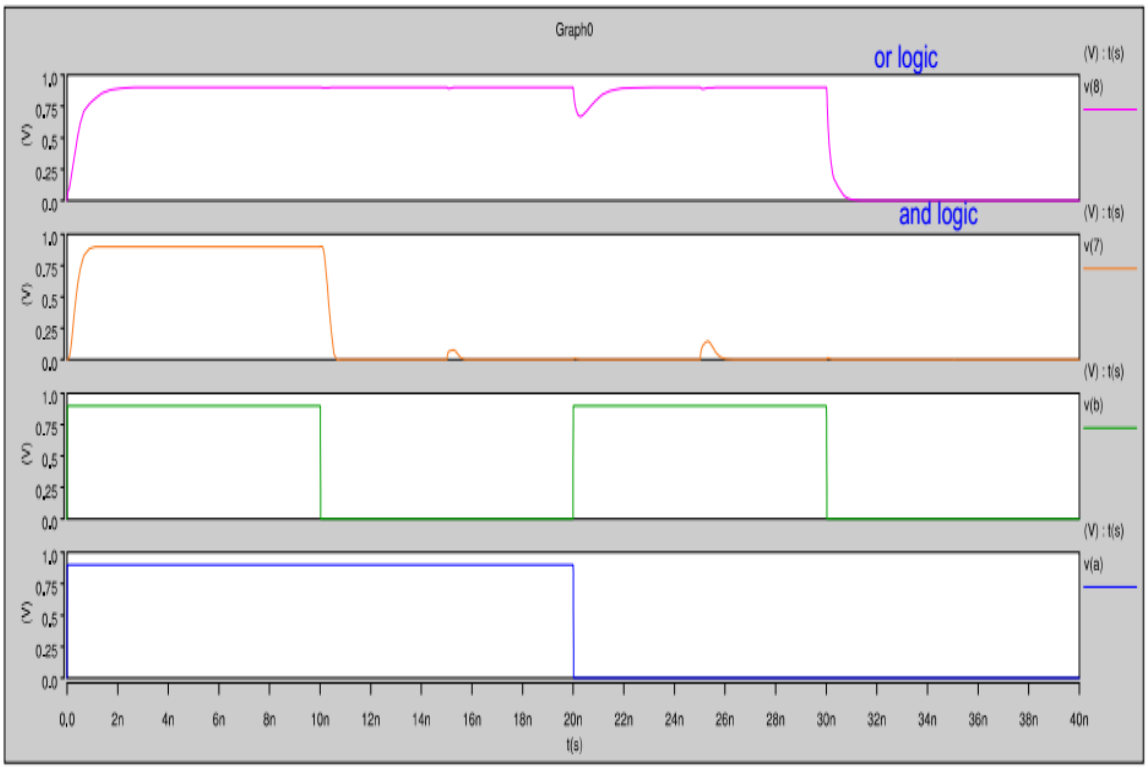

Figure 3: Output waveforms of AND and OR logic circuits at supply voltage of 0.9V

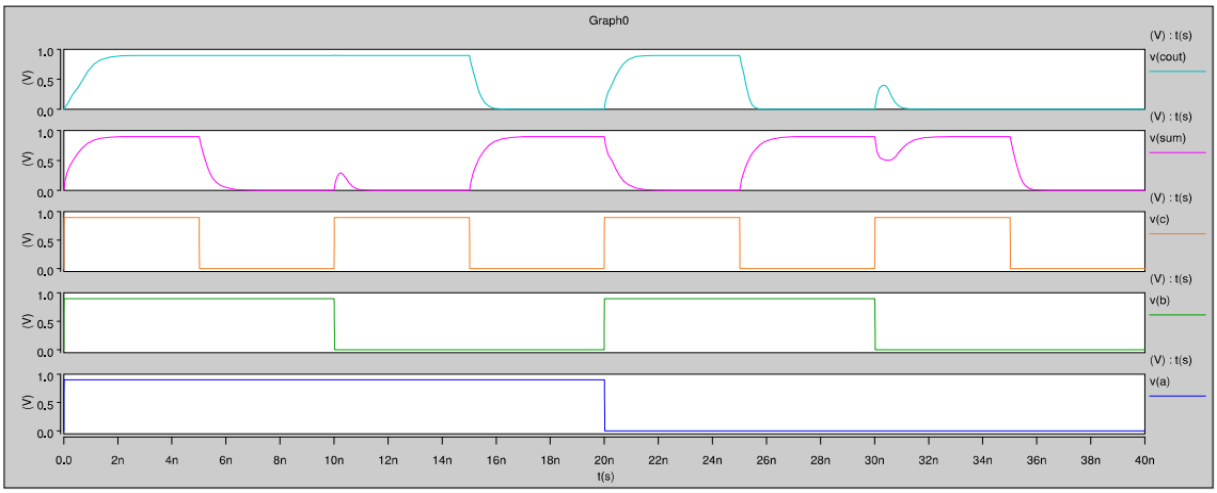

Figure 4: Simulation waveforms of full adder circuit at supply voltage of 0.9VSIMULATION TEST BENCH

The performance of adders must be evaluated under load conditions and driving elements. The adder must produce full swing output under load conditions and also it must supply sufficient current to the driving elements.

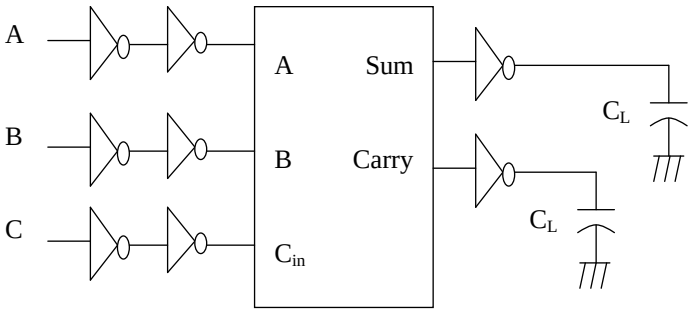

Figure 5: Simulation environment test bench

Fig. 5 shows the test bench setup used in simulation of full adder circuits. This simulation environment has been used for the analysis of full adder circuits by adding inverters at the input and output terminals. The size of transistors used for achieving full swing output with output capacitive load of 6.4fF. The performance of design under test (DUT) is calculated in terms of propagation delay, average power dissipation and power-delay-product. The propagation delay is measured for 50% of input signal voltage resulting in 50% of output signal voltage of all the rise and fall transitions. The average power consumption is measured for all possible input transitions of the circuit.

III. SIMULATION RESULTS OF PROPOSED CMOS BASED FULL ADDER

The simulation results of the circuits in [21-22], Hybrid CMOS [2] and designed full adder circuit are carried out with PTM 32-nm CMOS technology using HSPICE tool. Simulations are performed on all the four full adders using the common test bench on varying operating voltage ranging from 0.6V to 1V. Full adder without test bench means no buffers are inserted at input and outputs. Full adder with test bench means buffers are attached at input terminals and output terminals, with load of 6.4fF at output nodes. Comparison of the proposed full adder (without and with test bench) with regard to propagation delay, average power dissipation and Power-delay-product (PDP) with the existing full adders using PTM 32-nm CMOS technology is given in Tables 1, 2.

The designed full adder has lower power dissipation and low PDP values when compared with all the other three adder circuits. The designed full adder (without test bench) achieved power dissipation reduction of 71.2% and PDP reduction of 80.8% respectively comparing with circuit in [21] at operating voltage of 1V. The designed circuit achieved reduction of 62.8%, 10.6% in power dissipation and 62.9%, 7.99% reduction in PDP compared with circuits in [2] and [22] respectively.

Table 1 Comparison of full adders (without test bench) with their Delay, Power and Power-Delay-Product values at different operating voltages.

V_{DD}(V)	1.0	0.9	0.8	0.7	0.6
DELAY (nS)					
Circuit in [21]	10.887	11.284	12.192	13.183	13.751
Circuit in [22]	7.312	7.219	6.986	6.328	4.320
Hybrid CMOS [2]	7.074	6.972	6.796	6.437	5.523
Proposed	7.284	7.231	7.141	6.960	4.511
POWER DISSIPATION (µW)					
Circuit in [21]	24.432	15.567	8.707	4.140	2.530
Circuit in [22]	18.883	13.279	8.785	5.255	2.713
Hybrid CMOS [2]	7.854	6.177	4.806	3.655	2.649
Proposed	7.018	5.576	4.364	3.324	2.429
POWER DELAY PRODUCT (fJ)					
Circuit in [21]	265.987	175.662	106.157	54.575	34.79
Circuit in [22]	138.066	95.871	61.369	33.257	11.720
Hybrid CMOS [2]	55.559	43.066	32.662	23.527	14.630
Proposed	51.115	40.319	31.159	23.133	10.958

Table 2 Comparison of full adders (with test bench) with their Delay, Power and Power-Delay-Product values at different operating voltages.

V_{DD}(V)	1.0	0.9	0.8	0.7	0.6
DELAY (nS)					
Circuit in [21]	11.512	12.059	13.298	14.394	15.998
Circuit in [22]	6.482	6.132	5.386	4.754	3.321
Hybrid CMOS [2]	6.614	6.421	6.088	5.431	3.773
Proposed	6.878	6.728	6.456	5.886	3.718
POWER DISSIPATION (µW)					
Circuit in [21]	28.591	18.359	11.068	6.253	3.798
Circuit in [22]	25.507	17.148	11.202	7.093	4.189
Hybrid CMOS [2]	15.627	12.402	9.719	7.523	5.182
Proposed	14.167	10.985	8.422	5.299	3.526
POWER DELAY PRODUCT (fJ)					
Circuit in [21]	329.131	221.392	147.189	90.014	60.760
Circuit in [22]	165.331	105.157	60.334	33.723	13.915
Hybrid CMOS [2]	103.353	79.631	59.166	40.855	19.552
Proposed	97.450	73.905	54.370	31.191	13.110

Comparison of full adder circuits in terms power dissipation and power-delay-product (PDP) is shown in Fig 6 and 7 respectively. The designed full adder dissipates lower power against other circuits over a range of voltages from 1V to 0.6V.

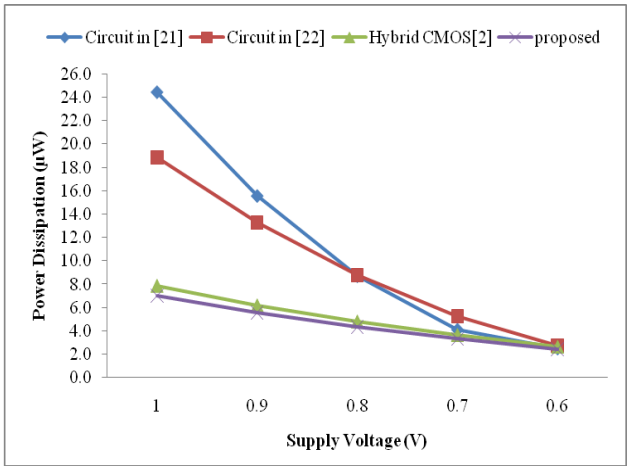

Figure 6: Power dissipation of the full adder circuits (without test bench) for different supply voltages

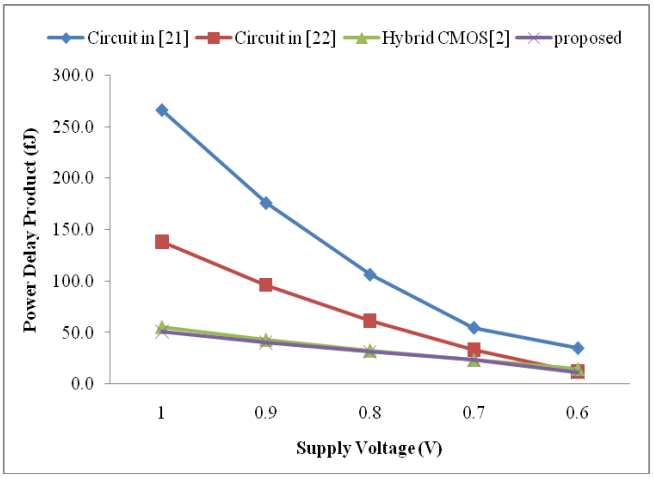

Figure 7: Power-Delay-Product (PDP) of the full adder circuits (without test bench) for different supply voltages

The designed circuit with test bench achieves 50.4% reduction in power dissipation, 70.3% reduction in power delay product comparing with circuit proposed in [21] at voltage of 1V. Comparing to the circuit in [2] and [22] the proposed circuit achieved power dissipation reduction by 9.34% 44.4% and power-delay-product reduction by 5.7% 41% respectively. Comparison of power dissipation and PDP of simulated circuits with test bench is presented in Fig 8 & 9 respectively.

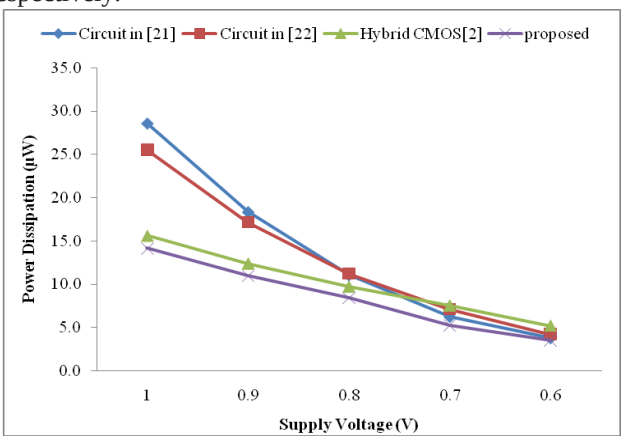

Figure 8: Power dissipation of the full adder circuits (with test bench) for different supply voltages

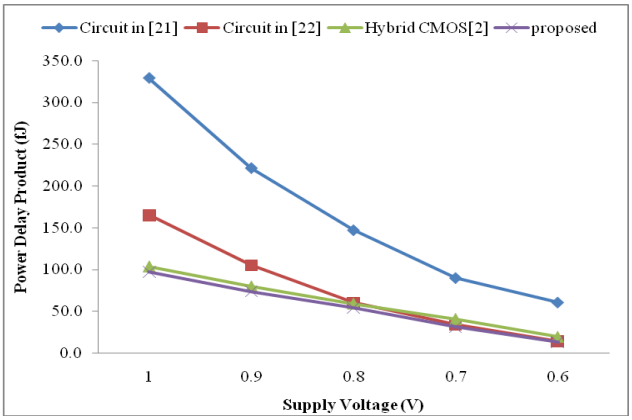

Figure 9: Power Delay Product (PDP) of the full adder circuits (with test bench) for different supply voltages

Below 0.6V all the full adder circuits fail to produce the full swing output voltages and also the power dissipation increases due to high leakage currents of CMOS circuits. To reduce the power dissipation, conventional CMOS devices are replaced with FinFET devices due to its low leakage currents [24]. FinFETs differ in structure only but the operation remains same like conventional FETs. FinFET is controlled by multi-gate terminal known as 'fin' which surrounds the channel between drain and source in three dimensional. Since gate surrounds channel, it forms gate electrodes on both sides to reduce the leakage currents and increase the driving current. FinFETs has control over process parameter variation because of self-alignment of gates. Fig 10 shows the cross-sectional view of FinFET device. The effective width of the channel 'W' must be twice the height of the fin 'H_{fin}' [25].

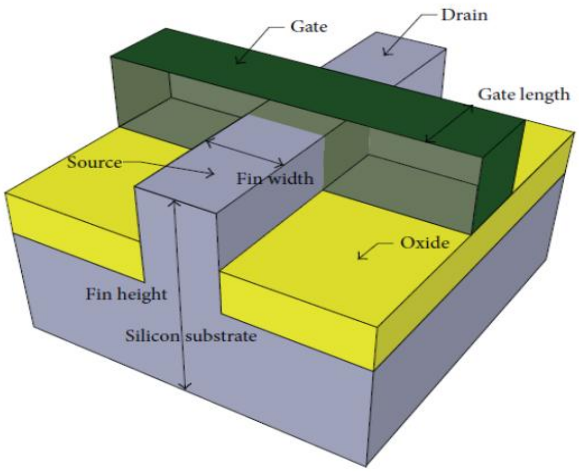

Figure 10: FinFET device structure

IV. SIMULATION RESULTS OF FINFET BASED FULL ADDER

The proposed circuit is implemented with FinFET devices to achieve the advantage of low power dissipation with full swing output voltages at very low operating voltages. Fig. 11 shows the output waveforms of designed full adder implemented using FinFETs.

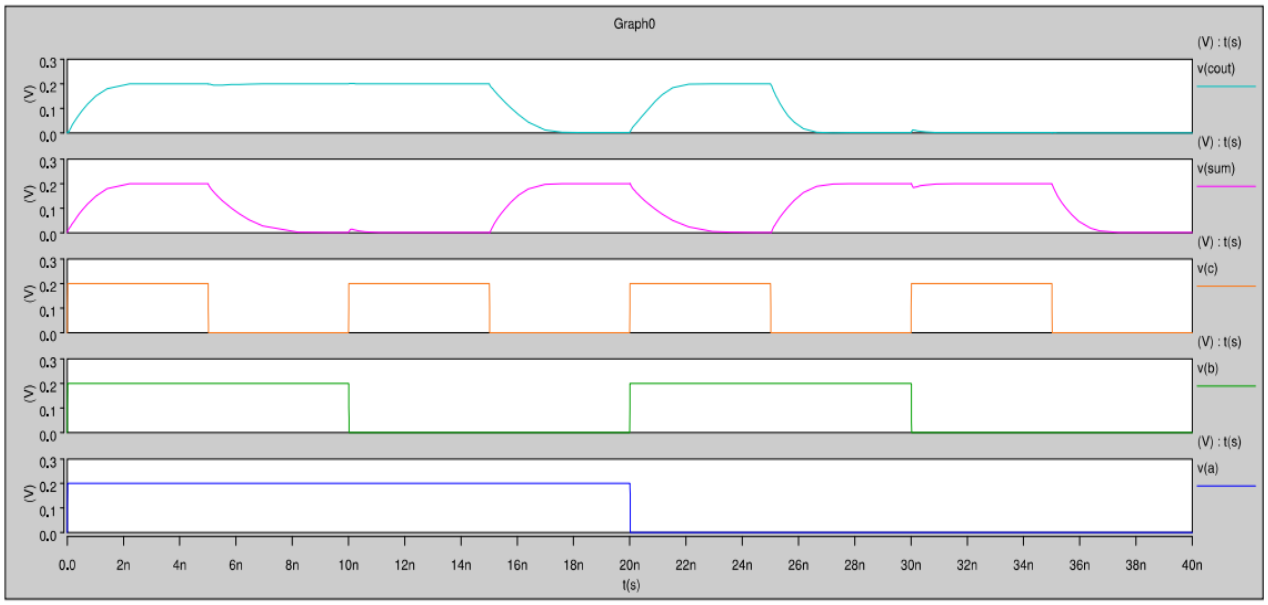

Figure 11: Snapshot of waveforms of proposed full adder designed with FinFETs

The designed full adder is designed using FinFET devices and simulated using PTM 32-nm DG FinFET model. The proposed FinFET based full adder is simulated with different capacitive loads at operating voltage of 0.9V. Table 3 shows the delay, power consumption and Power-delay-product of proposed FinFET based full adder without and with test bench under different load capacitances. Variation of delay, power dissipation and power-delay-product of proposed FinFET based circuit with capacitive loads is presented in Fig 12, 13 and 14 respectively.

Table 3 Delay, Power and Power-delay-product of designed FinFET based full adder at different capacitive loads

Load capacitance		6fF	5fF	4fF	3fF	2fF	1fF
Without test bench	Delay (nS)	5.035	5.03	5.024	5.019	5.014	5.009
	Power Dissipation (nW)	1566.9	1370.6	1177.9	993.4	805.8	627.7
	PDP (fJ)	7.89	6.89	5.92	4.99	4.04	3.14
With test bench	Delay (nS)	5.049	5.042	5.035	5.028	5.023	5.017
	Power Dissipation (nW)	4366.6	3882.1	3408.6	2949.1	2544.1	2415.5
	PDP (fJ)	22.05	19.57	17.16	14.83	12.78	12.12

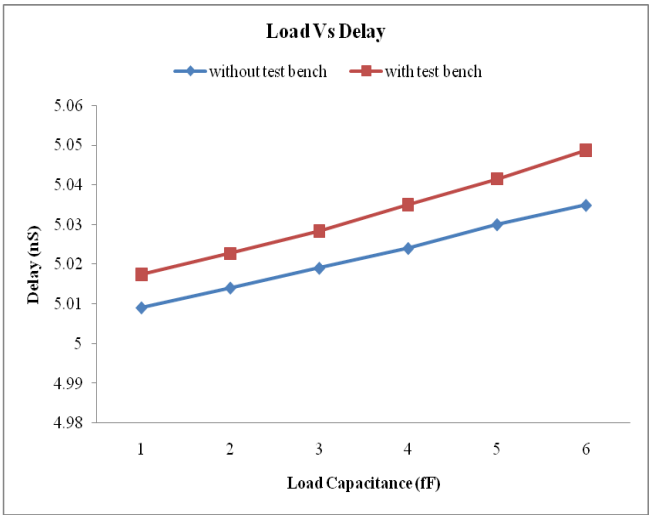

Figure 12: Delay variation with load of Proposed FinFET based full adder without and with test bench

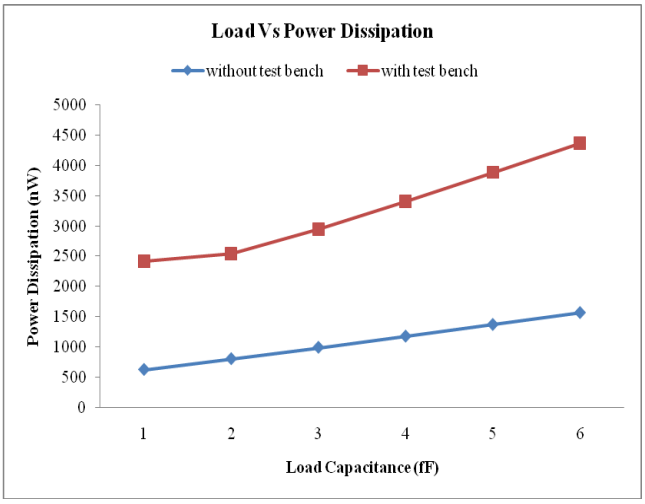

Figure 13: Variation of Power dissipation with load of Proposed FinFET based full adder without and with test bench

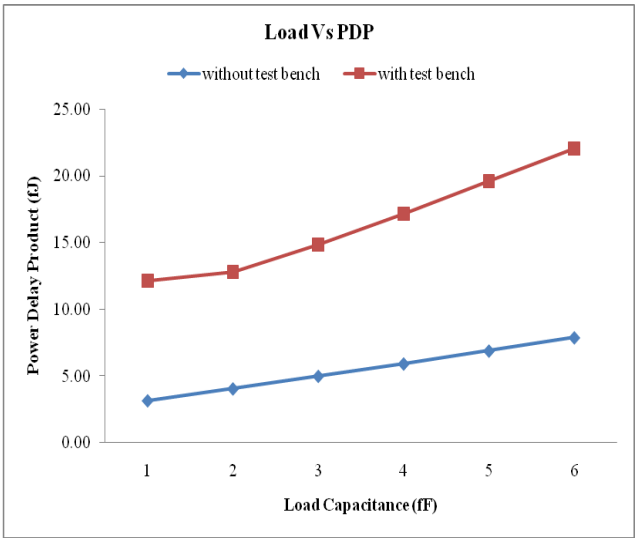

Figure 14: Variation of power-delay-product with load of Proposed FinFET based full adder without and with test bench

The proposed FinFET based full adder circuit is simulated at operating voltages from 1V to 0.2V with capacitive load of 5fF. propagation delay, average power dissipation and power-delay-product of proposed FinFET based proposed full adder without and with test bench at different operating voltages are given in Table 4. variation of Delay, power dissipation and PDP of proposed FinFET based circuit with different operating voltages are given in Fig. 15, 16 and 17 respectively. It is evident that the FinFET based proposed full adder circuit is able to produce full swing output voltage at reduced operating voltages with reduction in power dissipation and PDP.

Table 4 Delay, Power and power-delay-product of designed full adder at different operating voltages

Vdd (V)		1	0.9	0.8	0.7	0.6	0.5	0.4	0.3	0.2
Without test bench	Delay(nS)	5.028	5.029	5.031	5.035	5.041	5.052	5.073	5.139	5.580
	Power Dissipation (nW)	1894	1370.6	973.9	672.8	445.9	280.3	164.8	88.3	38.3
	PDP (fJ)	9.52	6.89	4.90	3.39	2.25	1.42	0.84	0.45	0.21
With test bench	Delay(nS)	5.042	5.046	5.045	5.047	5.053	5.066	5.092	5.178	5.728
	Power Dissipation (nW)	3882.10	2611.30	1906.80	1245.40	767.36	447.92	247.33	127.20	55.43
	PDP (fJ)	19.57	13.18	9.62	6.29	3.88	2.27	1.26	0.66	0.32

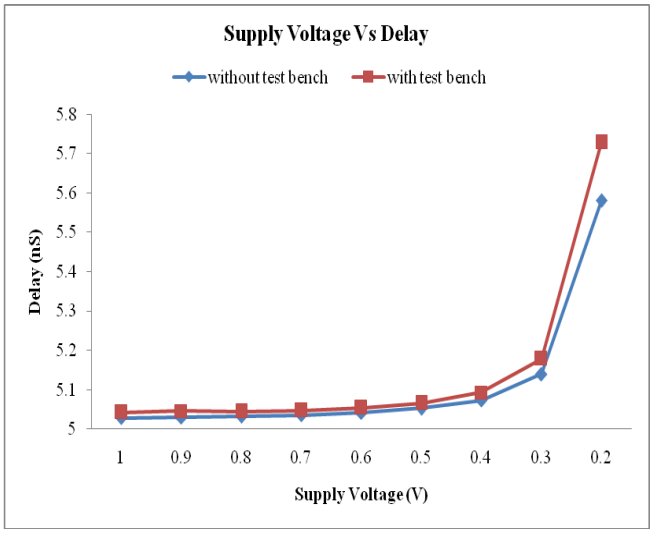

Figure 15: Delay variations against supply voltage of Proposed FinFET based full adder without and with test bench

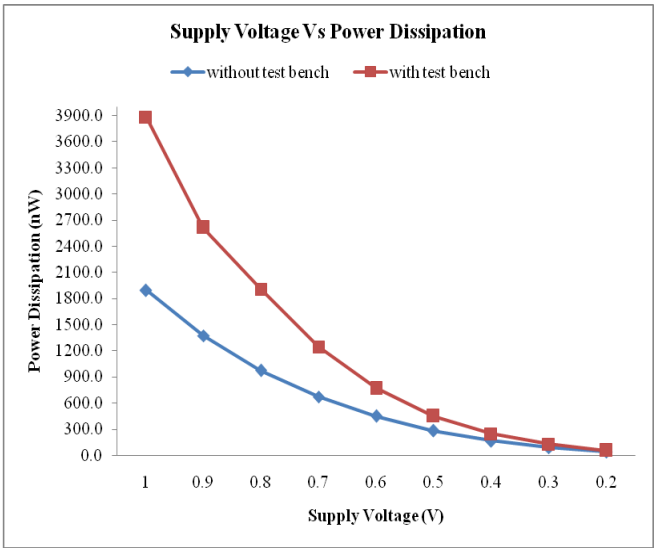

Figure 16: Power dissipation variations against supply voltage of Proposed FinFET based full adder without and with test bench

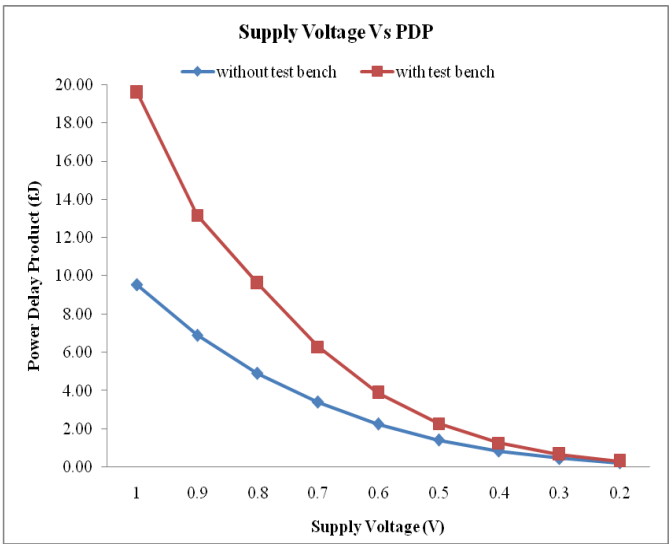

Figure 17: Power-delay-product variability against supply voltage of designed FinFET based full adder without and with test bench

V. CONCLUSION

In this research paper, a new hybrid full adder with AND, OR logic circuits are proposed. The designed full adder is implemented using both CMOS and FinFETs. The simulations are carried out on HSPICE using 32-nm PTM model. The proposed CMOS based full adder achieves power reduction of 50.4%, 44.4%, 9.34% and PDP reduction of 70.3%, 41%, 5.7% comparing with other full adder designs. FinFET based design has an advantage of driving capacitive loads with full output voltage swing and also operatable at very low voltages. The FinFET based proposed full adder achieves low power dissipation and low PDP than CMOS based circuit.

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