International Journal of Recent Technology and Engineering (IJRTE)
ISSN: 2277-3878 (Online), Volume-8 Issue-2, July 2019

Design of Non-Volatile Phase Change Memory for FPGA Architectures

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Abstract*: Phase change memory circuit has been designed to function as Non-Volatile memory circuit using 45nm and 90nm technology. The other non-volatile memory circuits like Flash and MTJ-MRAM are realized in 45nm and 90nm CMOS Technology in which their output behavioral characteristics, power and delay parameters are obtained in order to compare with performance of MTJ-MRAM and Flash memory circuits. The design has been carried out using Cadence Virtuoso – Electronic Design Automation (EDA) Software tool in Analog Design Environment (ADE), the advanced design and simulation is performed in virtuoso platform. The schematic for PCM is designed and simulations are carried out in 45nm and 90nm technology using a test environment. Further the work has been extended to design memory circuit that gives non-volatility which can be implemented for FPGA architecture. Existing FPGA architectures which are non-volatile based, have limitations and demands for a better computing memory to be integrated within. The present work brings out a novel Phase Change Memory design with better performance than existing flash based and anti-fuse based types of FPGAs and also better than MTJ-MRAM attributes. The present work compares attributes like power dissipation and delay of PCM with other non volatile memories used for FPGA architecture. Further PCM techniques indicate significant power and delay reduction when compared to MTJ-MRAM and flash memory circuit.

***Index Terms*: Phase Change Memory, Non-Volatile Memory, Endurance, Power, Delay.**

I. INTRODUCTION

The continuous demand for fast computing devices becomes very dominating and forces the semiconductor industry to find more feasible and better alternative in the memory hierarchy. The conventional memories like SRAM, DRAM have played prominent role in computing devices but however due to continuous device miniaturization and evolution of modern computing systems power factor becomes the major concern and these memory devices face design challenges. The future computing systems are looking forward for potential alternatives of existing memories that combines the speed of SRAM, density of DRAM, non-volatility of Flash memory and hence become an attractive alternative for future memory hierarchy.

Non-Volatile Memory (NVM) advances, take up a primary role in the microelectronics Industry. The continual growing of functionalities and performances of consumer electronics products for example, computerized cameras, MP3 players, advanced mobile phones, PCs, also, more as of late, hard discs claims for a nonstop improvement of memory limit and highlights. Among Non-Volatile Memories, Flash memory is the dominant in today's NVM market and is also expected to continue in near future as well [5].There is lot of scope for upcoming non-volatile memories which can be alternative to Flash memory in future. The objective of the developing memories is mainly concentrated on the reduced power consumption and improved performance. Among many upcoming non-volatile memories Phase Change Memory is one of the interesting emerging non-volatile memories [6,10].

Objective: As the density increases with increasing demand in portable devices, scalability becomes increasingly important in order to accommodate the demand. With increasing scalability Flash memory faces difficulties in maintaining the specifications of memory and also the performance. These factors create challenge for the existence of Flash memory in near future and results in transition of memories that are more reliable on scaling. The paper proposes a novel design of Phase Change Memory (PCM) that offers better performance compared to Flash memory in terms of delay and power. The work also compares the performance of PCM with that of designed MTJ MRAM and Flash memory.

Motivation: With growing demand of portable devices and its computational characteristics, the computing systems also demands for emerging non-volatile memories. One such computational system being Field Programmable Gate Array (FPGA) which is mainly classified based on memory such as, SRAM based FPGA, Flash based FPGA and Anti-fuse based FPGA. Among these classifications SRAM being fast but volatile, while Anti-fuse is only one time programmable and Flash based FPGA not offering many advantages as that of SRAM. It is required to design a new non-volatile memory based FPGA which offers the combined advantage of speed of SRAM and non-volatility of Flash. The research work focus on design of new non-volatile memories like MTJ-MRAM and PCM for FPGA architecture.

Phase Change Memory

The Phase Change Memory (PCM) is also called Ovonic Unified Memory (OUM) or Phase-Change Random Access Memory (PCRAM) is a class of solid state Non-volatile Memory.

Revised Manuscript Received on 30 July 2019.

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PCM is a non-volatile memory and is viewed as a standout amongst the most encouraging contender for the cutting edge memory technology [7].

PCM is essentially a storage class memory operating on the principle of resistance change to store data.

PCM employs chalcogenide glass material that is sandwiched between two electrodes [1].

The operation of the memory is fundamentally based on a unique behavior of Chalcogenide glass material, that can switch between two different states called as Crystalline state and Amorphous state [2,9]. The chalcogenide material is connected to electrode on one side and on the other side it is connected to heating element which in turn is connected to the other electrode as shown in figure 1.

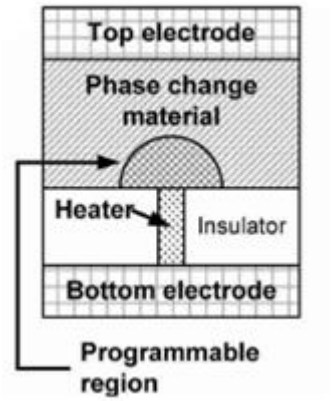

Figure 1: PCM memory cell [3]

When voltage is applied at the electrode it heats the resistive heater, depending on the applied voltage the current changes and when current is large enough it heats the heating element (resistive heater). Large current is injected to the chalcogenide layer through the resistive heater from electrode, at this stage the material reaches crystallization state or also called as set state during which the material behaves conductive in nature [7]. While when the material is cooled, that is when the current is removed, it reaches amorphous state or also called as reset state in which the material behaves resistive in nature. If material is crystalline then it offers low resistivity and in case of amorphous it offers high resistivity [4,8]. The set and reset state of the material stores the data on memory cell.

II. DESIGN OF PHASE CHANGE RAM

In PCM device the memory element is basically a variable resistor that is made of a chalcogenide material. The PCM element is controlled by bottom electrode through the selection transistor by the bit line and top electrode through word line. The PCM cell can be accessed by applying suitable bias at word line and bit line.PCM basically functions between two states namely high conductive poly-crystalline state and low conductive amorphous state through proper electrical pulses that cause heating of the material.

The memory cell mainly comprises of an NMOS device which behaves like the access transistor and a chalcogenide element. The gate of NMOS device is connected to word-line and the chalcogenide material is connected to the source of the NMOS device [10]. The chalcogenide is connected to the electrode through which the voltage is applied and its output is controlled by the access transistor which also behaves like an isolation device as shown in figure2.PMOS device can also be used instead of NMOS but it is preferable to use NMOS due to its large drive current. The set and reset state offering varying resistance stores data on the memory cell.

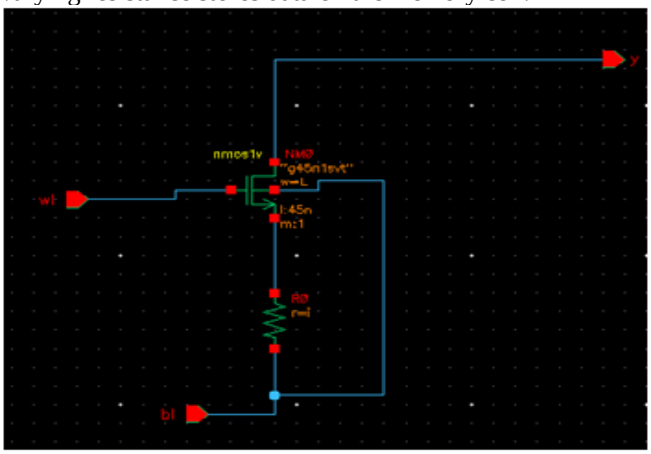

Figure 2: Schematic of PCM

III. METHODOLOGY

The results of PCM design are obtained using Cadence Virtuoso Schematic tool, by designing the schematics for PCM memory and simulating the design and verifying its behavioral characteristics. The VLSI design flow is adopted for obtaining the results using Cadence Virtuoso tool. Design Flow in VLSI is sequence of steps involved in designing a circuit for analog or digital IC. The flow begins from System specification, followed by Functional or Architectural design, then subsequently functional verification and Logic design which involves gate level representation. Succeeding these steps the circuit design is done accompanied by circuit verification and simulation of circuit designed as shown in figure 3.

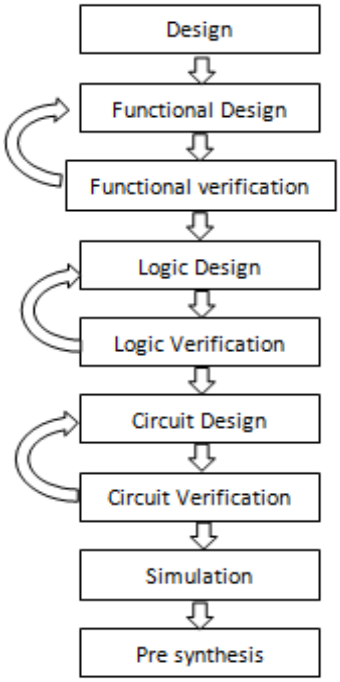

Figure 3 : VLSI Design Flow

IV. PERFORMANCE ANALYSIS

The PCM memory cell is designed and verified for its output behavioral characteristics using cadence virtuoso schematic tool. A resistive PCM memory design is done and also the Flash and MTJ MRAM circuits were designed using cadence tool. The figure 4 shows the output behavioral characteristics of PC-RAM, whose behavioral characteristics shows non-volatile behavior as compared with Flash and MTJ-MRAM memory circuits. The output obtained for various values of resistance that is offered by the circuit and its data stored at various states is shown in figure 5.

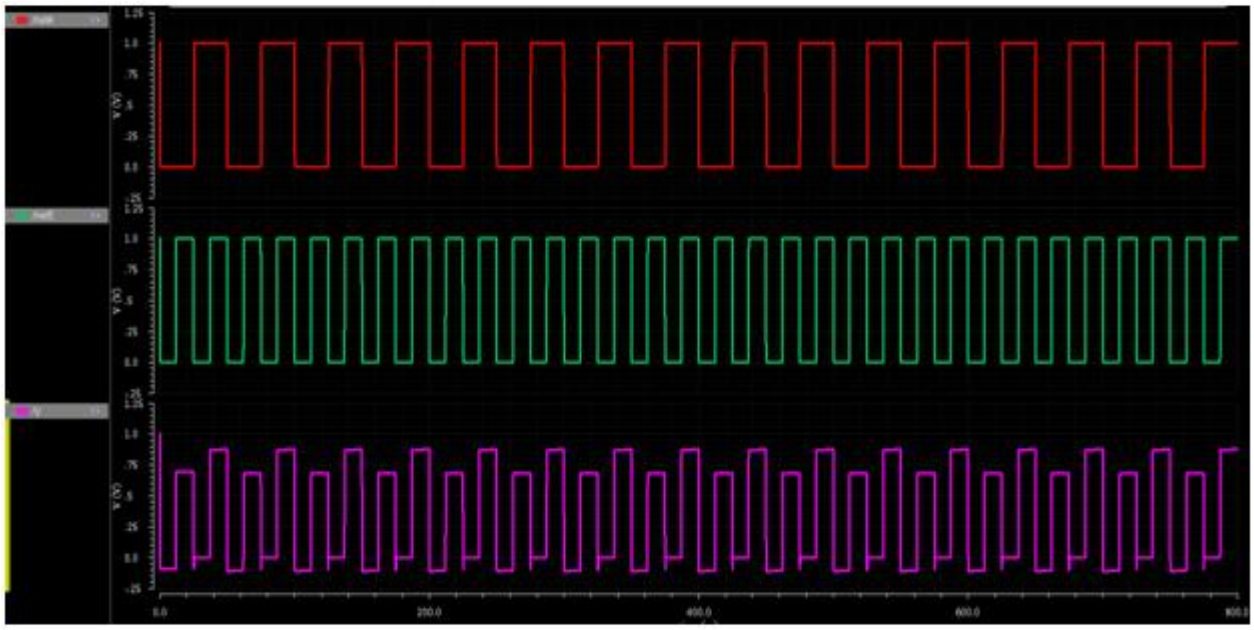

Figure 4: Output behavioral characteristics of PCM

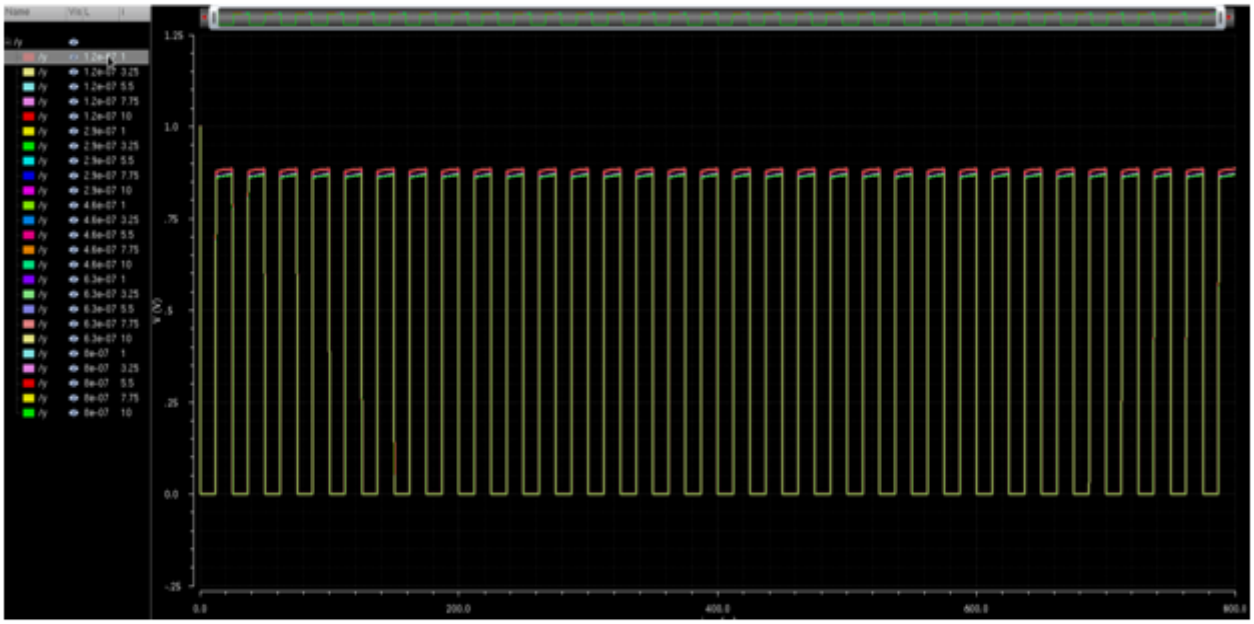

Figure 5: Output Behavioral Characteristics Of PCM With Scaling And Change In Resistance

The output obtained when voltage is high and when high current is passed through the memory cell. The full swing output is seen at resistance of 1 ohm and NMOS width of 120 micrometer as seen in figure 6 and the output behavioral characteristics obtained from MTJ MRAM memory cell is shown in figure 7.

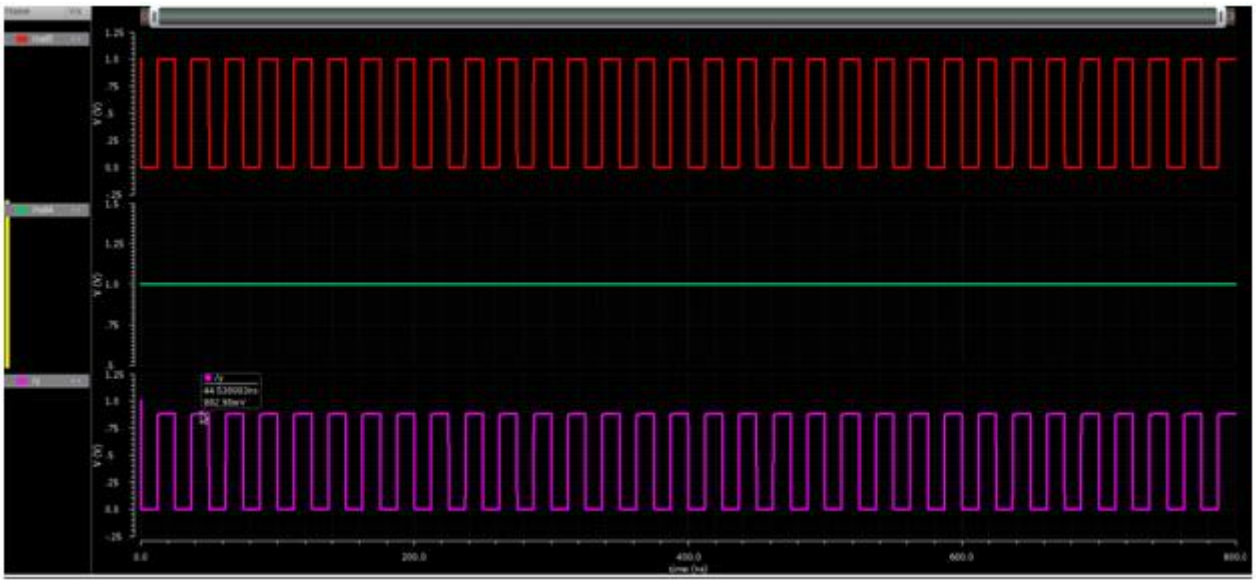

Figure 6: Output behavioral characteristics of PCM at large applied current

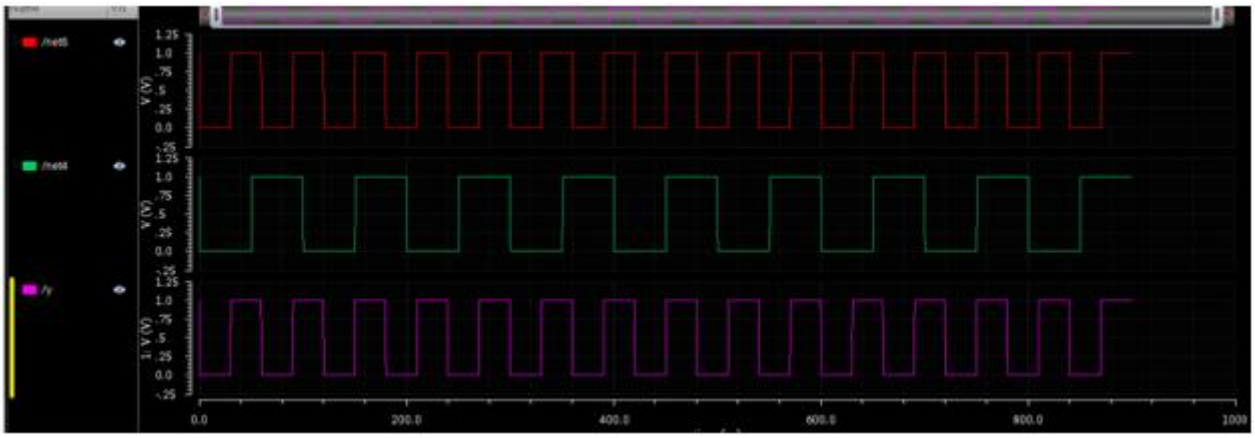

Figure 7: Output behavioral characteristics of MTJ-MRAM

V. RESULTS AND DISCUSSION

Flash, MTJ-RAM and PCM circuits are designed PCM circuit in 90nm and 45nm technology and attributes like power and delay are estimated. The power dissipation of PCM is found to be ~21.42x10^{-12} W and delay is found to be ~12.09x10^{-9}s in 90nm technology. Also the power dissipation of PCM is found to be ~9.60x10^{-12}W and delay is found to be ~7.66x10^{-12}s in 45nm technology. The results shows that there is prominent reduction in power dissipation of PCM and also have good speed of operation.

It is observed from SRAM behavioral characteristics that the data is stored only when word-line is high and when wordline is low the data is not stored in memory cell. This behavioral characteristic of SRAM makes it volatile and hence the data is not retained in SRAM on power off. While in the behavioral characteristic of flash memory which is the present non volatile memory in market showed that data is retained even when word-line is low. This characteristic of Flash memory makes it non volatile that stores data even when powered off [9]. It is observed that in the designed resistive PCM memory cell, it offers similar behavioral characteristics of that of flash memory showing non-volatility. Also the attributes like power dissipation and delay are measured for designed PC-RAM circuit and it is observed that PC-RAM offers better performance than the flash memory.

Table1: Comparison Of Different Non-Volatile Memories

Memory	Delay	Power	Feature
NAND-FLASH			
90nm Technology	4.56x10^{-12}s	5.4x10^{-9}W	Non-Volatile
MTJ-MRAM			
90nm Technology	15.14x10^{-15}s	19.97 x10^{-9}W	Non-Volatile
45nm Technology	70.85x10^{-15}s	11.73 x10^{-9}W	Non-Volatile
PC-RAM			
90nm Technology	12.09x10^{-9}s	21.42x10^{-12}W	Non-Volatile
45nm Technology	7.66x10^{-12}s	9.60x10^{-12}W	Non-Volatile

A detailed comparison between different non-volatile memories like NOR-Flash, MTJ-MRAM memories designed in 90nm and 45nm technology is compared with that of PC-RAM and shown in Table 1. The observation shows that PC-RAM exhibits non-volatile feature offering good speed and low power consumption.

VI. CONCLUSION

The following conclusion can be made from the behavioral analysis of circuits and the transient analysis of the simulation carried out.

1. The VLSI design of PC-RAM shows that there is significant power reduction of about 3 times when compared to MTJ-MRAM and that of Flash memory in 90nm and as well as in 45nm technology. The delay of the design shows as there is increase in delay of about 3 times compared to MTJ-MRAM which is bottleneck, but whereas when compared with Flash it almost maintains the same speed.
2. It is also noticed that the designed PC-RAM offers non-volatility feature along with storing data in different states. Hence by integrating the 45nm PC-RAM for FPGA architecture, the power is eventually reduced which is more advantageous than the existing SRAM based or Flash based FPGAs.
3. Overall the design offers tremendous reduction in power about 3 times and also offers non-volatile behavioral characteristics.

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