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Design and Implementation of Fpga Based Digital Switching Controller for Dc-Dc Converters Used In System- On- A-Chip Applications

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Abstract*: *DC-DC converters are electronic devices that are used to change DC electrical power efficiently from one voltage level to another. This paper proposes a new Digital Pulse Width Modulator (DPWM) which generates variable duty cycle PWM pulse and it can be used as switching controller for DC-DC converters used in battery powered portable electronic and mobile devices. DPWM utilizes the advantage of Digital Clock Manager (DCM) present in FPGA to multiply the clock frequency to eliminate the clock skew. The proposed DPWM uses the four bit gray counter and one hot encoder with SR flip flop to generate the PWM pulse whose duty cycle can be varied according to the control signal. To verify the results DPWM was implemented in SPARTAN 3A.

Index Terms*: *Digital Clock Manager (DCM),FPGA,Gray counter, Pulse Width Modulators

I. INTRODUCTION

In today scenario battery powered applications need a low power, high switching frequency digital switching controller to regulate the voltage in DC-DC Converters[1]. Sensor can be used to measure the change in power converter output signals and power converter output signals are converted in to digital signals using Analog to Digital converter. These signals can be used as input to digital controller which adjusts the duty cycle of PWM pulse which controls the power converters. Digital control scheme is shown in Fig.1. The power levels in these applications are in the range of milli watts and switching frequency in the range of MHZ. There are different digital control techniques realized with DSP and Microcontrollers to generate the variable duty cycle PWM pulse in which high switching frequency leads power losses. With advancement in Very Large Scale Integration Technology (VLSI) and development of design tools it is possible to develop the digital controller which has high speed, lower power realized with Field Programmable Gate Array (FPGA). FPGA's are known for re programmability, ease of design and low cost etc. DPWM implemented in FPGA can use as switching controller to control DC-DC Converters used in batter powered applications. Proposed PWM digital controller is shown in Fig.2. Traditional DPWM techniques are counter and comparator based and these techniques uses binary counter and in binary counter multiple bits changes at a time for each change in switching level. These counter and comparator are power consuming devices[2]. The PWM signal generated by these methods is not constant, they are duty cycle dependant. The output PWM signal value is given by

Output = Duty cycle (D) * input ---------- (1)

Duty cycle $D = T_{ON}/(T_{OFF}+T_{ON})$ ---------- (2)

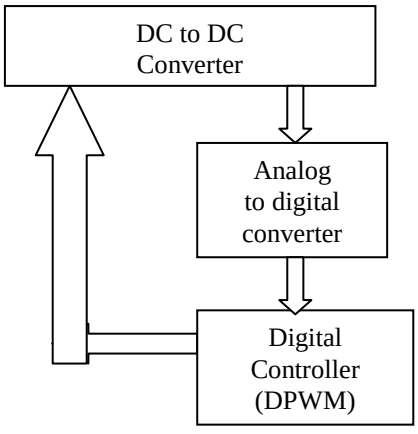

Fig. 1 Block Diagram of Digital Control Scheme for DC-DC Converter

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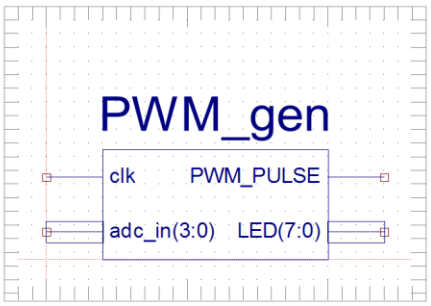

Fig. 2 Schematic symbol for PWM digital controller

II. LITERATURE REVIEW

There are different architecture available for DPWM to generate PWM pulses, each of them differs on the type of counter realization and also the based on the methodology used for generation of PWM pulse.

A. ***Counter Comparator Based DPWM.***

DPWM architecture counter is used with comparator along with RS latch to generate the PWM pulse of variable duty cycle [2]. With higher switching frequency and high resolution the clock frequency is high which increases the power consumption[3].

PWM architecture with variable duty cycle from 0% to 100% is achieved with usage of DCM block in FPGA [4]. Comparator compares the counter data, with up-down counter data generated with push buttons and produces variable PWM pulse. This architecture uses DCM to decrease the clock frequency which minimizes the skew of clock signal.

B. ***Delay line based DPWM architecture***

This method eliminates the need for higher clock frequency by using a delay line in which a pulse from a reference clock starts the cycle when the time delay matches with delay experienced through the multiplexer it sets the PWM pulse to high ,when reference clock travels through the delay line and reaches the output selected by the multiplexer it set the PWM output to low[5]. In this method the area increases with increase in resolution bits of multiplexer and causes gate delays

C. ***Hybrid DPWM Architecture***

A hybrid architecture combining the delay line and counter approach proposes a new architecture which compromises between area and power consumption .It uses 32 cell ring oscillator and 32:1 multiplexer[6]. This architecture was developed for low power and lower voltage levels but the control circuit consumes much power which affects the overall power conversion efficiency.

D. ***DLL Based DPWM Architecture***

A new FPGA based Digital pulse width architectur that utilizes the DLL block present in FPGA. This architecture combines a synchronous block with an asynchronous block for increased resolution without increasing the clock frequency. Synchronous block is counter based uses the clock frequency multiplied by four with help of advanced feature of DLL. Asynchronous part which is complex in nature uses the lower clock frequency and phase shifting capability of DLL for decreased power consumption .This clock phase shifting capability the improves the resolution of counter based solution with available number of clock pulses. However this approach has different delay for each data paths which minimizes linearity of proposed DPWM.

III. PROPOSED DPWM ARCHITECTURE

A. ***DCM Block***

Clkin is the input to DCM block in FPGA which provide advanced clocking capabilities to FPGA based applications. DCMs blocks are able to multiply the incoming clock frequency to yield clk2x and clk4x frequency, clock signals along with phase shifted clocking capabilities. This advanced feature of DCM is used to yield a new clock frequency which minimizes the clock skew. In the proposed method 12.5 MHZ input clock frequency is multiplied by two (clk2x) to yield 25 MHZ

1cycle = 1/25MHZ = 40 ns

B. ***Gray Counter***

In gray code only one bit changes at time between two successive values whereas in binary code multiple bit changes at a time which leads to glitches. The gray counter toggles only one bit at a time while the binary counter toggles multiple times .Gray code counter has less noise when compared to binary counter and also consumes half of power as binary counter. The four bit gray counter is designed which starts counting from 0000 to 1000 and when it reaches the final value it sends a enable signal to one hot encoder.

C. ***One Hot Encoder***

One hot encoder is digital circuit in which only one bit is high in a state vector at a time and the remaining bits are zero. It has low switching activity and hence less power consumption, less glitches. The difficulty with one hot encoding is that when number of states increases it increases the number of flip flops. But it is advantageous to incorporate one hot encoder in FPGA as each logic block in FPGA has one or more flip flops.

Each time when the gray counter output reaches final state 1000 it makes the one hot encoder bits D0 to D15 to high state one by one. When D15 bit set to high then the set signal issued to the RS flip flop with help of pulse width control circuit .In the next clock cycle all the bits of one hot encoder resets to zero. Then again counter starts counting from 0000 to 1000 it sets one hot encoder bits one by one to high state, when a particular bit of one hot encoder set to high state (depending on control signal to adjust the duty cycle) pulse width control circuit issues resets signal to RS flip flop.

D. *Pulse Width Control Circuit*

It receives the input signal D0-D15 from one hot encoder, when the D15 bit of one hot encoder set to high state then pulse width control circuit issues set signal to RS flip flop connected to it. When one hot encoder reaches a particular state and based on the control signal for modulating the duty cycle of PWM pulse, pulse width Control Circuit resets the RS flip flop. The PWM width depends on set and reset condition of RS flip flop.

IV. RESULTS AND DISCUSSION

High frequency DPWM architecture with a N bit counter, N bit register with overflow detector and RS flip flop was designed [7]. Traditional architecture is designed with VHDL, behavioral simulations results were obtained for functional verification and synthesized with XILINX ISE 13.3.The target FPGA was SPARTAN 3A. Traditional high frequency DPWM architecture with binary counter is shown in Fig.3

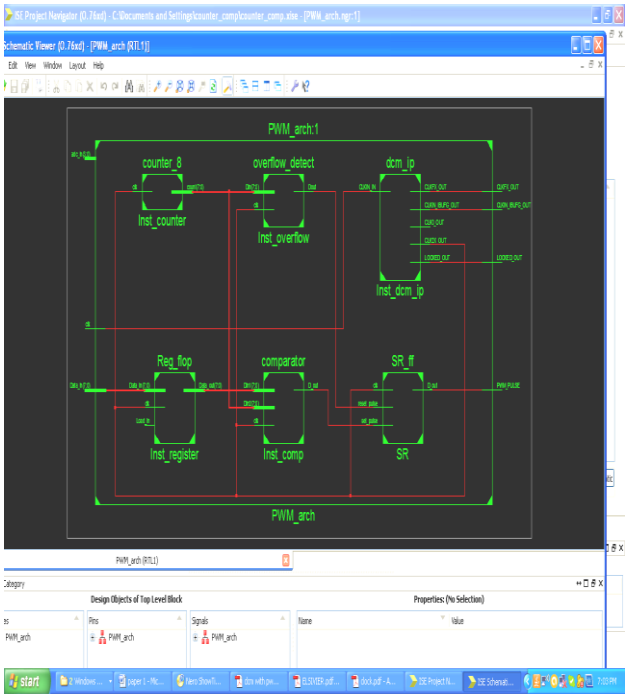

Fig:3 RTL Schematic of High frequency DPWM Architecture.

8 bit binary counter was designed with 8 bit register which stores the duty cycle value. When the clock input is given the binary counter starts counting and comparator checks the value of counter with the data in the register when the counter value matches the register value it sets the RS flip flop to high state, overflow detector detects the overflow signal from counter and it resets the flip flop. The output of RS flip flop gives the PWM pulse. For instance the register value is 10000100 ,the counter starts counting from 00000000 and when it reaches the value 10000100 the comparator output will be 1 which sets the RS flip flop and when counter value overflows the overflow detector will reset the flip flop. This gives the PWM pulse with duty cycle of 48% . The duty cycle value of PWM pulse can be changed by changing the data present in the register.Proposed DPWM technique was designed with VHDL and

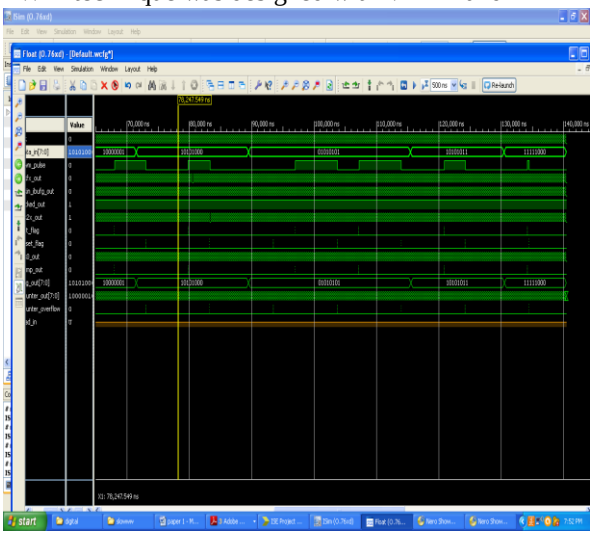

Fig : 4 Simulation Waveforms with variable duty cycle PWM pulse for high frequency DPWM architecture

behavioral simulations were obtained and Synthesized with Xilinx 13.3.Proposed Method is implemented in SPARTAN 3A.The experimental results were obtained for external clock frequency of 12.5 MHZ[8][9].

When the clock pulse is given the gray counter starts counting from $(0000)_G$ to $(1000)_G$ then D0 LSB bit is made high in one hot encoder and it continues till MSB bit D15 bit is made high[10]. When the D15 bit is set to high it sets the RS flip flop, once again the counter starts counting from 0000 to 1000 it again sets the D0 LSB bit in one hot encoder to high state and it continues till the particular bit in one hot encoder is set to high. When it is set to high it resets the flip flop. This set and reset condition of flip flop gives the desired PWM signal. For instance when the control signal(adc) is 1000 the gray counter starts counting from $(0000)_G$ to $(1000)_G$ then the bits of one hot encoder (D0 –D15) one by one goes to high state. When D15 bit $(1000000000000000)_B$ of one hot encoder set to high in turn sets the RS Flip flop. Again when gray counter starts counting from 0000 to 1000 and when one hot encoder D8 bit set to high $(0000000010000000)_B$ it resets the flip flop. This gives a PWM pulse with duty cycle of 55%.

8 bit register value for different duty cycle is shown in Table I. The device utilization summary for the proposed architecture is shown in Table II. The RTL schematic of the proposed DPWM architecture is shown in Fig.5. Simulation waveform for the duty cycle of 60% is shown in Fig.6.

Table I
8 Bit Register Value for Different Duty Cycle

Register Value	ON Time(ns)	OFF Time(ns)	Duty Cycle(%)

00001111	9520	750	94
10001000	4860	5410	47
01010101	6720	3550	65
10101111	3133	7137	39

Table II
Device Utilization Summary

Device Utilization Summary				
Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Flip Flops	51	1,408	3%	
Number of 4 input LUTs	17	1,408	1%	
Number of occupied Slices	35	704	4%	
Number of Slices containing only related logic	35	35	100%	
Number of Slices containing unrelated logic	0	35	0%	
Total Number of 4 input LUTs	35	1,408	2%	
Number used as logic	15			
Number used as a route-thru	18			
Number used as Shift registers	2			
Number of bonded IOBs	14	68	20%	
Number of BUFGMUXs	1	24	4%	
Average Fanout of Non-Clock Nets	1.90			

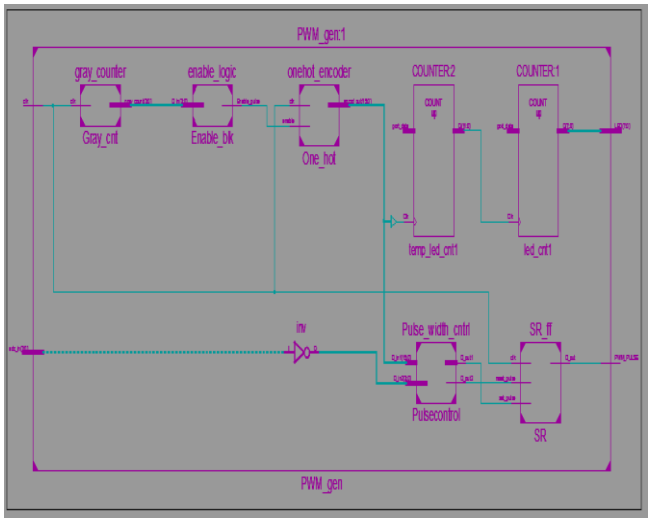

Fig. 5 RTL schematic of proposed PDWM

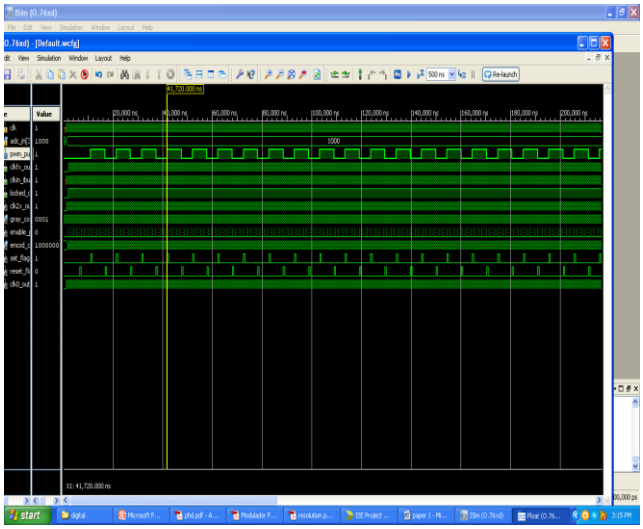

Fig. 6 Simulation Waveforms for duty cycle = 60% with adc:((1011)

V. RESULTS AND DISCUSSION

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After doing Place and Route simulation the VHDL code was down loaded into SPARTAN 3A The input was given with 4 switches in the board and results were viewed in Digital storage Oscilloscope. The input clock frequency given was 12.5 MHZ and multiplied by two with DCM and power analysis were obtained for different input frequency to target FPGA and power analysis was done

Power analysis report was obtained for SPARTAN 3A with low speed, high speed device and SPARTAN 3E with low speed, high speed devices. Power analysis report for the proposed architecture is shown in Table III.

Table III
Power Analysis Report

Device	Frequency (MHZ)	Power Consumption(W)	
		Proposed DPWM	High Frequency DPWM
SPARTAN 3A (XC3S50A-4tq144)	6	0.01479	0.01486
	12.5	0.01544	0.01549
	15	0.01569	0.01586
	25	0.01668	0.01696
SPARTAN 3A (XC3S50A-5tq144)	6	0.01480	0.01488
	12.5	0.01544	0.01561
	15	0.01569	0.01561
	25	0.01569	0.01702
SPARTAN 3E (XC3S100e-4tq144)	6	0.01479	0.01482
	12.5	0.01544	0.01549
	15	0.01567	0.01575
	25	0.01666	0.01678
SPARTAN 3E (XC3S100e-5tq144	6	0.01479	0.01481
	12.5	0.01543	0.01548
	15	0.01567	0.01574
	25	0.01666	0.01676

Proposed DPWM architecture consumes less power as compared to High frequency DPWM architecture. In proposed method the Gray counter was used which negligible power consumption as compared to binary counter has used in High Frequency DPWM. The comparator used in High frequency DPWM also contributes to significant amount power consumption.

VI. CONCLUSION AND FUTURE WORK

In this paper a new DPWM architecture was presented developed with VHDL language and PWM signals are generated using 4 bit Gray counter and One hot encoder .

The proposed PWM was implemented in SPARTAN 3A FPGA which uses the DCM resource available in FPGA. The external clock frequency was multiplied with DCM and given to the system. This DPWM architecture can be used as digital controllers for high frequency switching converters. Power Analysis report was obtained for the both techniques with different target FPGA with different input clock frequency and tabulated. In this proposed method gray counters and one hot encoder circuit is used which reduces the power as compared to High Frequency PWM Generator which uses binary counter and comparator.

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