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Low Power High Speed Ternary Content Addressable Memory

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Abstract: ***Compared to Binary Content Addressable Memory (BiCAM) there are many applications for Ternary Content Addressable Memory (TCAM) as a search engine. But TCAM consumes more power than BiCAM. So, the saving of TCAM power consumption is the main objective of numerous designs. Precharge phase of the TCAM leads to more power consumption. Newly, a precharge free NOR type BiCAM has been suggested but it takes more time for its operation. Here, precharge free high speed NOR type TCAM is proposed. The proposed TCAM architecture takes power same as precharge free NOR type TCAM but its delay has been reduced by 84% . Simulations performed with cadence 45-nm technology at the supply voltage of 1V.***

Index Terms: Matchline Structure, NOR type TCAM , Precharge, Ternary CAM.

I. INTRODUCTION

The development of the world is based on agriculture, industry and service sectors. For the sake of information, these three sectors depends on internet. Either as an individual or an organization, internet users demands for high speed. The performance of searching algorithms decides the Speed of the internet. But speed of software based search algorithms is not sufficient for most of the applications. So hardware search engines are required for high speed applications. Earlier, traditional memory elements are only used for this purpose. But traditional memory elements gives content as an output by taking its address location as input. To specify the address of the desired content, Content Addressable Memories (CAMs) are used. CAM gives address as an output by taking content as an input. CAMs are used in network router, cache memories [4]-[7]. Area, Power and speed are the key factors for any hardware design. CAM designers objective is to decrease the power depletion and to increase the search speed. Traditional TCAM is shown in Fig.1 [3] . In TCAM, information kept in rows and hunt happens in parallel. Content is the input and address is the output for Ternary Content addressable memory. If stored data is same as the hunt data then it returns the address of the content.

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A mismatch or match information is sensed by the Match line amplifier (MLSA). As presented in Fig. 1, all TCAM cells in a row is coupled to same matchline (ML). All matchlines are initially kept at high voltage. ML value remains at high level if there is a match. Or else the particular matchline discharges. To perform a different search, again MLs must be at high level.

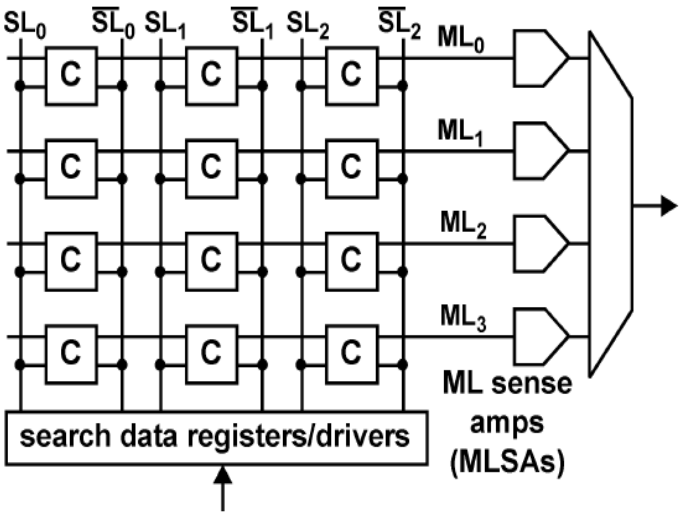

Fig.1: TCAM Architecture

TCAM cells comes under NAND & NOR category. NOR type TCAM cell offers high speed but needs more power where as NAND style TCAM cells consumes less power but it offers low speed. NOR style cells are chosen compared to NAND type. NOR category TCAM ML structure and TCAM cell is presented in Fig 2. Here TCAM cells are coupled in parallel. Traditionally, TCAM operation is divided into three phases. I.e. data write , matchline precharge, and data search. Initially all matchlines are kept at high voltage by keeping "pre" value at logic-0. Matchline voltage falls to 0 V , when there is a mismatch. So for every different search, matchlines are needed to charge to high voltage. Thus, the repeated charging and discharging occurs in content addressable memories. This causes more power dissipation. NOR style TCAM cell & its encoding is presented in Fig. 3 and Table I respectively. TCAM cell is used to store two bits. Two bits are essential to place logic-0, logic-1 & don't care(X). Thus TCAM cell needs two SRAM cells. As shown in figure 3, TCAM cell needs two Static RAM cells and four nMOS transistors. In TCAM, a logic level "0" is stored by maintaining C = 0 and D = 1, Logic "1" by maintaining C =1 and D = 0 & don't care by maintaining C = 1 and D = 1. At this point D= 0 and C = 0 is an unused state.

In TCAM, logic "0" is searched by keeping SL = 0 & $\overline{SL}$ = 1, Logic "1" by keeping SL = 1 & $\overline{SL}$ = 0 & don't care (X) by setting SL = 1 & $\overline{SL}$ = 1 . During precharge phase ML value is high. During evaluation phase, If C = 0 , D = 1 and SL = 0 then M_2, M_3 is in OFF state and M_1, M_4 is in ON state.

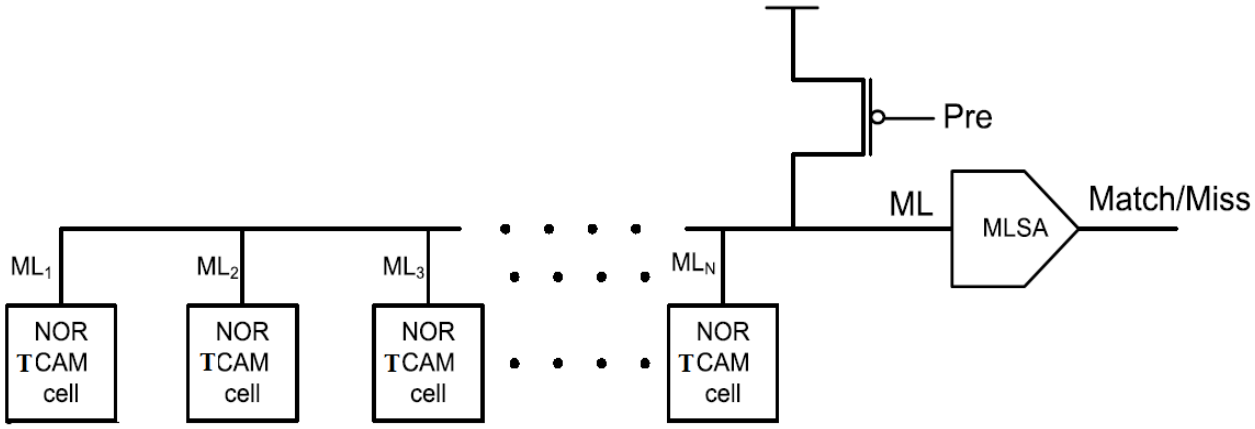

Fig. 2: NOR type matchline TCAM

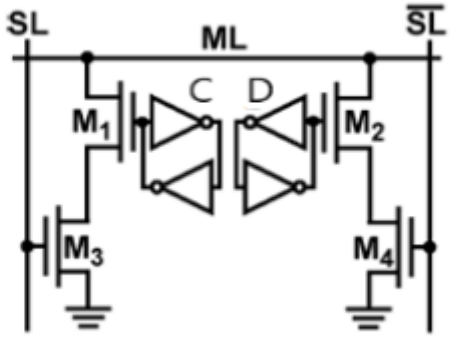

Fig.3: NOR style Ternary CAM cell

Table I: Encoding of NOR cell

Stored Value	Stored C	Stored D
0	0	1
1	1	0
X	1	1

Here there is discharging path for ML which results match case. Similarly, If C = 0 , D = 1 & SL = 1 then M_1, M_3 transistors are in ON state and M_1, M_4 transistors are in OFF state. Here ML discharges through M_1, M_3 transistors which results mismatch. To perform a new search, again ML requires to be charged to high voltage. Precharge phase causes more power dissipation. Precharge phase is the major constraint to the power dissipation. Recently, precharge free Binary CAM structure[2] and self controlled precharge free Binary CAM structures[1] have been presented. Here low power high speed Ternary CAM structure is proposed.

II. LOW POWER TCAM

Precharge free TCAM (PF-TCAM) cell is presented in Fig 4. As like conventional TCAM cell, PF-TCAM cell is also consists of two SRAM cells & four nMOS transistors. To keep the information in cells of PF-TCAM, write enable (WE) must be high. Q1 & Q2 transistors are in ON state when WE is active and the information bit is loaded into the cell. Logic '0' is kept in the cell by keeping WE= 1, D = 1 and C = 0 . Similarly, logic '1' is stored in cell by setting WE =1, D =0 and C = 1 & don't care by keeping WE = 1,D = 1 ,C = 1. If D is '1' and C is '1' then don't care(X) is placed in TCAM. To hunt for logic '0', set SL = 0 and $\overline{SL}$ = 1. Henceforth Q3 transistor OFF & Q4 transistor is ON state. Thus ML level is high since D is high. This one shows match. Likewise, If search for logic '1' happens in the same case by setting SL = 1 and $\overline{SL}$ = 0. Now Q3 transistor ON and Q4 transistor in OFF state. Thus ML level is high since C is at high level. Here there is no need of Pre charging of ML. ML value is decided by input logic levels.

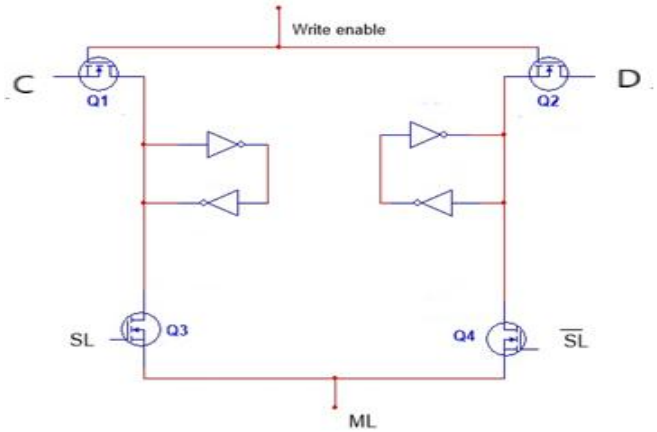

Fig.4: PF- TCAM cell

TCAM without precharge logic is shown in Fig.5. PF-TCAM action is divided

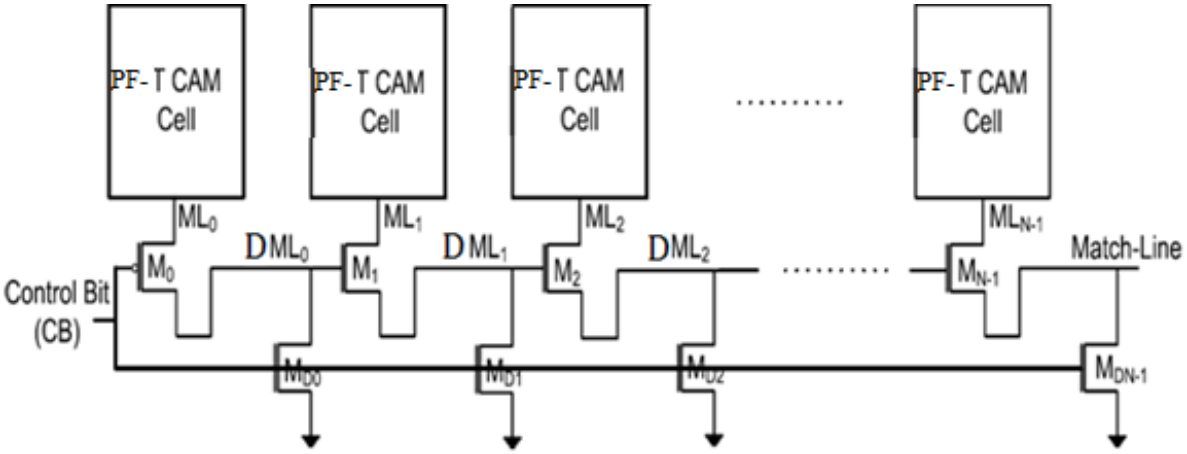

Fig5: PF-TCAM

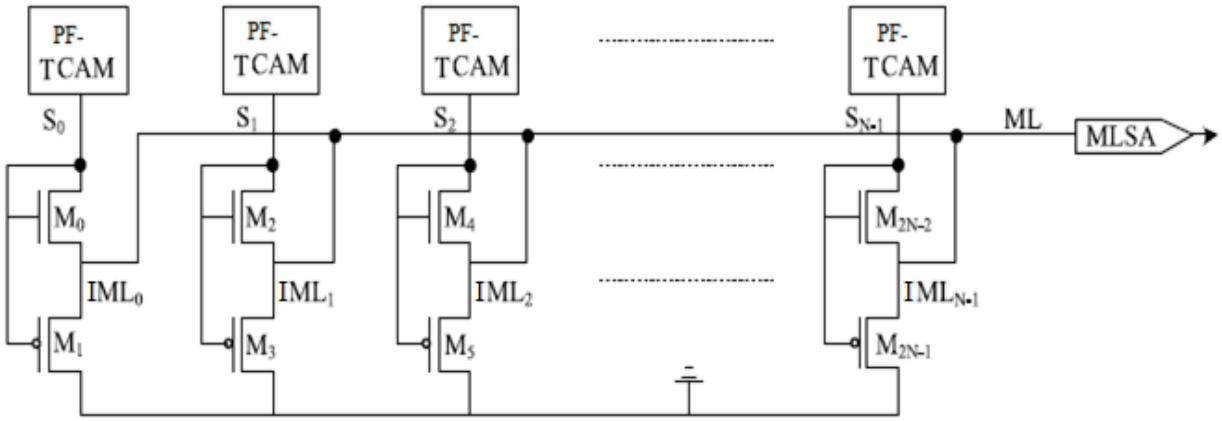

Fig6 : Proposed PF-TCAM

into two phases, i.e. data write and data search. Search operation begins by setting control bit is logic '0'. For logic '0' , M_0 is in ON state and M_{D0}, M_{D1}……. M_{DN-1} is in OFF state. Consider a two bit data for explanation. M_{L0} is in high state when first bit matches. Because of the pass transistor action of M_0, DML_0 is also high so M_1 is in ON state. If second bit is also matches, then DML_1 is in high state, so matchline is said to be in high state which indicates data match. If first bit match and second bit mismatch occurs, then ML_0 , DML_0 is in high state but DML_1 is in low state because ML_1 is in low state. It results data mismatch. Similarly, If first bit mismatch and second bit match occurs, then ML_0 , DML_0 is in low state and DML_1 is also in low state because M_1 is in OFF state. It also results data mismatch. If both bits does not match, ML_0 , ML_1 ,DML_0, DML_1 is in low state which indicates data mismatch. It offers low power dissipation due to the absence of precharge phase. But this structure increases the delay because control bit is given to the first cell. one cell has to wait for the result of its previous cell. if 't' is the delay of one cell , for 'n' cells the delay could be 'nt'. It causes performance degradation of ternary content addressable memory.

III. LOW POWER HIGH SPEED TCAM

Main reason for the reduction of speed is the usage of control bit (CB) in PF-TCAM architecture. In PF-TCAM structure, the cells are interdependent. This can be corrected by making the cells independent. Proposed PF-TCAM without control bit is shown in figure 6. Here M_0, M_2 , M_4, …M_{2N-2} are nMOS transistors and M_1, M_3 , M_5, …M_{2N-1} are pMOS transistors. S_0, S_1 , S_2 ,…..S_{N-1} are the status values and IML_0, IML_1,….. IML_{N-1} are the matchline values of PF-TCAM cells respectively. Here IML_0, IML_1,….. IML_{N-1} are all connected to matchline(ML). Proposed PF-TCAM action is also divided into two phases, i.e. data write and data search. As like earlier, Consider a two bit data for explanation. S_0 is in high state when first bit matches. As S_0 is high, M_0 is in ON state and M_1 is in OFF state so because of the pass transistor action of M_0, IML_0 is also high. If second bit is also matches, then S_1 is in high state, so M_2 is in ON state and M_3 is in OFF state, results IML_1 is also high. Hence matchline (ML) is said to be in high state which indicates data match. If first bit match and second bit mismatch occurs, then IML_0 is in high state but IML_1 is in low state because M_3 is ON . Here ML is coupled to ground,It results data mismatch. Similarly, If first bit mismatch and second bit match occurs, then IML_0 is in low state and IML_1 is also in high state because M_3 is in OFF state. It also results data mismatch. If both bits does not match, S_0 , S_1 ,IML_0, IML_1 is in low state which indicates data mismatch. In the proposed structure, the operation of TCAM cells are independent. One cell need not wait for the previous cell data. if 't' is the delay of one cell , for 'n' cells also the delay could be 't' only.

IV. RESULTS

The proposed PF-TCAM and conventional PF-TCAM were implemented for 3 bits with the help of cadence 45nm technology at the source voltage of 1V. Waveforms of conventional PF-TCAM and suggested PF-TCAM are shown in figures 7 and 8 respectively. Waveforms shows that the average power depletion of proposed PF-TCAM is same as conventional PF-TCAM and that is 42.8 µW. Delay of conventional PF-TCAM is 1.84 ns and for proposed PF-TCAM is 0.29 ns.

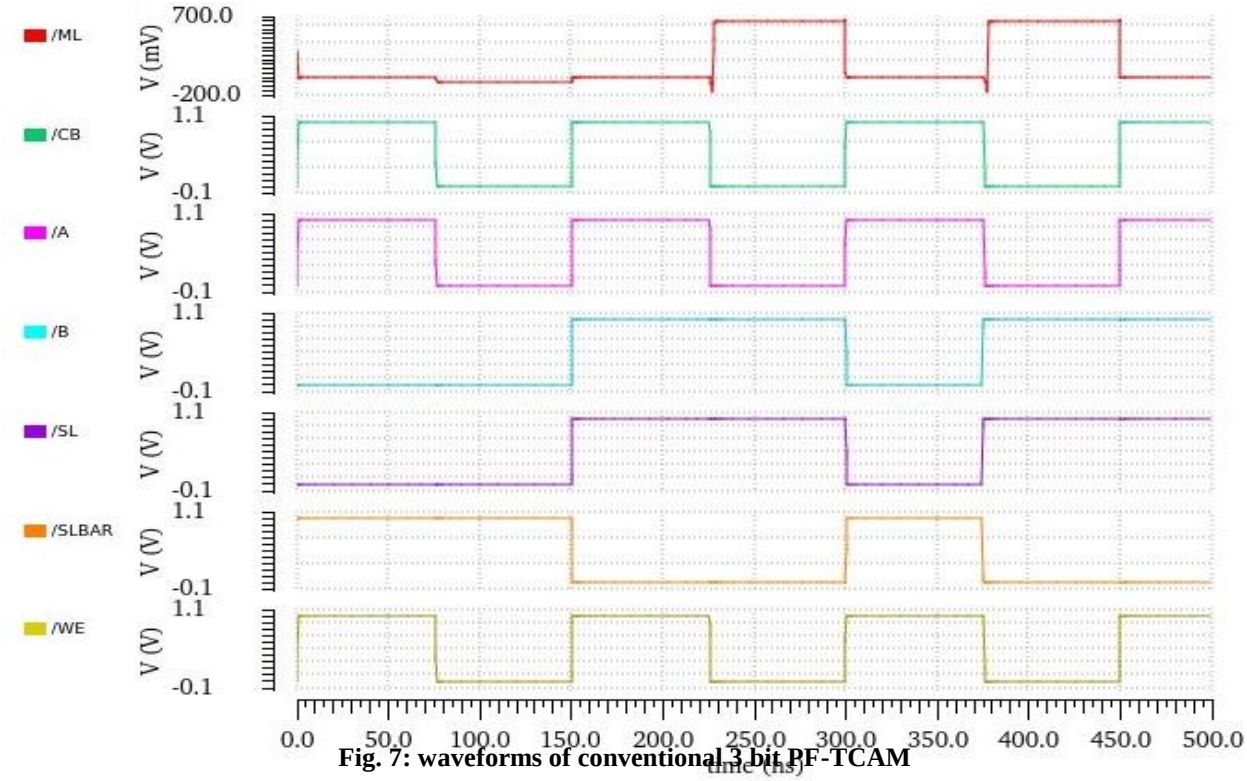

Fig. 7: waveforms of conventional 3 bit PF-TCAM

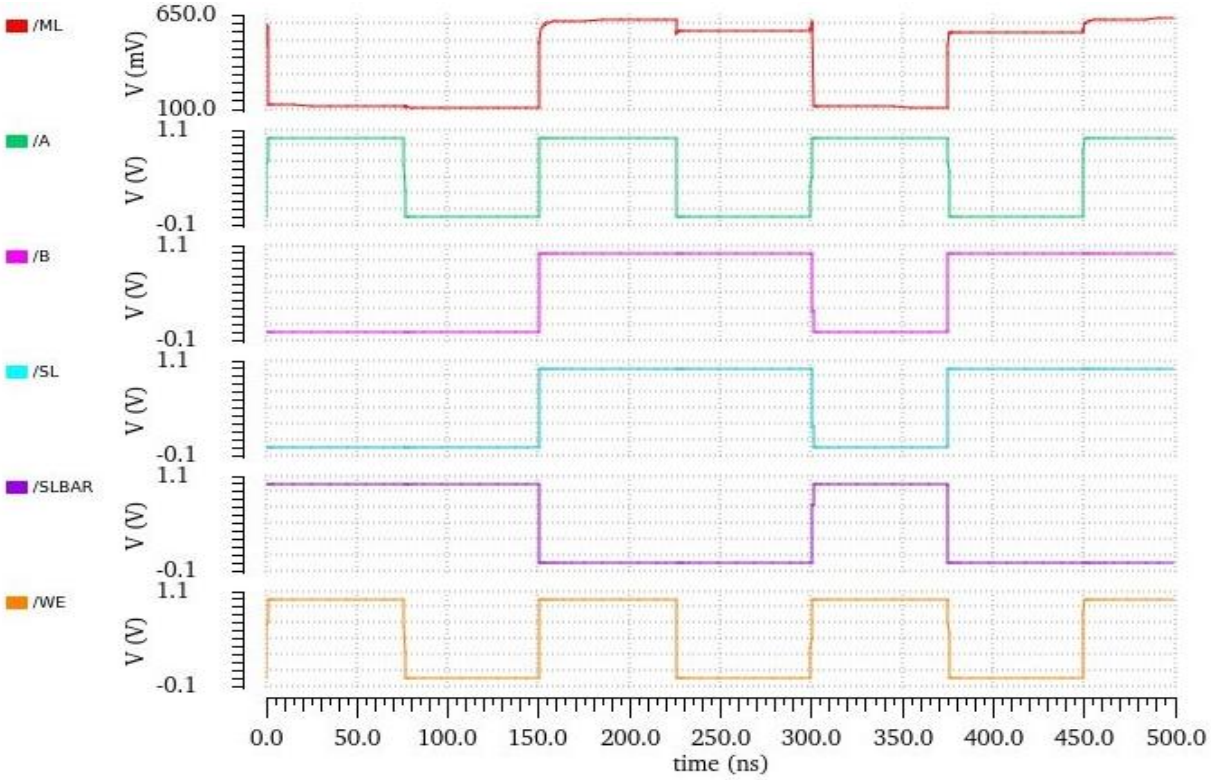

Fig. 8: waveforms of proposed 3 bit PF-TCAM

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V. CONCLUSION

Conventional NOR type 3 bit PF-TCAM is computer-generated and detected that it has added delay. The planned 3 bit PF-TCAM is also simulated using cadence at 1 V supply voltage and observed that its delay is 84% lesser than the conventional. Power dissipation of both the circuits are same.

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