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Design and Analysis of Gate All Around Tunnel FET based Ring Oscillator Circuit

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Abstract: ***In this work, we have designed and simulated a Gate All Around TFET (GAATFET) based 3 stage ring oscillator circuit and compared its performance with the CMOS based counterpart. The results of SPICE simulations indicate that GAATFET based ring oscillator circuit consumes 3.5 times lower power consumption in active mode than CMOS based ring oscillator. However, 0.43 ns and 0.17 ns of propagation delay is observed for GAATFET based ring oscillator and CMOS based ring oscillator circuit respectively. The obtained output waveform frequency for CMOS based ring oscillator is 2.5 times higher than the GAAATFET based ring oscillator. Further, undershoot is also investigated and it is found that the amplitude of undershoot in case of GAATFET based oscillator is roughly 6.5 times more as compared to CMOS based counterpart. The undershoot and delay observed in case of GAATFET based ring oscillator can be over-shaded by the fact that it has lower active power consumption than the CMOS based ring oscillator. Simulation results signify that GAATFET based ring oscillator can be deployed in future low power VLSI circuits and systems.***

Index Terms: Tunnel FET, Ring Oscillator, Gate All Around, Low power, Analog performance.

I. INTRODUCTION

Continuous device miniaturization of conventional MOS devices leads to increase in the leakage power consumption along with the short channel effects (SCEs). Further scaling will cause more degradation. There were needs to find the alternative device that can be fabricated using similar processes which were used to fabricate MOSFETs thereby ensuring continuous device miniaturization. Tunnel FET emerged out as a strong candidate for future device scaling. Its band to band tunneling charge injection mechanism makes it a replacement of CMOS devices. Tunnel FET inherit unique properties like < 60 mV/decade sub-threshold slope, low leakage current, high ION/IOFF ratio [1]. Si-based Tunnel FET have the drawback of low ON state current due to large tunneling distance and high band gap. It is quite evident from the literature that, Tunnel FETs ON current enhancement can be achieved by increasing the electric filed across the junction, using low band gap materials, high-k dielectric material, junction less and silicon thin body [2-12]. The ON current enhancement in sandwiched tunnel barrier FET (STBFET) is comparable to the CMOS counterpart with improved sub-threshold slope and good output saturation mechanism which makes it a fairly good candidate for analog circuits [8]. Further TFET is also a victim of the ambipolar effect which contribute its part in enhancing the overall leakage current and also leakage power. In order to mitigate the ambipolar conduction in TFET, lightly doped drain and drain/gate underlapping device engineering is done [13]. However analog prospects based on the GAATFET is still a lagging area, specifically ring oscillator which is the main source of signal generator for analog applications [14-15]. In literature, enough exploration has been done in all fronts which includes device engineering, device circuit interaction for digital applications focused on low leakage power, hybrid device circuit interaction [16]. However little exploration is done for analog prospects specifically using the gate all around Tunnel FET (GAATFET) based devices [17]. GAATFET is most preferred device for low power applications because of its strong control over the electrostatic potential which is responsible for leakage reduction. In this work GAATFET based ring oscillator is designed using the device-circuit co-design approach and results are compared with MOSFET based ring oscillator circuit. The organization of the work is as follows: in section-II, device computational details are discussed along with important device parameters like device dimensions, doping concentration and other related parameters. In section-III results and discussion are presented and finally in section-IV conclusions are drawn.

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II. DEVICE DESIGN & SIMULATION SET-UP

a) Gate-All-Around Device Structure

It is well known fact that TFETs designed in double gate configuration has better control over the channel electrical properties as compared to the TFET device designed in single gate configuration. Another promising configuration that exhibits best control over the channel electrical properties is known as GAATFET. This device configuration has gate covering the entire channel region and hence it possesses better control over the channel as compared to any other TFET configuration. GAATFET provides higher ION/IOFF ratio and also the sub-threshold slope of less than 60 mV/decade. The device structure and front view of the single gate material GAATFET is shown in Fig.1. To enhance the ON state current of the GAATFET, work function engineering using three different metals is explored.

The device structure for work function engineering and device schematic is shown in Fig.2. The gate material is divided in three parts namely: M1, M2 and M3 with works functions ϕ_1, ϕ_2 and ϕ_3 respectively. This device structure is known as Tri Material Gate Tunnel FET and is typically a barrier controlled TFET device. The energy barrier depends on the combination of the work unction of the materials used in the gate region. The value of ϕ_1 is kept higher than ϕ_2 and ϕ_3 value is kept lower than ϕ_2. Keeping ϕ_1 high leads to enhancement of electric field.

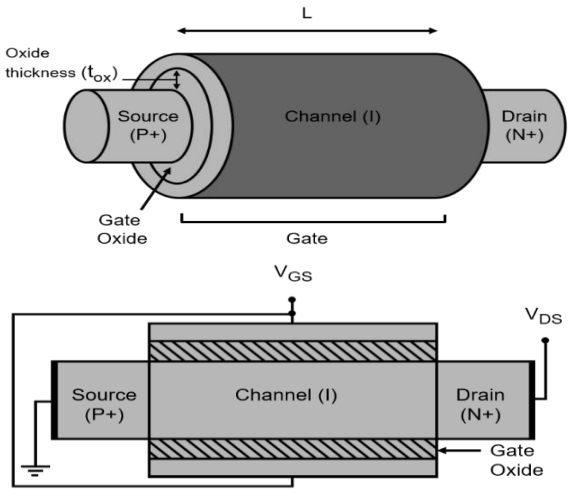

Fig.1. Gate All Around TFET device designed using single material gate

In order to simulate the device on TCAD tool the first step is to calibrate the tunneling model results with the fabrication results available at the same technology node. In this work the Kane's tunneling model is calibrated against the experimental data published in [15]. The calibrated curve is shown in Fig.3 which signify that there is a close match between the experimental data and the simulation thereby validating the tunneling model used.

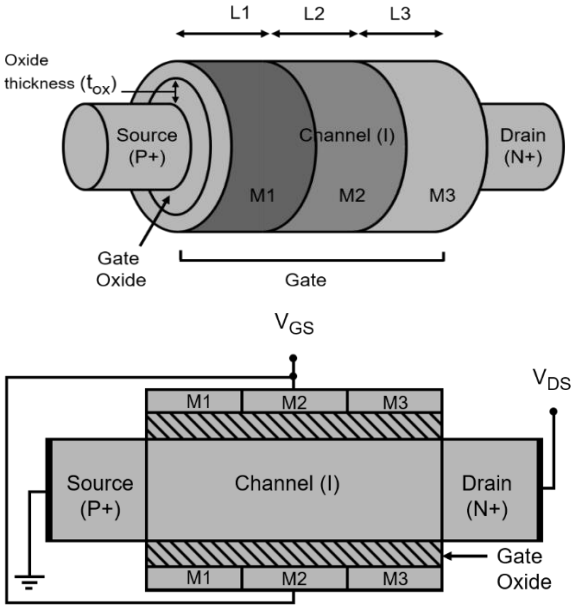

Fig.2. Gate All Around TFET device designed using triple material gate

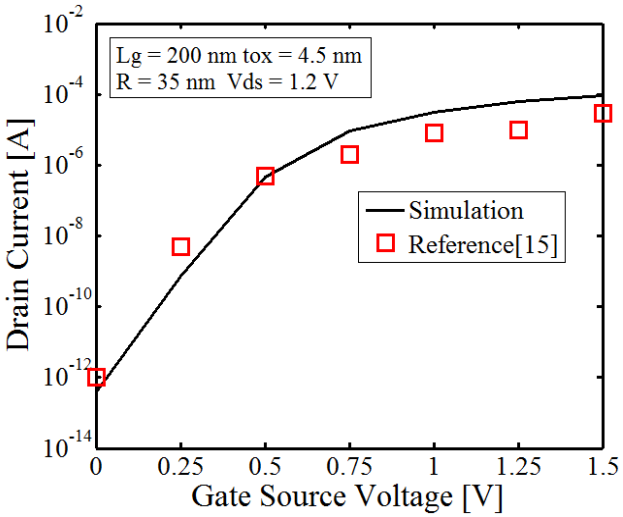

Fig.3. Validation of the simulation results with the experimental data

b) Proposed TFET Device

In this work we have designed NTFET and PTFET device's in Gate All Around configuration using three different materials for the gate region similar to a traditional TMGTFET device structure. To enhance sub-threshold slope of the device, high K dielectric is used beneath the M1 region and on the remaining part of the gate SiO_2 is used as dielectric. The device structure of HDTMGTFET device is shown in Fig.4.

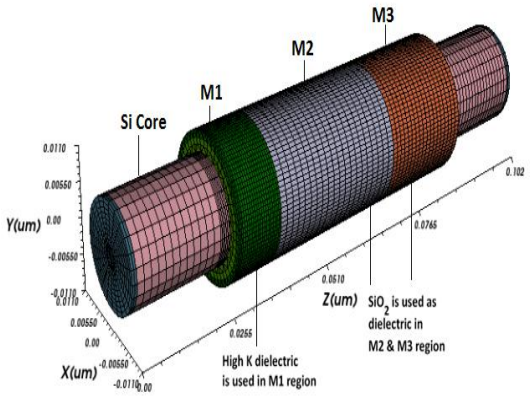

Fig.4. Proposed N type HDTMGTFET device structure

This novel configuration known as HDTMGTFET device as proposed in [17] gives slightly high drive current and better sub-threshold slope than TMGTFET device. However, the leakage current reduction is also achieved in HDTMGTFET. The device physical parameters are listed in Table-1. The better performance achieved in case of HDTMGTFET is because of the high-K dielectric material. The electric field across the junction tightened the control across the tunneling junction which leads to reduction in the tunneling width. Due to high electric field more band lowering and overlapping occurs, which is the reason behind the increased drive current of the HDTMGTFET device structure.

Table-1: Device important device physical parameters

Parameter	NTFET device	PTFET device
Source Doping (Ns)	1e20 (p-type)	1e20 (n-type)
Drain Doping (Nd)	1e17 (n-type)	1e18 (p-type)
Intrinsic Doping (Ni)	1e16	1e16
L_g (nm)	60	60
T_{ox} (nm)	2	2
ϕ_1, ϕ_2, ϕ_3 (eV)	4.4, 4.8, 4.6	5.0, 5.4, 5.2
Radius of Silicon Core (nm) (R)	8	20
High-K	7.9	21
Gate Source Under-lap (nm)	0	4

The output characteristics of the proposed NTFET and PTFET devices is shown in Fig.5. It can be inferred from Fig.5 that, both NTFET and PTFET devices gives the extremely low leakage current.

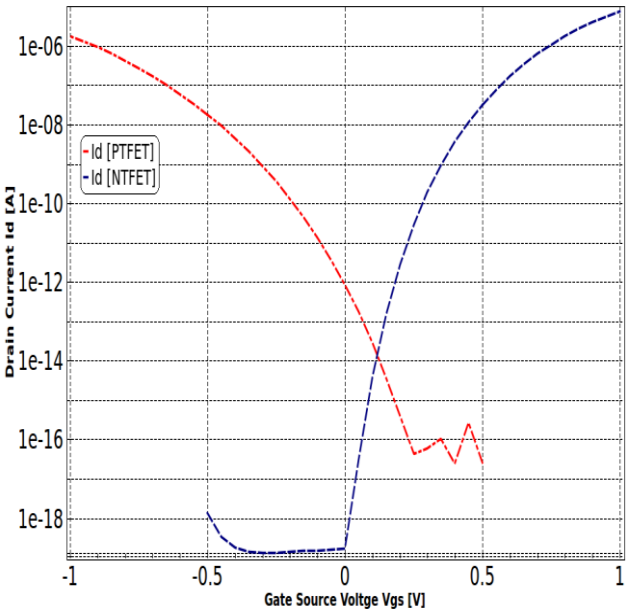

Fig.5. Transfer characteristics of NTFET and PTFET device

III. RESULTS AND DISCUSSIONS

a) Ring oscillator: An overview

To analyze the performance of 3-stage ring oscillator circuit which is designed using the proposed TFET devices, look up table based Verilog-A modeling approach is used. This model is used in Symspice tool for performing ring oscillator simulations and is one of the most widely used models for analyzing the feasibility as well as the success of an IC during fabrication. To design the ring oscillator, odd number of inverters are connected back to back so as to form a positive feedback closed loop system with high gain. Circuits such as VCO and PLL makes use of ring oscillator circuit to gather important information like the delay time per gate which is crucial for designing these high speed clock circuits. The schematic diagram of a three stage ring oscillator is shown in Fig.6.

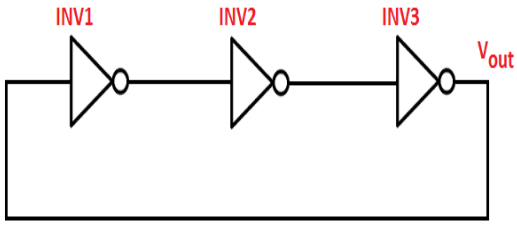

Fig.6. Three Stage Ring Oscillator

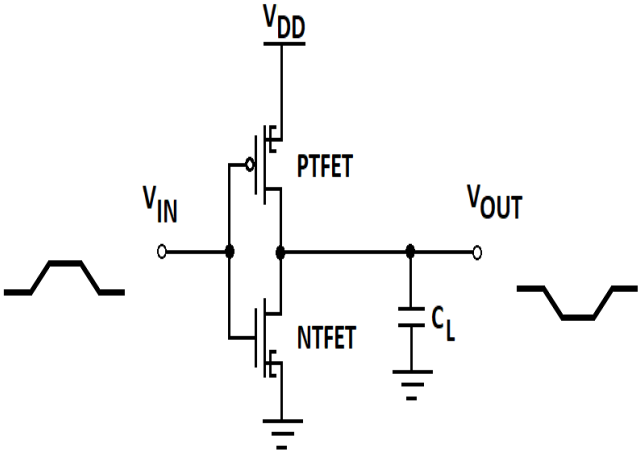

Fig.7. Tunnel FET based Inverter Circuit

INV3 out is fed back to the input of INV1 and V_{out} gets inverted after every cycle thereby resulting in oscillations. It is a point to note here that there is always a finite propagation delay that is associated with each inverter and it is because of this delay time the entire circuit oscillates at a particular frequency (f). The frequency of oscillation depends on the number of stages (n) of the ring oscillator and the delay time (Tp) of the inverters. The oscillation frequency (f) is given by

$$f = \frac{1}{2nT_p}$$

Inverter circuit is the building block of the ring oscillator and it can be easily designed using both NTFET and PTFET devices as shown in Fig.7 shows the performance analysis of the TFET based ring oscillator circuit.

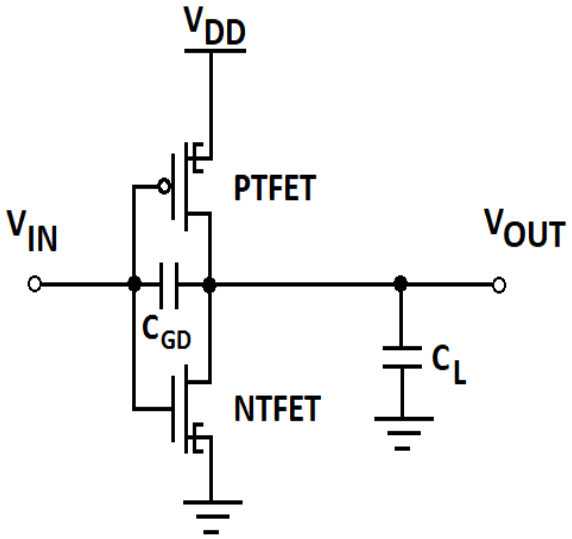

Fig.8. Miller Capacitance CGD (C_M) in TFET based Inverter Circuit

b) Undershoot and Overshoots in TFET based Circuits

The problem of undershoot and overshoot that comes into picture during transient simulation occurs mainly because of the gate-drain capacitance that connects the input node and output node as shown in Fig.8. This capacitance is popularly known as miller capacitance, denoted by C_M. When the gate input is at logic '0' then both C_L and C_{GD} will charge towards V_{DD} and low to high transition of the gate input will not cause much charge sharing between these two capacitances. On the other hand, when the gate input is at logic '1' then output capacitor C_L discharges through the pull down NTFET device which is in the ON state while the miller capacitor C_{GD} charges via NTFET device. During high to low transition of the gate input charge sharing takes place between C_{GD} and C_L because of the potential difference between the two capacitor voltages and this leads to large undershoot peaks during transient simulations. The situation during high to low transition of the gate input is depicted in Fig.9 which clearly shows the charge sharing phenomenon that takes place in the tunnel FET based inverter circuit leading to undershoot peaks.

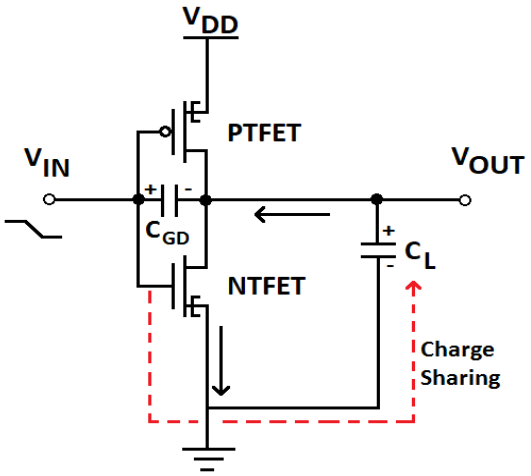

Fig.9. Charge Sharing leading to Undershoot Peaks

The principle of charge conservation can be exploited to calculate undershoot and overshoot as follows:

$$C_L V_M + C_M (V_M - V_{DD}) = (C_L + C_M) V_{DD}$$

$$V_P = V_M - V_{DD}$$

$$V_P = \left(\frac{C_M}{C_M + C_L} \right) V_{DD}$$

The percentage overshoot is calculated as:

$$100 * \left(\frac{V_M - V_{DD}}{V_{DD}} \right)$$

Similarly, the undershoot peak is calculated as:

$$V_V = -V_{\min}$$

$$V_V = \left(\frac{C_M}{C_M + C_L} \right) V_{DD}$$

The percentage undershoot is calculated as:

$$100 * \left(\frac{-V_{\min}}{V_{DD}} \right)$$

c) Three Stage Ring Oscillator

Fig.10 shows the schematic diagram of three stage ring oscillator that is designed using tunnel FET device. Load capacitance is connected at the output node of each inverter in order to reduce the undershoot and overshoot peaks that occurs during transient simulations.

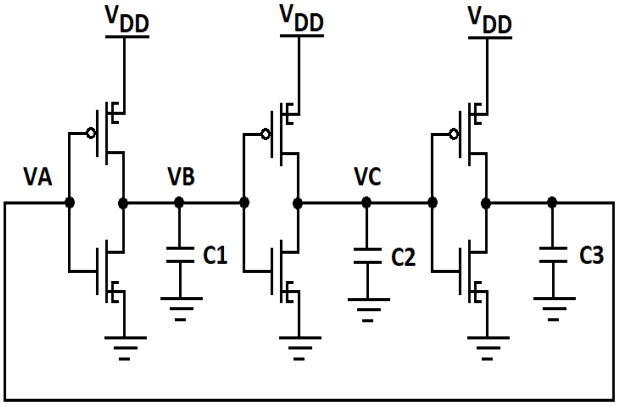

Fig.10.GAATFET based Three Stage Ring Oscillator Circuit

The ring oscillator circuit has been simulated using Symspice tool using Verilog-A model. In order to perform the transient simulations a piece wise linear waveform (0 to 1V) with rise time of 10 ps is applied to the supply voltage V_{DD}. Simulation run is carried out for 1 ns and from the simulation waveforms shown in Fig.11, it is quite clear that oscillations are seen in between 0 to 300 ps with undershoot peaks.

Enhanced Miller capacitance is the main reason for the observed undershoot peaks in the transient simulation waveforms. Miller capacitance is an important parameter that can lead to overshoot and undershoot peaks however the percentage of undershoot is more as compared to the overshoot.

d) Ring Oscillator Performance Analysis

The performance of 3 stage ring oscillator designed using TFET device has been compared with MOSFET based ring oscillator that is designed at 65 nm. PTM model files are used for carrying out circuit simulations of the MOSFET based ring oscillator circuit. In order to compare the performance of these two circuits the following parameters are kept constant: supply voltage is kept at 1V and the same piece wise linear waveform is used for the supply voltage V_{DD}. The main performance parameters that are extracted from the circuit simulation includes: Frequency of operation, Propagation delay, Power consumption and the percentage undershoot observed during transient simulations. The performance of 3 stage ring oscillator designed using TFET device has been compared with MOSFET based ring oscillator that is designed at 65 nm technology node. PTM model files are used for carrying out circuit simulations of the MOSFET based ring oscillator circuit. Fig.12 shows the transient analysis waveform output of the MOSFET based ring oscillator circuit. Table-2 shows the comparative analysis results of the ring oscillator circuit that is designed using tunnel FET and MOSFET device.

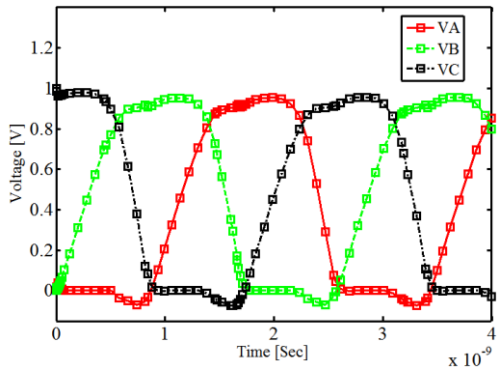

Fig.11.Transient Simulation GAATFET based Three Stage Ring Oscillator Circuit

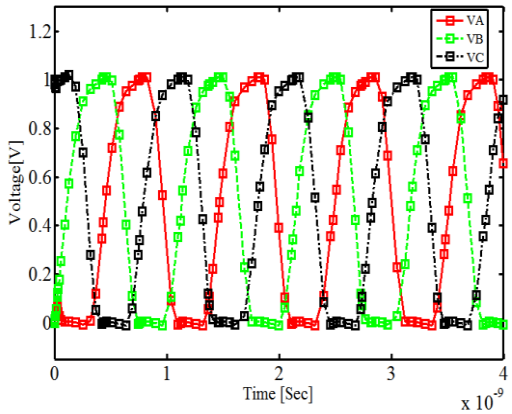

Fig.12. Transient Waveform MOSFET based Three Stage Ring Oscillator Circuit.

Table-2: Ring Oscillator Performance Comparison

Parameter	3 stage TFET based Ring Oscillator Circuit	3 stage MOSFET based Ring Oscillator Circuit
Supply Voltage (Volts)	1.0	1.0
Frequency of Operation (GHz)	0.39	0.98
Delay (ns)	0.43	0.17
Power Consumption (uW)	1.53	3.52
% Undershoot Observed	6.76	1.12

It is quite clear GAATFET ring oscillator circuit exhibits better power performance than MOSFET based counterpart. This is mainly due to the low OFF state current of the tunnel FET device. TFET based ring oscillator achieves 2.3X times power saving in active mode than MOSFET based ring oscillator. Tunnel FET based ring oscillator shows large undershoot peaks due to miller effect. The frequency of output transient waveform obtained in MOSFET based ring oscillator circuit is 2.5 times more as compared to TFET based ring oscillator circuit. It is due to high drive current of MOSFET device which leads to fast transient response leading to high frequency of operation. This is evident from the fact that that the propagation delay per stage in case in case of TFET based ring oscillator is 2.5 times than MOSFET ring oscillator. In order to ensure that TFET based ring oscillator circuit defined using GAATFET device outperforms MOSFET based ring oscillator it is required to boost the ON state current of the TFET device. This can be done by using low band-gap materials.

IV. CONCLUSION

In this work, GAATFET based ring oscillator is designed using the device-circuit co-design approach and results are compared with MOSFET based ring oscillator. TFET based ring oscillator achieves 2.3 times power saving in active mode as compared to MOSFET based ring oscillator circuit. Tunnel FET based ring oscillator shows large undershoot peaks due to miller effect. The frequency of MOSFET based ring oscillator circuit is 2.5 times more as compared to TFET based ring oscillator circuit. Further the propagation delay per stage in case in case of TFET based ring oscillator is 2.5 times more as compared to MOSFET based counterpart. In order to ensure that TFET based ring oscillator circuit designed using GAATFET device outperforms MOSFET based ring oscillator it is required to boost the ON state current of the TFET device.

This can be done by using low band-gap materials. GAATFET based ring oscillator is strong candidate for low power applications.

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