Ultra-Wide Band LNA Design using Active Inductor with Modified Noise Cancellation Technique

Najeemulla Baig, Fazal Noorbasha

Abstract: An Ultra-Wide Band (UWB) Low Noise Amplifier (LNA) is affective in deciding the chip size and in the implementation cost at Radio Frequency applications. The proposed LNA design with an active inductor is a different solution to trounce the habit of passive inductors to cut the chip area. Designed in 90-nm CMOS process, a voltage gain of 9dB to 15.5dB for a supply voltage of 0.9v to 1.8V with a smallest Noise Figure (NF) of 5.7dB is achieved by the LNA, with low power utilization and at 2.40 GHz, with 345um² of chip area.

I. INTRODUCTION

LNA is very essential in Radio Frequency (RF) receiver structure as this LNA gets fragile signals from an antenna and passes the enlarged signal to the consequent circuits. Since a relatively frail signal is received by the antenna, a good gain and Noise Factor (NF) is necessary. Thus the requirements of the LNA are both elevated gain and little noise to guarantee good concert of the receiver. In the present market scenario different communication standards are demanded for wireless communication. A particular wireless communication gadget merges a lot of features as possible; thus, it became very important to design a multiband LNA with flexibility. In designing reconfigurable receivers LNA with wide band characteristics is a key construction block. The designed distributed amplifier works with wide frequency band [1] but consumes more power and occupies significant silicon area. The noise performance of wideband LNAs [2], utilizing a feedback resistor is degraded due to thermal noise added by the feedback resistor. The passive inductor in LC band-pass filter which is used at the input of wideband LNA [3] occupies large silicon area in chip design. We can obtain wide input matching by using common-gate (CG) configuration [4]. There is no inductor at input of CG amplifier. To design multiband LNA circuits multiple passive inductors are used with switches to choose the preferred frequency band but, Passive inductor usage has limited the concert as they occupy larger silicon area with fixed values of inductance and Q-factor.

Using active inductors we can achieve less significant die area. Additionally, it is capable of tuning the inductance and Q-factor values. Active inductor design results in increased power dissipation, with higher noise but gives a divergent scheme to design SOC. To limit the noise by allowing considerable power consumption we have to be careful in designing the CG-LNA. The plan to absorb the all out circuits framework in a solitary chip has given a decent bit of leeway to the manufacturer to have littler coordinated circuit (IC), diminished assembling cost and reduced silicon area. In[5], LNA is implemented using resistive shunt feedback with current reused technique to reduce power dissipation and noise-canceling technique to reduce noise factor, but in this LNA passive inductors are used which occupies large silicon chip area. In this work ultra wide band LNA is proposed with an active inductor which is a different solution to trounce the habit of passive inductors to cut the chip area. This paper is planned as follows. In section 2 CG LNA circuit design with active inductor will be described. Section 3 presents the proposed modified noise cancellation technique for CG LNA. Section 4 shows the simulation results, and then conclusion is followed.

II. CG LNA CIRCUIT DESIGN WITH ACTIVE INDUCTOR

2.1 CG LNA circuit design:

Fig.1 shows CG LNA architecture with active inductor, transistor M2 and M4 provide biasing value to transistors M1 and M3. M1 and M3 is the amplifier stage of LNA. This design proposed to use active inductor, Ls. Active inductor Ls is used to tune to control input impedance Zin. Common gate LNA design is carried out for an operating frequency (f0) equal to 2.4GHz and VDD equal to 0.9v.

![Fig.1. Architecture for CG LNA with active inductor](image-url)

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The transistors M1, M2, M3, and M4 widths are calculated for channel length equal to 100nm. By considering input impedance of CG LNA equal to 50Ω, the parameter value of source inductor Ls is calculated. This source inductor (Ls) equal to 16.9nH is implemented using active inductor topology; the active inductor design is given next.

2.2 Active inductor design:
Active inductor is structured by utilizing the gyrator-C topology to give the inductance. Gyrator-C is created by utilizing two amplifiers which are connected consecutively. The intrinsic capacitance from the amplifier is transformed into an inductive behavior by using the gyrator-C topology. The inherent capacitance from the amplifier is changed into an inductive behavior by utilizing the gyrator-C topology.

The gyrator-C topology is depicted in Fig.2. Common Gate LNA requires a single-ended active inductor.

Using a differential active inductor by grounding one output terminal to get single ended active inductor will waste silicon area. Hence single ended Abdullah Feedback Resistance Active Inductor [4] is used.

III. MODIFIED NOISE CANCELLATION TECHNIQUE FOR CG LNA:
Even though it is feasible to have lesser silicon chip area and tunable inductance with active inductor, trade off is done by presenting a higher noise and power utilization in the plan. By optimizing width of transistor the power dissipation’s optimized and employing of Noise reducing techniques can reduce the noise. The noise cancellation technique for CG

![Fig.4. small-signal equivalent circuit [4]](image)

![Fig.2. Basic Gyrator-C Topology [4]](image)

![Fig.3. Abdullah feedback resistance active inductor [4]](image)
LNA shown in fig.5 is modified further to reduce noise figure. Using this modified noise cancellation technique shown in fig.6 it is observed that a better S11 value is obtained which is very useful result obtained with the same gain and reduced noise figure, because differential output is taken.

Gain in this case is same as without noise cancellation technique with reduced NF of 6.77dB shown in Fig.10. We can further increase the gain by increasing the VDD supply voltage. In this case VDD used is 900mV, for low voltage applications.

In Fig.11, S-parameters with better values for S11, S12, and S22 are obtained which is very important at RF frequencies; if S11 is large, reflection coefficient is small which shows better input impedance matching and maximum power transfer takes place.

A measure of linearity is IIP3 is equal to -4.06788dB, which is shown in Fig.12. From the Fig.13 we can observe that the -3dB bandwidth is about 3GHz which is very wide that is the reason noise figure is also high. Layout diagram of CG LNA is shown in Fig.14.

### IV. SIMULATION RESULTS:

The proposed UWB LNA is designed in a TSMC 90 nm, 0.9 V CMOS RF process and simulated using CADENCE RF-spectre. In Table 1 the parameters of the LNA are listed.

<table>
<thead>
<tr>
<th>parameter</th>
<th>value</th>
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<tr>
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<tr>
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<td>646.62um/100nm</td>
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<tr>
<td>Lₛ</td>
<td>16.9nH</td>
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</tbody>
</table>

### 4.1 CG LNA with passive inductors

When noise figure (NF) is swept with respect to frequency in case of CG LNA with passive inductors we can observe in Fig.7 that at frequency equal to 2.4GHz noise figure is 1.608dB.

### 4.2 Common Gate LNA with active inductor without noise cancellation technique

A CG LNA utilizing active inductor without noise cancellation technique is shown in Fig.8. Because active inductor is used here noise figure is 7.16dB at 1.8V supply voltage as shown in Fig.9 which is higher than the common gate LNA with passive inductors. The voltage gain of this circuit is about 9dB.

### 4.3 Common Gate LNA with active inductor with noise cancellation technique
Ultra-Wide Band LNA Design using Active Inductor with Modified Noise Cancellation Technique

4.4 CG LNA with active inductor with modified noise cancellation technique

This modified circuit schematic shown in Fig.6 gives a better input impedance matching with S11 is equal to -20.13dB;

S12 is equal to -35dB which is shown in Fig.15. This value results in maximum power transfer at the input, when compared to the circuit shown in Fig.8. Input is not loaded by the gate of the output transistor because output of the Common gate LNA is connected to the input of the output transistor. The 3rd order input intercept point is equal to -3.57m dB.

Here Single ended active inductor is used, For Ls in the Common Gate LNA. The schematic diagram is shown in the Fig 16.

The size of active inductor layout for 16.4nH is 23µm*15µm approximately, whereas for passive inductor of same value it is 500µm*500µm. This gives a reduction in area occupied, by a factor of 724. From this we can understand that how much larger silicon area a passive inductor occupies when compared to active inductor.
V. CONCLUSION
This paper presents an UWB low-noise amplifier through modified technique for noise-cancellation with the 90nm CMOS process. It consists of a CG stage at the input and common-source stage for noise cancelation. Modified noise-canceling technique is used with active inductor to reduce silicon chip area required. The simulated results demonstrate that high and flat voltage gain of 32.4dB and S11 less than −10 dB within 3GHz bandwidth is archived by the proposed LNA. The chip area is reduced by a factor of approximately 724 by using the active inductor which is capable of tuning the inductance. From the results it can be concluded that the LNA planned is a right option for ultra wide band and multi-standard applications.

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