

Low-Power Adiabatic Computing with Modified Quasi Static Energy Recovery Logic of MQSERL 4x4 multiplier



M.Mailsamy, V.Rukkumani, K.Srinivasan, B.Sharmila

Abstract: This work depends on another methodology for limiting vitality utilization in semi static vitality recuperation rationale of Modified Quasi Static Energy Recovery Logic (MQSERL) circuit which includes enhancement by expelling the non-adiabatic misfortunes totally. Vitality recouping hardware dependent on adiabatic standards is a promising system driving towards low power superior circuit plan. The productivity of such circuits might be expanded by lessening the adiabatic and non-adiabatic misfortunes drawn by them amid the charging and recuperation tasks. In this paper, execution of the proposed rationale style is broke down and contrasted and CMOS in their agent inverters, entryways, flip- flop and snake circuits. Every one of the circuit was reproduced by test system of TANNER TOOL in 0.18 μ m innovation. In our proposed inverter the vitality proficiency has been enhanced to practically 30% and 20% up to 20MHz and 20fF outside load capacitance in contrast with CMOS and MQSERL circuits individually. Our proposed circuit gives vitality proficient execution up to 100 MHz and in this way it has ended up being utilized in superior VLSI hardware.

Index Terms: Component; Adiabatic logic; Power consumption; Quasi Static Energy Recovery Logic (QSERL); CMOS logic.

I. INTRODUCTION

With the developing prerequisite of convenient correspondence many research have been done to lessen vitality scattering [1]-[4], among them adiabatic rationale procedure [5] is extremely encouraging. In adiabatic circuits vitality scattering happens because of adiabatic and non-adiabatic misfortunes. On the off chance that we bring down the rate of charging, lesser measure of intensity is drawn from the source and lesser will be adiabatic misfortunes. Non-adiabatic misfortunes happen because of the voltage on.

The majority of the adiabatic circuits have these non-adiabatic misfortunes because of the voltage drop over the diodes or inadequate vitality recuperation. The essential thought for lessening adiabatic misfortunes is that; clock transient time T is kept a lot bigger than characteristic time consistent RCL of the gadget [6]. Non-adiabatic misfortunes are limited by recouping the vitality put away in load capacitances [7]. The vitality in charging the heap capacitances is recouped amid releasing and put away for reuse. In adiabatic rationale circuits time differing voltage supply is utilized so that the nodal capacitance are charged or released at a consistent current which makes voltage drop practically unimportant, while in CMOS rationale circuits we utilize steady DC voltage source. The word 'adiabatic' is utilized in a reversible thermodynamic process [8] where a change is done as such that no gain or loss of warmth or vitality happens. By making the change procedure moderate the warmth or vitality misfortune can be made just about zero in a perfect world. Lately numerous adiabatic rationale structures have been proposed which chip away at a similar hypothesis however have distinctive circuit structures and multifaceted nature. The semi static vitality recuperation rationale (QSERL) circuit [9] endeavors to diminish the disadvantages of the past vitality recuperation rationale (ERL) families because of its static rationale similarity circuit structure, decreased exchanging action and number of intensity tickers however it have downside of in-power and yield coasting due to the interchange hold stages.

Integral vitality way adiabatic rationale (CEPAL) gives enhancement to the QSERL circuit since it needn't bother with input manager to evacuate coasting yield which thusly enhances zone and power overhead [10]. Likewise its throughput is better (twice) than QSERL. Be that as it may, because of the additional MOSFET diodes in charging and releasing way somewhat bigger power dissemination than QSERL circuits happen. Because of these difficulties with detailed adiabatic rationale circuits [11-19] we propose altered semi static vitality recuperation rationale (MQSERL) circuit. MQSERL acquires every one of the upsides of as of late detailed QSERL circuits with extra enhancement in power sparing by decreasing the non-adiabatic misfortunes just as adiabatic misfortunes. We have planned and recreated different MQSERL based rationale circuits and their exhibitions have been assessed and contrasted and some detailed adiabatic circuits and traditional CMOS circuits. This paper contains four segments. Segment 1 bargains the presentation part.

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Segment 2 portrays the proposed vitality recuperation rationale (MQSERL) circuit and it's working. In area 3 we have reenactment results and dialog. The area 4 condenses the end.

II. PROPOSED ENERGY RECOVERY LOGIC CIRCUIT

2.1. ENERGY RECOVERY LOGIC CIRCUIT

The circuit of altered semi static vitality recuperation rationale (MQSERL) is appeared in Figure 1(a). It is made out of with two correlative sinusoidal power timekeepers (V_A and $V_{A_{bar}}$), a charging PMOS transistor (P1) whose door is associated by the power clock V_A , and a P-arrange in charging way, and a releasing NMOS transistor (N1) whose entryway is associated by the power clock $V_{A_{bar}}$, and a N-organize in releasing way. The power clock ($V_{A_{bar}}$) is in stage while the other clock (V_A) is 180 degree out of stage. The sinusoidal clock charges/releases the heap capacitance nearly gradually than the triangular or trapezoidal power timekeepers. We have talked about in past area that we can upgrade control productivity of adiabatic rationale circuits by guaranteeing that how gradually the nodal capacitances are charged or released in this manner control dissemination is limited by utilizing these sinusoidal tickers. The top to crest voltage of intensity tickers $V_{A_{bar}}$ and V_A is 1.8 V. The transistor (P1) in the draw up system and transistors (N1) in the draw down system are utilized rather than the diode (which was utilized in QSERL circuit) for lessening the non-adiabatic misfortunes. Power clock ($V_{A_{bar}}$) controls the ON and OFF time of transistor (N1) and (V_A) controls the ON and OFF time of transistors (P1). The perceptible wellspring of intensity dissemination in QSERL circuits was because of the MOSFET diode's limit voltage drop (which is non-adiabatic misfortune) though in the proposed MQSERL circuit, the principle wellspring of influence misfortune is because of the ON opposition of channels of MOSFET transistors P1 and N1 [12]. The hardships as a result of the ON impediment of P1 and N1 are on a very basic level lower than the mishaps in view of the limit voltage drop through diodes and all in all setbacks can also be brought somewhere near cutting down the charging speed. Along these lines by using transistors (P1 and N1), control spread is very diminished interestingly with the diode based circuits. At any rate we can't empty the power dissipating absolutely in light of the non reversible nature of the proposed circuit.

2.2. CIRCUIT OPERATION

The activity of the circuit is separated into two phases dependent on the supply clock phases, evaluation and hold. In assessment stage $V_{A_{bar}}$ step by step increments from low to high voltage while V_A bit by bit diminishes from high to low voltage, though in hold stage $V_{A_{bar}}$ bit by bit diminishes from high to low and V_A increments from low to high voltage as appeared.

In assessment stage, whenever yield hub (V_{out}) is at LOW rationale and the P tree is turned ON; stack capacitance (CL) is charged through PMOS transistor (P1) delivering HIGH rationale at the output. Whereas whenever yield hub (V_{out}) is at HIGH rationale and N tree turns ON, releasing and reusing to the power clock (V_A) by means of NMOS transistor (N1) happens, creating LOW yield rationale. In hold stage, $V_{A_{bar}}$ diminishes from high to low and V_A increments

from low to high and when they comes to underneath the edge voltage of P1 and N1 the two turns OFF in this way no advances appeared at the yield. Dynamic exchanging is decreased due to the hold stage, which will again diminish the vitality dissemination.

2.3. PROPOSED ENERGY RECOVERY LOGIC NOR GATE

The proposed MQSERL NOR entryway is appeared in Figure 2(a). This circuit is produced using two PMOS transistors (M1 and M2) and two NMOS transistors (M3 and M4).

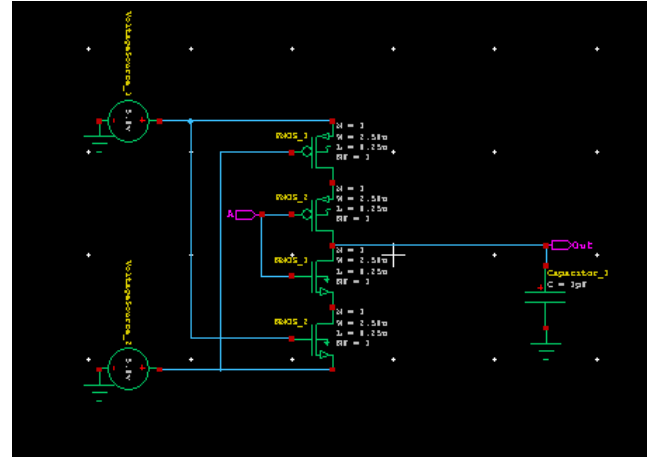


Figure 1. Proposed energy recovery logic INVERTER

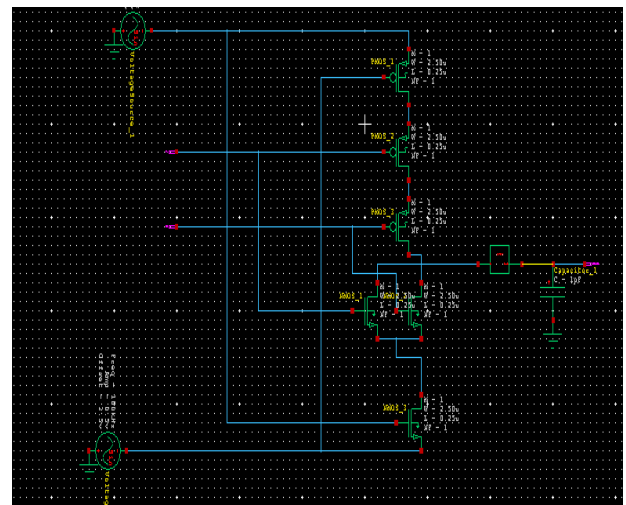


Figure 2. Proposed energy recovery logic NAND Gate

2.4. PROPOSED ENERGY RECOVERY LOGIC NAND GATE

The proposed MQSERL NAND entryway is appeared in Figure 3(a). The circuit is produced using two PMOS transistors (M1 and M2) tied in parallel and two NMOS transistors (M3 and M4) which are associated in arrangement.

Yield stack capacitance is charged/released through charging/releasing pMOS/nMOS transistors P1 and N1 whose door is specifically associated with sinusoidal power clock (V_A and $V_{A_{bar}}$ separately). M1 and M3 doors are associated together with data and M2 and M4 doors are associated with another data B.

2.5. PROPOSED ENERGY RECOVERY LOGIC XOR GATE

The proposed MQSERL XOR entryway is appeared in Figure 4(a). Its' circuit is produced using a P coordinate with four pMOS transistors (M1, M2 tied in parallel and M3, M4 associated in parallel) and a N connect with four nMOS transistors (M5 and M7 associated in parallel with M6 and M8).

A charging pMOS transistor P1 and a releasing nMOS transistor N1 is likewise utilized which are controlled by sinusoidal power timekeepers (VA and VABAR individually). M1 and M6 doors are associated with data and M3 and M5 with VA. Anyway M2 and M8 entryways are associated with data B and M4 and M7 with B.

2.6. PROPOSED ENERGY RECOVERY LOGIC 4 BIT HALF ADDER AND FULL ADDER

The MQSERL full viper comprises of two MQSERL half adders and an OR gate. The square dimension outline of our MQSERL half adder is given in Figure 5(a).(b) It is produced using a XOR entryway and one AND gate. By using this method total delay and power consumption to be reduced.

2.7. PROPOSED ENERGY RECOVERY LOGIC D FLIP-FLOP

The proposed MQSERL D flip slump is appeared in Figure 6, it is produced using two MQSERL 3 input NAND entryways and two MQSERL 2 input NAND doors and a MQSERL inverter circuit. From the simulation of various logic like CMOS, QSERL, IQSERL and Proposed MQSERL with a common frequency is calculated.

Table I shows that the proposed MQSERL circuits have practically 36% or more prominent vitality sparing to the traditional CMOS circuits aside from half snake (25.7% vitality saving).Comparison of proposed MQSERL and CMOS circuits at (fA, fA_{bar})=200MHz, balance =50MHz

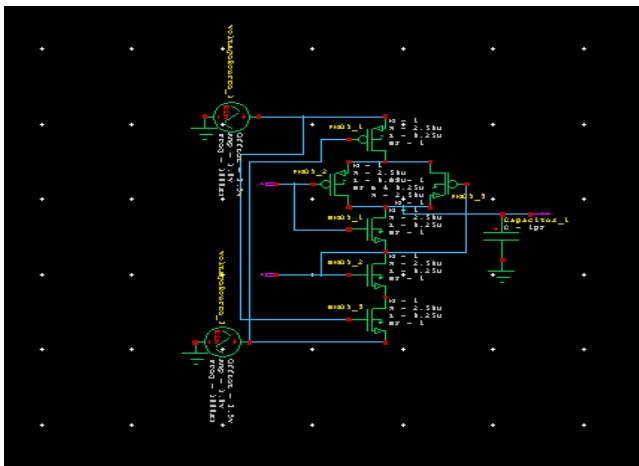


Figure 3. Proposed energy recovery logic NAND Gate circuit of MQSERL.

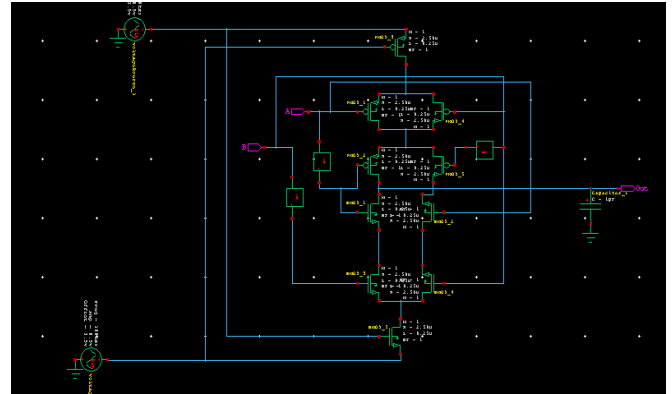


Figure 4. Proposed energy recovery logic XOR Gate circuit of MQSERL

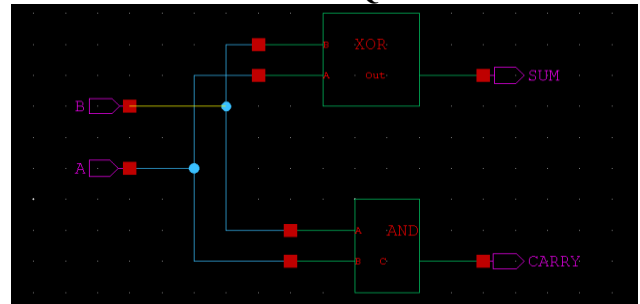


Figure 5(a). Half Adder circuit of MQSERL

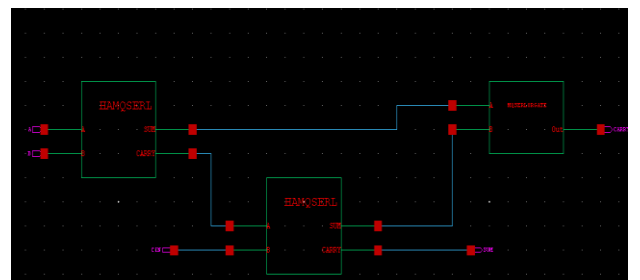


Figure 5 (b).Full Adder circuit of MQSERL

2.8. PROPOSED MQSERL 4X4 MULTIPLIER CIRCUIT.

A 4×4 piece MQSERL cluster multiplier is constructed and designed to demonstrate the handiness of the new methods of family for expansive circuits. This architecture contains of 16 MQSERL AND gate, 4 MQSERL half adders, 8 IQSERL full adders, and 8MQSERL D flip-flops as appeared in Figure 7(a). D flip-flops are used to store the 8-bit signals. The stage is finished with recreation parameters as W/L of PMOS 540/180 nm and NMOS 240/180 nm Technology, and data rate was kept multiple times the power clock rate (in IQSERL). From Figure7 (b), the modified data and output timing waveforms check the 4-bit multiplier basically. Modified results for the proposed IQSERL multiplier are contrasted and CMOS and as of (QSERL) multipliers [17– 19] utilizing a similar rationale usage, level with exchanging likelihood of sources of data, and a similar reproduction condition. The data and supply frequencies are continuously all the while from 0.1MHz to 20MHz, and comparing power dispersals for the multipliers have been estimated. IQSERL multiplier has huge power sparing to the CMOS and QSERL multipliers.

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As recurrence builds, the power sparing of IQSERL to the CMOS and QSERL multipliers diminishes as appeared in. At 0.05MHz 98% sharing in power when contrasted with the QSERL multiplier and 94% power sharing to the CMOS multiplier are achieved. At 20MHz the power sufficiently to the QSERL multiplier is 7% though to the CMOS multiplier is 11%. As recurrence goes higher, the resistive scattering increases, so control sparing is less.

After a specific high recurrence (here 20MHz), mistaken yield rationales are gotten, so for bigger complex circuits, our MQSERL circuit is constrained in some high recurrence go. Additionally from the design of proposed MQSERL inverter circuit as in Figure 7, we can sum it up for multiplier circuit likewise that, for a given execution, gadgets can be littler for a CMOS multiplier circuit than the MQSERL multiplier circuit. Thus the proposed MQSERL circuit is progressively reasonable for some particular applications where speed and territory are not basic. Since a 4×4 bit cluster multiplier is a huge complex circuit, so number of transistors on a chip (transistor check) is likewise a critical parameter to be examined. In Table II, we have given the similar investigation of transistor check of our proposed multiplier with others. It might be seen that the proposed IQSERL rationale requiring less transistors is similar to the CMOS, while IQSERL rationale have less transistor checks than QSERL. Thus it needs less mind boggling format plan and can be utilized to fabricate bigger circuits on a device chip.

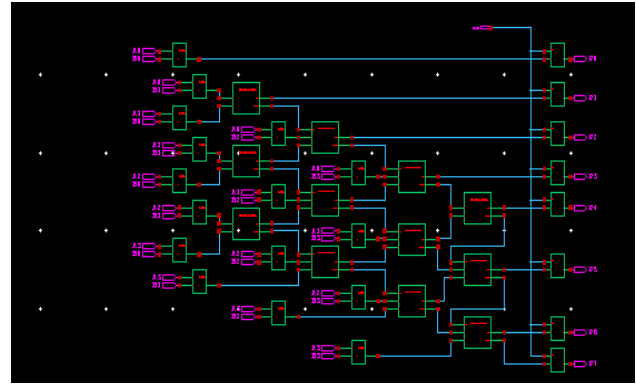


Figure 7(a). MQSERL 4×4 bit array multiplier Circuit.

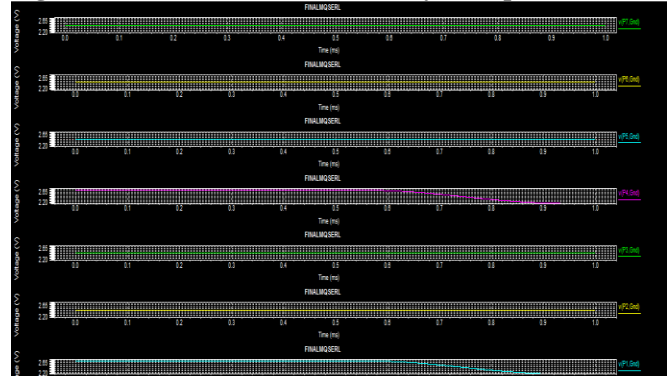


Figure 7(b). MQSERL 4×4 bit Array Multiplier Circuit Transient response.

TABLE I ENERGY DISSIPATION IN DIFFERENT LOGIC CIRCUITS

Energy dissipation in μ W							
Circuits	4 inverter chain	NAND Gate	NO R Gate	XOR Gate	Half adder	Full adder	D Flip-flop
CMOS	28.8	11.26	7.34	31.6	48.2	159.4	100.4
QSERL	15.7	8.6	9.02	30.01	34.5	140.2	92.3
IQSERL	1.65	3.2	8.4	28.3	116	179	263
Proposed MQSERL	1.2	1.1	2.1	2.8	11	17	26
% Energy Saving	39.2	36.3	55.3	38.23	25.6	43.1	48.1

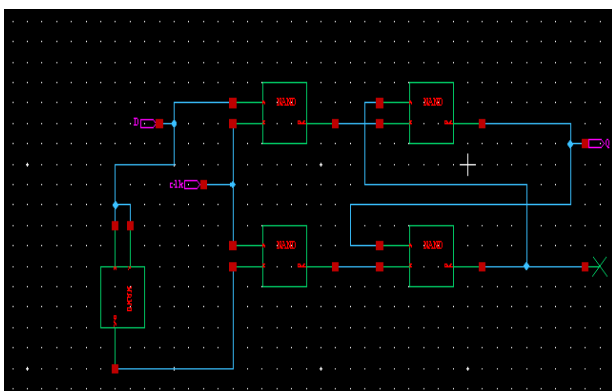


Figure 6. Proposed energy recovery logic D flip-flop

TABLE II COMPARISON OF DIFFERENT LOGIC CIRCUITS WITH VARIOUS FREQUENCIES

Frequency(MHz)	0.01	0.1	1	10	20	33.3	50
Logic	Power dissipation in μ W						
CMOS	0.09	0.12	0.40	3.32	6.6	10.9	16.4
QSERL	0.02	0.10	0.66	3.69	6.2	8.95	11.7
IQSERL	0.01	0.02	0.13	1.92	4.8	8.92	15.2
Proposed MQSERL	0.05	0.01	0.08	1.7	4.1	8.90	13.3
	Delay in ns						
CMOS	55.4	3.5	1.3	1.5	1.5	1.48	1.47
QSERL	4210	522	64.4	9.38	.69	4.10	4
IQSERL	1.92	6.24	4.53	2.56	2.07	1.8	1.68
Proposed MQSERL	1.8	5.2	3.45	1.46	1.9	1.6	1.3
Frequency(MHz)	Power Consumption (Microwatts)						
CMOS	4.99	0.38	0.55	5.05	9.9	16.1	24.1
QSERL	84.2	52.2	42.5	34.6	35.3	36.7	38.5
IQSERL	0.02	0.12	0.59	4.92	9.94	16.05	25.5
Proposed MQSERL	0.1	0.9	0.4	3.2	8.37	14.3	20.2

III. CONCLUSION

Table II shows the comparison between various logic with various working frequency ranges. The frequency selected for all the circuits varies from 0.01 MHz to 50 MHz because in that region only we have drastic change in power dissipation, power consumption and delay. All the above values were calculated and displayed. From the tabulated value it is observed that the total power dissipation, Delay and power consumption the proposed method MQSERL performs well in all circuit present in a multiplier. The reenactment results and relative execution assessment uncovered that control dispersal in the MQSERL rationale family is impressively lower than the CMOS and the detailed adiabatic (QSERL) family; subsequently the proposed MQSERL family beats and gives practically 20% or more noteworthy power sparing over CMOS and QSERL up to 50MHz for the MQSERL.

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