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High Performance Robust Keeper Design Technique for Wide Fan-In Domino OR Logic Using CNTFET 16nm Node Technology

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Abstract-This paper deals with the proposed adaptable threshold keeper&dynamic buffer technique(ATKDB) for CNTFET based wide fan in domino OR logic which simultaneously reduces the average power and propagation delay of the wide fan in logic implementationcompared to various dominogatetopologies.The proposed technique provides adaptable threshold voltage for the keeper transistor by means of a designed body bias generator which drives thebulk of the keeper and there by regulates the power. The design also includes a dynamic buffer at the output node to reduce pre-charge phase power consumption. With this technique, threshold voltage for keeper device is varied dynamically to reduce the contention current and clock loading. The proposed system was tested for 16 and 32 input domino gate using 16nm CNTFET model andthesatisfactoryresults w.r.t power and delay wereobtained.

Index Terms: Body Bias Generator, CNTFET Logic, Domino Logic, Delay, PDP, Power

I. INTRODUCTION

Dynamic and domino logic circuits are used widely over static logic circuits because of their power saving advantages and reduced load capacitances. Dynamic logic circuits have pull-up and pull-down networks which are built using P-type and N-type transistors respectively. Dynamic logic enables the circuit to have precise control over the output with the help of single clock input. In dynamic logic, output signal is obtained in two phases pre-charge phase & evaluation phase. In pre- charge phase, the low clock input makes the output to remain high irrespective of inputs. During evaluation phase the clock input remains high which enables pull-down network of the dynamic circuits resulting in the actual evaluation of the input logic [1], [2]. One of the major requirements for dynamicgates is monotonicity. The operation of dynamic gates is satisfactory with monotonicity rising inputs. But the operation of dynamic gates with monotonicity falling inputs is not satisfactory, which acts as major drawback in cascading of gates [3].

To achieve better performance, domino logic can be To overcome this drawback domino logic circuits have been widely used in which there is a presence of anadditional static inverter which converts monotonically falling inputs in cascaded circuits to monotonically rising inputs. The operation of domino logic circuits is similar to dynamic circuits but has an inversion in the output signal. designed with diverse circuit design techniques with keepers and footers as discussed in further sections of this work. Domino logic circuits are widely used for high speed operations & low power applications like high speed Digital Signal Processors(DSP) and so on [1], [3]. Domino logic circuits are widely preferred due to its meritorious advantages over the conventional logic circuits. [4]. Some of the merits are as such: the domino logic circuits require ‘n+2’ numbers of transistors for ‘n’ number of inputs, the two transistors are for pre-charging and evaluation of the logic. For instance It requires ‘2n’ numbers of devices for an n input universal gate and ‘2n+2’ number of devices for ‘n’ input basic gates. The number of devices is more in case of convectional design. To leverage this device reduction in this work we have deliberated the domino logic which plays a vital role in the design of wide-fan-in circuits and able to reduce the power consumption and propagation delay One of the major challenges in domino logic circuits is to make an applicable tradeoff between power consumption and propagation delay of the logic gates simultaneously [5], [6].To achieve this in this paper a new circuit design method has been used with a body bias generator and modified keeper footer techniques. In the domino logic gates the role of a keeper transistor is to eliminate charge sharing and sub threshold leakage currents. The keeper transistor remains on during evaluation phase which intends to keep the dynamic nodeat logic high state, and based on the input combinations a discharge path will be created for the output node. The aspect ratio of the keeper transistor should be as small as possible to reduce the power and propagation delay simultaneously. But with very smaller keeper transistor the output has considerable disturbances. Thus, there exists a need of apt circuit design to avoid signal disturbances and obtain a robust output of low power and high speed operation [5]. The proposed ATKDB technique enables concurrent power reduction and propagation delay reduction and it is validated for domino OR logic. It is achieved by providing a varying threshold voltage for the keeper transistor.

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This reduces the contention current which in turn reduces the power consumption. Also a dynamic foot buffer is provided which helps in avoiding the signal from navigating to output node in pre- charge phase and thereby reduces clock loading. The paper provides comparative analysis of different domino variants with CNTFET device and presents the improved performance wrt power, delay and PDP of proposed design. It also further deals with charge sharing analysis for the wide fan in gate

II. BACKGROUND

Parasiticcapacitanceinthe logic circuitaffectsthespeedof operation in a hardway, this capacitance opposes the discharge of output voltage, and hence propagation delay plays an important role in circuit design. [7], [8] .Sometimes this delay should be maintained appropriately inordertopreventtheshortcircuitbetweenoutputpowersequenc es.This delay also prevents the merging of different output sequences. Thus a prudently designed circuit delay gives it the neededreliability, and robustness.[9].It is necessary to design the aspect ratios of devices in domino logics to minimize the effect of parasitic capacitances. In this work, the variants of domino OR gates have been designed and simulated with CNTFET 16nm model and the performance is elucidated.

A. *Standard Footless Domino Circuit Design*

Standard domino logic circuits can be implemented with or without foot transistor. The domino logic circuit implemented without foot transistor is called as foot- less domino circuit design depicted in Fig 1. T1 to Tn are inputs for the OR gate, T3 is the keeper to keep the output stable. [10], [11]. In this design the circuit suffers from high contention current during evaluation phase as a single keeper transistor cannot reduce the contention current to the greater extent. [12], [13]. This high contention current results in high power consumption and increases propagation delay which deteriorates the circuit performance in return. Since the use of CNTFETS the delay will be much improvised wrt CMOS based domino circuit due to the low power advantage of CNTFET.We use a CNT chirality of (13,0) for the design.

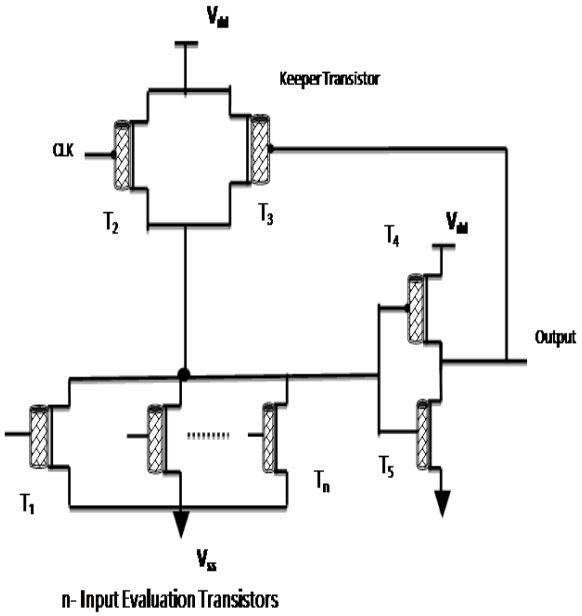

Fig 1, Standard footless domino logic circuit

B. *Standard Footed Domino Logi ccircuit Design*

In thisdominologiccircuit depicted in Fig 2,thepre-chargephaseandevaluation phases are operated through the foot transistor T6 with clock input. During pre-charge phase dynamic node gets pulled up to Vdd level and it is maintained at Vdd by utilizing keeper transistor T3 a PCNFET which counters the leakage currents on output node when it floats high for extended periods. And rest of the circuit in pre-charge other than the pull-upnetworkgetsdeactivated;thereisnoprocessingof inputs during this phase. During the evaluationphasethedynamicnodewhichismaintainedat Vdd (inpre-chargephase)isdischargedthroughpull-down network,thisleadstoprocessingoftheinputsduringthis phase. Due to the presence of parasitic capacitance and resistance the discharge time during evaluation phase increases, this results in the propagation delay to output node. When the output is low that is ‘0’, keeper transistor is always ON and pulls-up the dynamic node to Vdd level. A proper logic input provides a discharge path for dynamic node. The keeper transistor opposes the discharge of the dynamic node which degrades the power and speed characteristics of the standard domino logic. The current provided by the keeper Transistor during the discharge of dynamic node in evaluation phase is called as contention current. [14], [15].In this work with ATKDB technique we address the issues of contention current through the design of a body bias generator effect

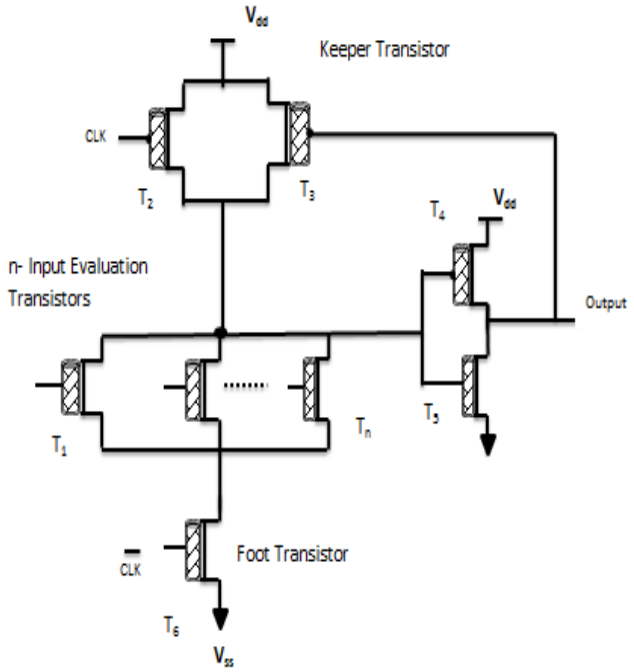

Fig2. Standard footed domino logic circuit

C. Conditional Keeper Domino Circuitdesign:

In this circuit design depicted in Fig.3, two keeper transistors wereused T3 and T6 in order to reduce power consumption. One of thekeeper transistorsissmallkeepertransistorandtheotherone connected to delayed clock is alargerkeepertransistor based on the aspect ratios. During evaluation phase larger keeper transistor was turned on which plays a major role in reduction of power consumption by reducing contention curre nt. Duringpre-chargephasesmallerkeepertransistorwas turned on for reduction of power consumption. In the design an AND logic was used in order to adjust the clock delay for evaluation and to achieve a stable output. This technique was employed in [11],[16] and it is redesigned with CNTFET devices in this work for validation.

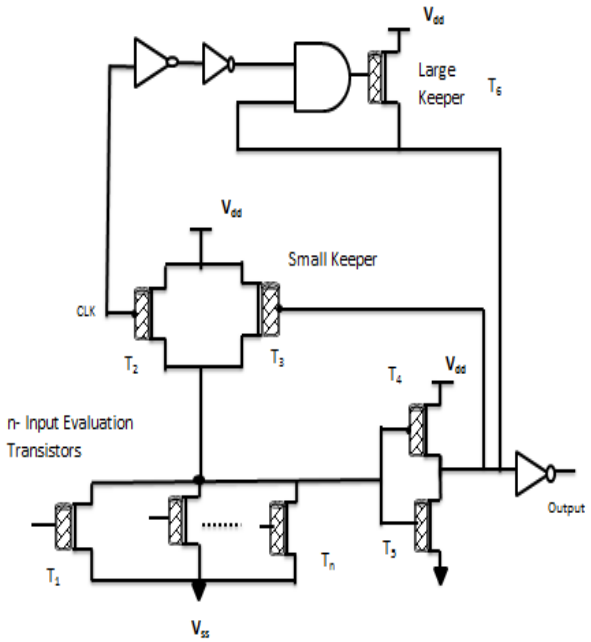

Fig 3. Conditional keeper domino circuit

D. High Speed Domino Logic circuit

This technique depicted in Fig.4, focuses to reduce the propagation delay.Duringpre-charge phase PCNFETS T2 & T7 were turned on. During evaluation phase the transistor T6 is turned on and T7 cut off. With proper inputs provided the dynamic node can be discharged. Thus, the T6 pass transistor works to keep the evaluated signal better when a weak '0' is available at dynamic node. The overall propagation delay was reduced [11], [17] as there is no need to adjust the delay with additional gates.

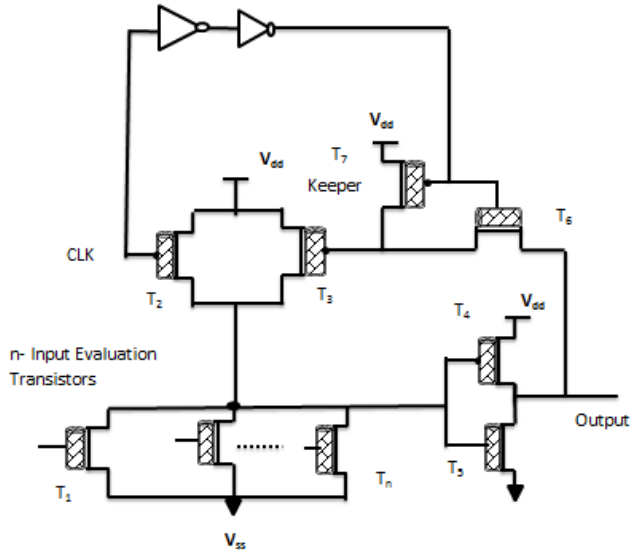

Fig 4. High speed Domino logic circuit.

E. Diode Footed Domino Logic Mirror Circuit

The arrangement of logic mirror circuit is as shown in the Fig 5. This logic mirror has been implemented in order to reduce power consumption and propagation delay by maintain uniform currents with available current mirror for the dynamic node. [11].during pre-charge phase the operation of diode footed domino logic mirror circuit was similar to the operation of standard domino logic circuit. During evaluation phase the mirror transistor circuit is turned on and it stabilizes the output node by maintaining the contention current identical to the drain current of footer there by providing a proper ground level for the dynamic node.

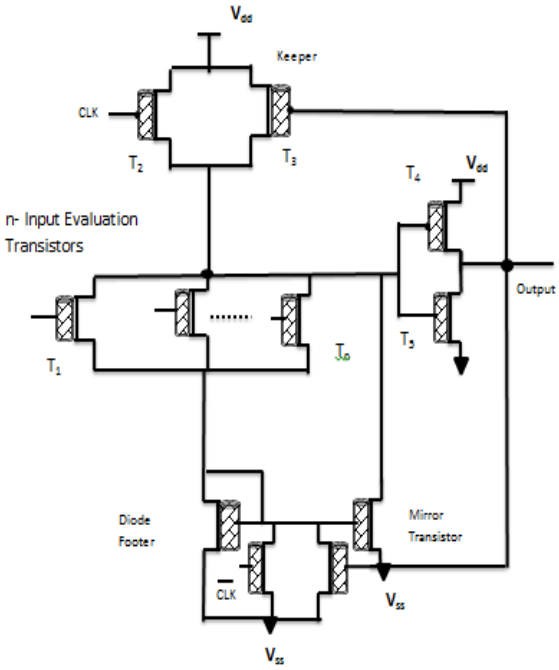

Fig 5. Diode footed domino logic mirror circuit

F. Current Mirror Footed Domino or Logic

Thecircuitrepresented in Fig 6, comprisesofacurrentmirrorcircuitwhich ismadeupofthree tail NCNFETSwhoseaspect ratios are designed such as to match the tail and contention currents. The operational difference of the circuitisseenintheevaluationphase.Asintheevaluation phase the clock signals provided is logic '1' it turns on all the tail transistors in the current mirror path which resultsinprovidingadditionalpathsforthedischargebased on inputs. Thus, in this way the overall propagation delay of the circuit isreduced.

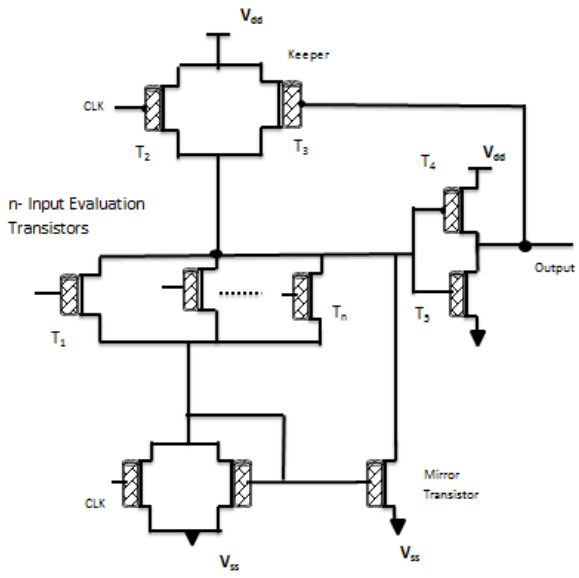

Fig.6, Current mirror footed domino logic OR

Comparedtotheabovetechniquesthepowerconsumptionandpropagationdelayoftheproposed ATKDB systemisvery less. The simulation results and comparative analysis of proposed technique with the above discussed techniques of section 2 is provided in the section4.

III. PROPOSED SYSTEM

A. Body Bias Generator (Bbg)

Theoperationof body biasgenerator used in [4] is designed with 16nm CNTFETS to suit the wide fan in gate. It is depicted in Fig 7, the device details are mentioned as below *Physical Channel length= 16nm, Oxide thickness=4nm, Pitch of tube=20m, chirality (13, 0), number of tubes used=3* It can be explained in two different stages namely: forward body bias generator and reverse body bias generator which provides different biasing voltages at its output node BBG_OUT which drives the bulk of the keeper transistor in the proposed circuit. During forward body bias generator stage the keeper transistor is forward biased which helps in providing stable output waveform. During reverse body bias generator stage,thekeepertransistorisreverse biasedwhichhelpsinreducingcontentioncurrentand helpsinreductionofpowerconsumption

i. Pre-charge phase:

During pre-charge phase the body bias generator circuit is reverse body biased i.e. the output of body bias circuit BBG_OUT will provide Vth2. In the design Vth2>Vth1. This high Vth2increaseskeeperthresholdvoltagewhichhelpsinreduction ofcontentioncurrentofdynamicnode.

ii. Evaluation Phase:

Duringevaluationphasethebodybiasgeneratorisforwardbodybiasedwhichreducesthekeeperthresholdvoltage to Vth1. This reduced voltage of keeper transistor helps in providing stability and reliability to the output waveform.

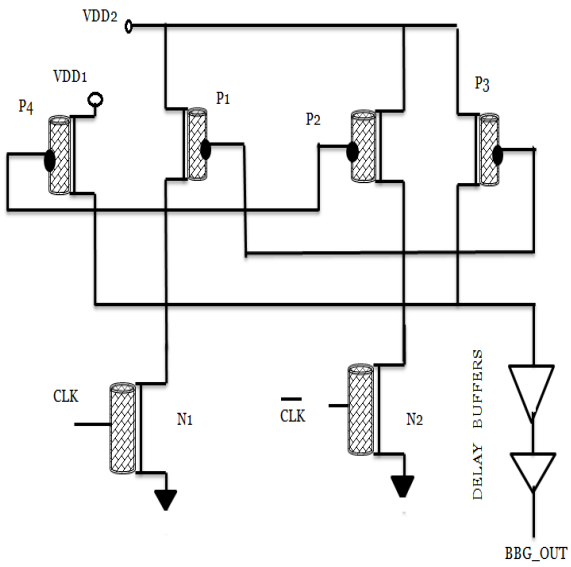

Fig7: Body bias generator

B. Dynamic Buffer

The operation of inverter in the proposed ATKDB technique is dynamic in each phase ofbody bias logic circuitoperation. Duringpre-chargephasethestaticinverterduetovariation in the circuit design results in the formation of floating node. Thus, during pre-charge phase though the major part of

output remains at logic '0' due to floating node a small part of output raises to a voltage lesser than thresholdvoltage andhence resultsinthepower reduction .Duringevaluationphasetheoperationofstaticinverter issimilartothatofstaticinverterinthestanddomino logiccircuit. Thus, it dynamically adapts to keep the contention current less and evaluate the logic. The operation of domino logic circuit with ATKDB techniqueisdependentonclocksignalandbody bias generator depicted in Figure 7. InthecircuitdesignusingATKDBtechnique,instead of connecting the source terminal of NCNFET transistor of buffertoground,itisconnectedtodrainterminal of footer NCNFET transistor of dynamic circuit. The adaptive threshold voltage is obtained from BBG_OUT stabilizes the keeper bulk and dynamic node power consumption is reduced under switching.

C. Operation

Thelogic'0'clocksignal is provided to T2 and alsoN1 device which is the input of BBG.The bulk of keeper T3 is driven by the output of BBG such that we have varied bulk potential to adjust the threshold voltage based on precharge or evaluation mode. Thekeepertransistor T3 will be chargedtohigh threshold voltageofVth2, this result in the increased keeper thres hold voltage,which is obtained from the differenceVth2-Vth1.This high thres hold voltage of keeper thus helps in reducing contention current in the circuit by the beginning of evaluation phase.

During pre-charge phase the dynamic node of the circuit will be charged to Vth1 through pull-up transistors i.e. PCNFET transistors of domino gate circuit. This Vth1 turns on NCNFET pull down transistor of dynamic buffer circuit, thus this dynamic node tries to discharge through NCNFET. This results in the output of domino logic circuit discharging to zero for a definite interval of time after which it raises to a voltage less than threshold voltage for a small interval. This is the intervaloftimewheretheoutputraisesfromzerotoavoltageless thanthresholdvoltageand during which the output pulse is paused from propagating to output. This results in reduction of power & propagation delay simultaneously during pre-charge phase. During entire precharge phase the footer NCNFET remains off. During evaluation, Thelogic'1'clocksignalwhenappliedto N1 of body biasgeneratorintheproposedsystem,itturnsonotherNCNFETtransistor(whichwasoffduringpre-charge),thusthenodeconnected to it is discharged to groundresulting in an output voltage of Vth1 at the BBG_OUT. The thirdnodeisalsochargedtoVth1throughoneofthePCNFET transistor.
Hencekeepertransistorofdominologicgatecircuitwill be charged to Vth1 which reduces the threshold voltage of the keeper transistor.
This reduced keeper threshold voltageensureshighercurrentandmaintainsstabilityand reliability in the outputwaveform. Duringevaluationphase,theproperinput combinations providedto domino logic gate circuit turns 'ON' NCNFET pull down transistors to evaluate the logic accordingly.Thisresultsinthedischargeofdynamicnode which is maintained at Vth1. Thus, during evaluation phase with proper logic gate inputs the dynamic node will be discharged to zero. This logic '0'at dynamic node turns of the PCNFET of dynamic buffer circuit. This results in producing logic high output waveform. During evaluation phase if no proper inputs are provided to logic gate circuit the dynamic node does not discharge to zero but remains at Vth1 which results in production of logic low output waveform. The PCNFET transistors in domino logic gate circuit which forms pull-up part of the circuit remains cut-off during evaluation phase of circuit operation.

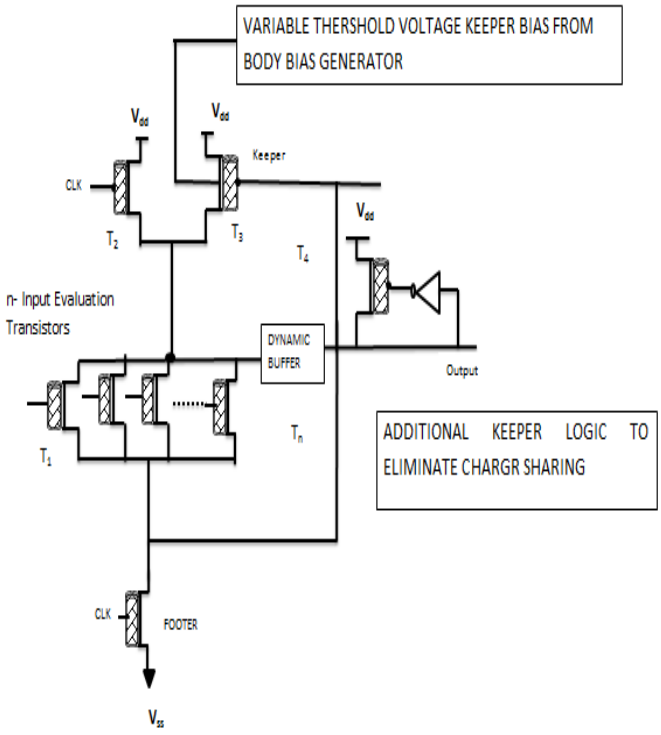

Fig 8. Proposed logic implimentation with variable threshold voltage keeper

The output waveform of ATKDB technique with Domino two input OR Gate circuit during pre-charge phase and evaluation phase is as shown in the Figure 9.

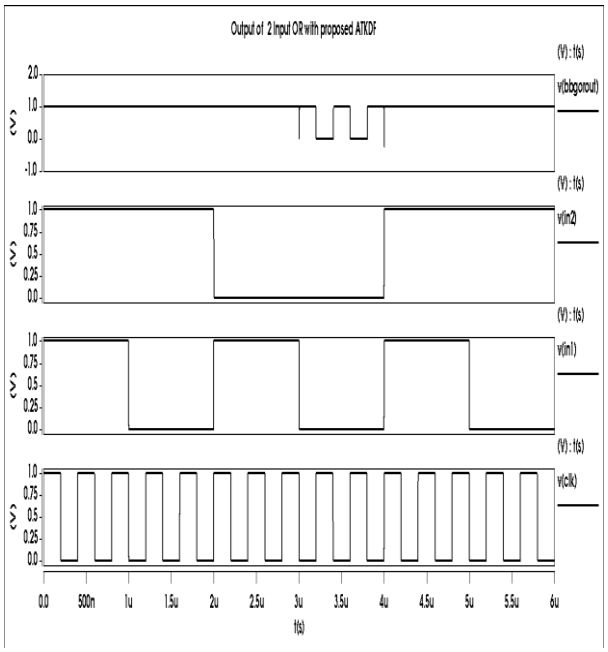

Fig. 9, Output waveform of two input domino logic OR with ATKDB technique

IV. SIMULATION RESULTS

The proposed system was simulated using CNTFET 16nm model. The propagation delay and power consumption are calculated using SPICE techniques. From figure 9 it is evident that OR logic is working for all the input combinations. We can observe that when both the inputs are logic '0' we can find low to high and high to low transition at body bias generator output (vbbgrout) as depicted. The logic is evaluated for clock 1 and node is pre-charged for clock 0 when both vin1 and vin2 are logic 0.That is the bias for the keeper is adjusted such that pull down device of dynamic buffer turn on/off as per the evaluation dynamically. The state changing of the node is dynamic so as to reduce the leakage power. The comparative analysis of the proposed system with other domino logics when built using CNTFETs is provided in table1. It gives information regarding the propagation delay, power consumption & power delay product of various circuits designed in this work.

Table 1: Comparison of PDP of different topologies

Circuit technique	**Power consumption (W)**	**Propagation delay(s)**	**Power delay product(J)**
Conv. Body bias generator OR	1.60E-05	9.79E-11	1.57E-15
Conditional keeper OR	2.70E-05	1.40E-06	3.78E-11
Logic mirror OR	1.14E-05	1.40E-06	1.59E-11
Current mirror OR	1.10E-05	1.37E-10	1.50E-15
Footless OR	1.20E-05	1.40E-06	1.68E-11
High speed OR	1.50E-05	1.40E-06	2.09E-11
Standard footed OR	1.09E-05	2.00E-07	2.19E-12
Proposed ATKDB OR	*1.51E-07*	*6.26E-11*	*9.47E-18*

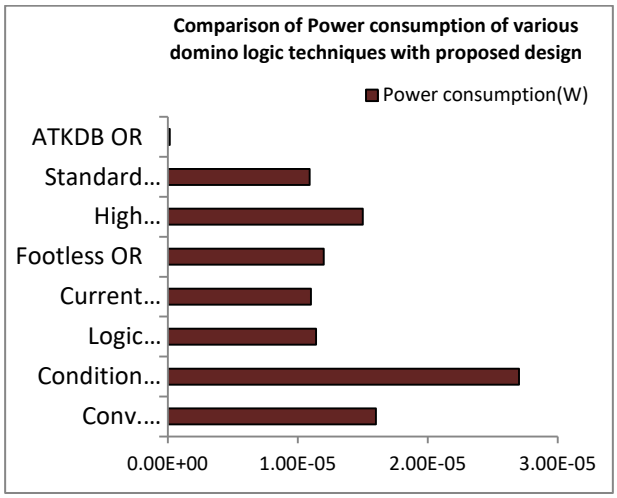

Fig 10. Representation of power consumption of various domino logic circuit

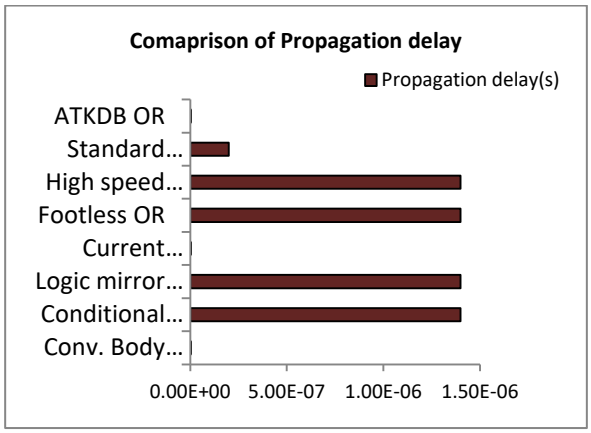

Fig 11. Representation of power consumption of various domino logic circuits

V. CHARGE SHARING ANALYSIS:

As in all dynamic circuits the proffered design also suffers from charge sharing problem for logic high inputs during pre-charge phase. Charge sharing is mainly due to parasitic capacitance at dynamic node. To have explicit operation the noise margin at dynamic node should be within limits and it can be maintained by having proper voltage drop at the node. Improper voltage drop at dynamic node causes

adverse effects in the next stages under cascading. The charge sharing issue has been addressed in this work usingfollowing strategies. I method: In this method the dynamic buffer is provided with voltage higher than the supply voltage. Though this method eliminates the problem of charge sharing completely it cannot be implemented in the design because the PCNFET transistor in the dynamic buffer circuit causes a large leakage current and this large leakage current cannot be reduced effectively.

II method: Increasing the channel length and providing an easy path for discharge which results in decrease of voltage drop. All though also the issue of charge sharing in pull-down devices effectively reduced, this method affects the propagation delay of the circuit.

III method: In this method load capacitance is increased and thus parasitic capacitance is decreased. The adverse effect of this method is that the average power consumption of the circuit increases significantly.

IV method: Introducing an additional keeper and an inverter circuit in the design to reduce charge sharing. This provides the best solution for solving charge sharing issue and thus is implemented in design. This method reduces the static current to almost zero and the voltage drop at dynamic node is completely eliminated. Thus, the method has less effect on delay as small parasitic capacitances are present. The simulation results of the proffered design with method IV incorporated is as depicted in the following figures.

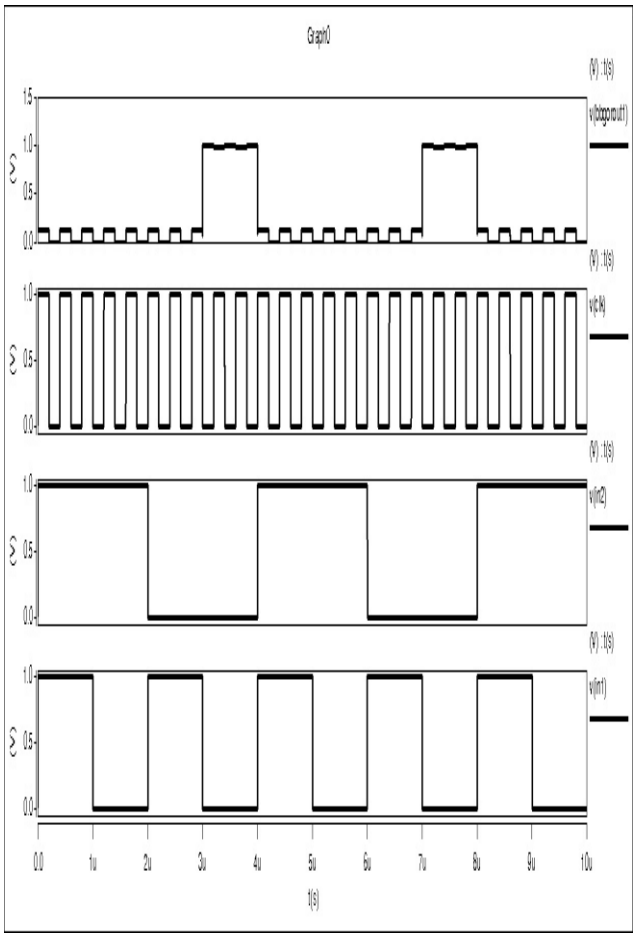

Fig 12, Output waveform with charge sharing elimination circuit.

VI. WIDE FAN-IN DOMINO OR GATE:

The ATKDB technique was also implemented with wide fan-in domino OR gate circuit to validate the stability of the proposed domino model. The technique was implemented with four, eight, sixteen input and thirty two input domino OR gates and the results were obtained satisfactorily. The power consumption, propagation delay output & Power delay product for Wide fan-in gates obtained is as shown in the table 2.

Table 2 .PDP comparison of wide fan in OR logic using ATKDB technique

Wide Fan-in OR with ATKDB	Power consumption	Propagation delay	Power delay product
4 input OR	2.15E-07	1.02E-07	2.20E-14
8 input OR	2.50E-07	4.99E-08	1.25E-14
16 input OR	1.22E-06	1.25E-06	1.52E-12
32 input OR	1.234E-06	1.299E-06	1.602E-12

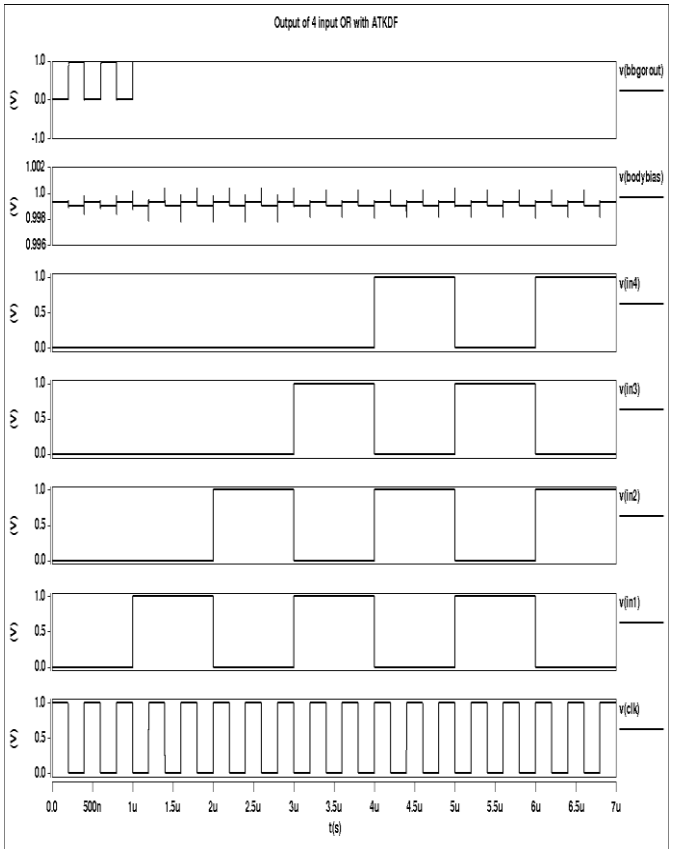

Fig 13. 4 input ATKDB OR circuit logic timing diagram.

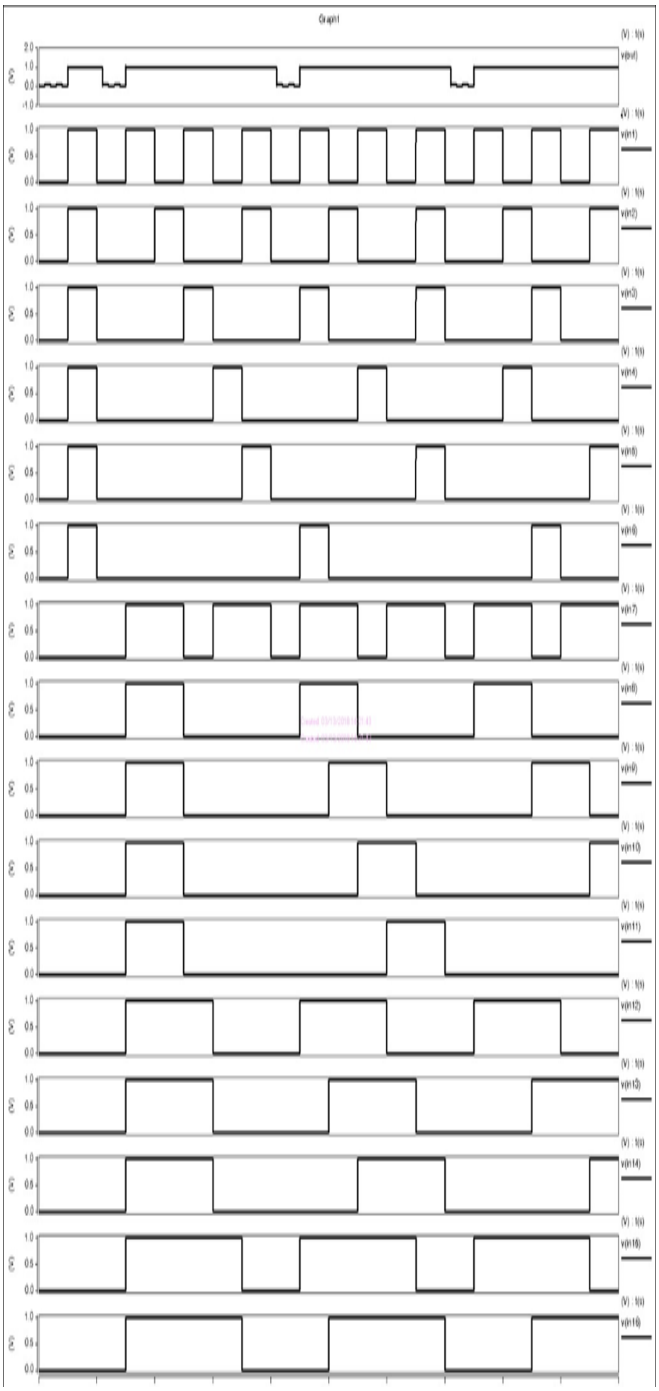

Fig 14. 16 input ATKDB OR circuit logic timing diagram.

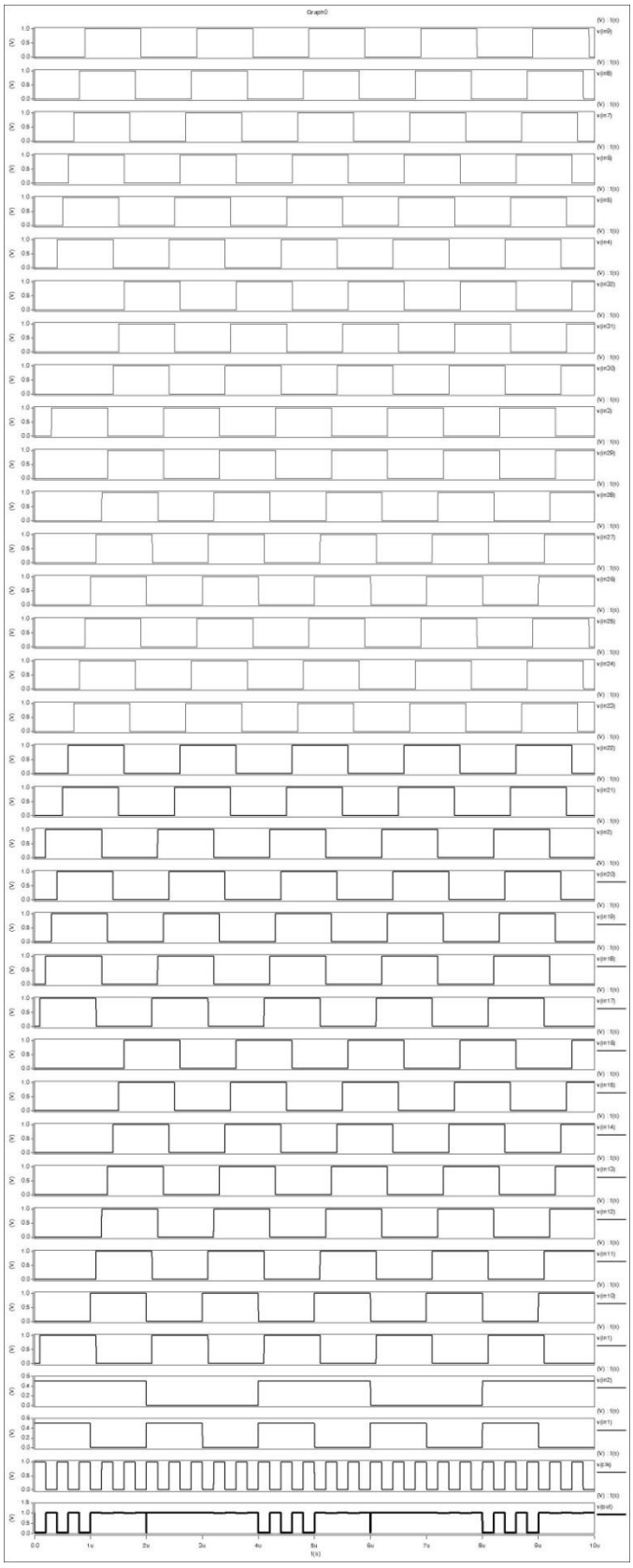

Fig 15. 32 input ATKDB OR circuit logic timing diagram.

VII CONCLUSION

By means of the proposed ATKDB technique with CNTFET 16nm devices as a building element, the design was able to achieve substantial reduction of the power consumption and propagation delay of a wide fan-in operation ofdomino OR gate. The proposed technique has been tested and benchmarked with various domino techniques proposed in the literature and it has been validated by keeping PDP as target. The comparative design study reveals drastic reduction in PDP for the proposed one. The design also attempts to address the issues of charge sharing in the pull down line using an additional dynamic keeper. The reliability of the design is established by attaining the glitch less output for 16 and 32 input OR gates. Though the circuit demands little more transistor count for the body bias generator, it is highly gainful in the circuits where power dissipation is a major check. Hence the recommended technique can be strongly considered for building high performance standard cells for future CNTFET based digital logics.

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