



# Energy Efficient Digital Circuits using Two Phase Clocking Sub-Threshold Adiabatic Logic

M. Bharathi, N. Padmaja, D. Leela Rani

**Abstract:** Power is a major constraint in Digital VLSI circuits, due to reduction in sizes of Metal Oxide Semiconductor (MOS) transistors are scaling down. Low-power technologies are used to diminish the power utilization be able to be classified as Sub-threshold CMOS and Adiabatic logic techniques. In, Sub-threshold CMOS defines a system which reduces the power utilization to inferior than the threshold voltage of a MOS Device, where as Adiabatic logic circuit is a method which minimizes the energy usage through suppress the applied voltage to the resistance of a given VLSI design. This effort deals to offer a subthreshold adiabatic logic circuit of low power CMOS circuits that uses 2φ clocking subthreshold Adiabatic Logic. The digital circuits were designed in HSPICE using 0.18 μm CMOS standard process technology. It is evident from the results that the 2φ Clocking Subthreshold Adiabatic design is beneficial in major application where power starving is of major significance at the same time as in elevated its performance efficiency in DSP processor IC, System on chip, Network on chip and High speed digital ICs.

**Index Terms:** Subthreshold Adiabatic, Threshold voltage, Two Phase clocking, Energy Dissipation & HSPICE

## I. INTRODUCTION

### A. Adiabatic Switching

The word “Adiabatic deals with a change of state without any heat loss or heat gain [5] [24]. This adiabatic logic configuration majorly reduces the power dissipation by storing and reusing the energy in capacitors as a load. In usual CMOS logic, the activity of transitions can cause a transfer of energy from VDD to output node or output to VSS[2] [17]. During a transition from 0-to-VDD transition of the output, the total output charge  $Q = C_{load} * VDD$  which drained from the power supply at a constant voltage. So the energy consumption,  $E_{supply} = C_{load} * VDD^2$  is drawn from the power supply during the transition. If output node is charged to VDD indicates the end of the transition, the amount of energy stored at the output node is given as  $E_{stored} = C_{load} * VDD^2 / 2$ . Thus, partly the injected energy from the VDD is dissipated in the Pull up network while half of the

energy is delivered to the output node. During a subsequent VDD-to-0 transition, the load capacitor stores the dissipated energy it cannot allow to sink through the ground. [4]. To further reduce the power dissipation, the designers has to minimize the switching activities or to reduce the node capacitance or to reduce the voltage swing, or any of the combination of the methods. To increase the energy efficiency of the logic circuits recycling is a technique that can be determined the energy drawn from the VDD which can be obtained by the fabrication technology, switching speed, and the voltage swing [16].

### B. Adiabatic Switching Principle

Low energy dissipation which is due to slowing of switching transition operation by under certain conditions. In Adiabatic, the dissipated energy/ heat can be stored in load capacitance as a charge. Hence Adiabatic logic is also referred to as Energy Recovery CMOS [7], [10],[23]. Practically, the energy dissipation related with transfer of charge typically consists of an adiabatic part and non-adiabatic part. Hence, it is not possible to reduce the energy loss completely, not considering the speed of switching activities. Thus, in the Adiabatic Switching technique, the energy will be preserved in rather than dissipated as a heat [21]. This approach can also be used to in digital systems for reduction of power.

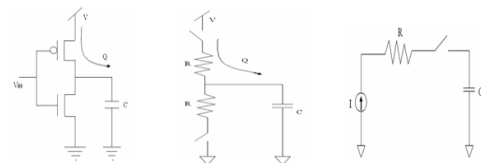


Figure 1.1 a) CMOS Inverter b) Adiabatic switching c) RC equivalent circuit for Adiabatic Switching.

Figure 1.1 represents a CMOS Inverter, an Adiabatic switching circuit and its RC equivalent circuit for Adiabatic Switching. In this circuit, a constant-current source is used to charge the capacitor as a load instead of voltage source that is use most often in the conventional CMOS circuits. [15]. A linear ramp voltage is generated in correspondence to a constant charging current. Assuming, zero initial capacitor voltage ‘VC’,

$$E = (2RC/T) \left( \frac{1}{2} CV^2 \right) \quad (1.1)$$

Where ‘E’ corresponds to energy dissipated through charging of capacitor, R’ is the Resistance of the MOS switch when switched ‘ON’, Q is the charged amount transferred to the load capacitance, ‘C’ is the effective load capacitance, ‘V’ corresponds to final voltage at the load and ‘T’ belongs to time required for charging [14].



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The following are the observations:

Here, the energy dissipated is lower than for the usual case, if the charging time 'T' is better than 2RC and is proportional to load resistance 'R'. It is in contrast to the conventional case, where energy dissipated depends on voltage swing and the load capacitance. Thus, by reducing the resistance of the PMOS network during the on period will inturn reduce the energy dissipation. Figure 1.2 is a simple circuit that depicts the reduction of energy dissipation.[13]

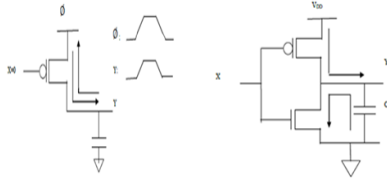


Figure 1.2 Energy dissipation of CMOS Inverter during charging and discharging

The energy which was stored in the capacitive load is only half of the energy supplied [1] [12],

$$E_{\text{charge}} = \frac{1}{2} C V_{DD2}^2 \quad (1.2)$$

From the energy conservation law,

$$\begin{aligned} E_{\text{total}} &= E_{\text{charge}} + E_{\text{discharge}} \\ &= \frac{1}{2} C V_{DD2}^2 + \frac{1}{2} C V_{DD2}^2 \\ &= C V_{DD2}^2 \end{aligned} \quad (1.3)$$

The load capacitance and further the energy consumption is reduced by replacing AC power supply to DC power supply in conventional CMOS logic. [11]. When an AC power supply is used, the applied voltage to the resistance can be expressed as equation (1.4) during the interval  $0 \leq t < T$  and by equation (1.5) for  $t \geq T$  [9].

$$\begin{aligned} V_R(t) &= \left(\frac{V_P}{T}\right) t - V_c \quad 0 \leq t < T \\ &= RC \left(\frac{dV_c}{dt}\right) \\ V_R(t) &= \left(\frac{RC}{T}\right) V_P (1 - e^{-t/RC}) \end{aligned} \quad (1.4)$$

$$\begin{aligned} V_R(t) &= \left(\frac{V_P}{T}\right) t - V_c \quad t \geq T \\ &= RC \left(\frac{dV_c}{dt}\right) \\ &= \left(\frac{RC}{T}\right) V_P (1 - e^{-t/RC}) e^{-\frac{t-T}{RC}} \end{aligned} \quad (1.5)$$

where  $V_p$  is AC supply voltage,  $V_c$  is the voltage which applies to the load capacitance and 'T' is rise time of AC power supply. Thus, energy consumption is represented as equation (1.6).

$$\begin{aligned} E_{\text{dis}} &= \int_0^T i V_R dt + \int_T^\infty i V_R dt \\ &= \left(\frac{RC}{T}\right) C V_P^2 \left(\frac{RC}{T} e^{-\frac{T}{RC}} + 1\right) \end{aligned} \quad (1.6)$$

## II. DESIGN OF DIGITAL CIRCUITS USING SUBTHRESHOLD ADIABATIC LOGIC

Sub-threshold CMOS theory and Adiabatic logic circuit technology are two low-power technologies that can be used for lower power consumption. Using Sub-threshold CMOS

technique, the consumed power can be reduced to a lower threshold voltage [7]. In Adiabatic logic technique, the constant voltage power supply slope is varied which inturn reduces the energy utilization by altering the applied voltage to a given circuit. In the present work, a Sub-threshold Adiabatic logic circuit uses two alternating power supplies with dissimilar frequency and amplitudes. [22].

### Sub-Threshold Region- Operation

Figure 1.3 shows NMOS transistor  $I_d$  vs  $V_{gs}$  characteristics for 180nm conventional CMOS process. The transistor Width to length ratio chosen is  $1.0 \mu\text{m}/1.0 \mu\text{m}$ . A more rapidly check of the  $I_d$  vs  $V_{gs}$  curve of Figure 1.3(a) shows that the current is not symmetric to zero at  $V_{gs} = V_t$  (where,  $V_t$  be the threshold voltage of the MOS device), since the conduction of MOS transistor will be, below the threshold voltage. This gives the "subthreshold conduction" or "weak-inversion conduction". The onset of strong inversion region means that abundant numbers of charge can be seen in the channel for conduction, but current doesn't flow for gate-source voltages below the threshold voltage. The switching activity from the ON to the OFF conduction is regular. To substantiate this effect,  $I_d$ - $V_{gs}$  curve is plotted on a logarithmic scale as represented in Figure 1.3(b). This affirms that the current do not sink to ground at once for  $V_{gs} < V_t$ , but it gradually decreases exponentially.[1].

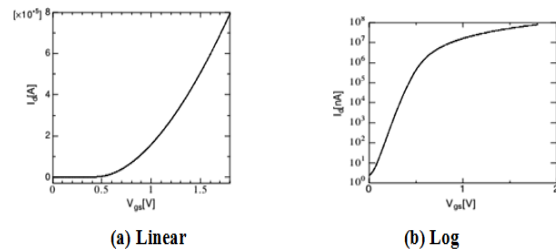


Figure 1.3:  $I_d$ - $V_{gs}$  characteristics of NMOS transistor

The current can be approximated by the equation [3].

$$I_d = I_s e^{\frac{V_{gs}}{nKT/q}} \left(1 - \frac{V_{ds}}{nkT/q}\right) \quad (1.7)$$

given  $I_s$  and  $n$  are the empirical parametric values, where  $n \gg 1$ , on average ranging around 1.5. In majority of the CMOS digital applications, the existence of subthreshold current is disagreeable because it shifts from the ideal switch-like behavior of the MOS transistor. We require that the current should drop abruptly when  $V_{gs}$  falls below  $V_t$ . Thus digital circuits are operated using infinitesimal leakage current in the subthreshold region, which results in ultra-low power VLSI circuits [8]. However, because the driving current vs delay of the circuit decreases exponentially. Hence subthreshold operation of logics can be used to limited areas only where the performance of the circuit is secondary.

### III. SIMULATION RESULTS OF ADIABATIC LOGICS AND DISCUSSION

The results of simulation of various Adiabatic Logics are shown below. They are implemented in HSPICE [26] using 0.18μm standard CMOS process . The simulated waveforms are shown for different types of Inverters as shown below.

a) 2N2N2P Inverter:

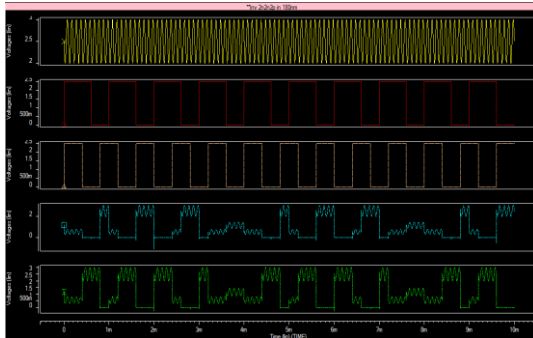


Figure 1.4(a) : Simulation result of 2N2N2P Inverter

The input pulse is a Sine wave with a selected frequency of 10 KHz and an amplitude of 0.5V that is shown as the first pulse in figure. The first waveform in the figure 1.4(a) is the input pulse and the next two waveforms are the inputs applied to 2N2N2P Inverter circuit i.e. 'ina' and 'inb' respectively. Their corresponding outputs are 'outa' and 'outb' respectively which are shown in the third and fourth waveforms of figure 1.4(a). The Simulation time is 10 ms and the average power obtained by 2N2N2P Inverter is 4.9147E-05 Watts. The same process is applied for different Inverter circuits.

b) ECRL Inverter:

The simulation time is 10 ms and the average power obtained by ECRL Inverter is 4.1567E-05 Watts which is represented in figure 1.4(b)

b)ECRL Inverter:

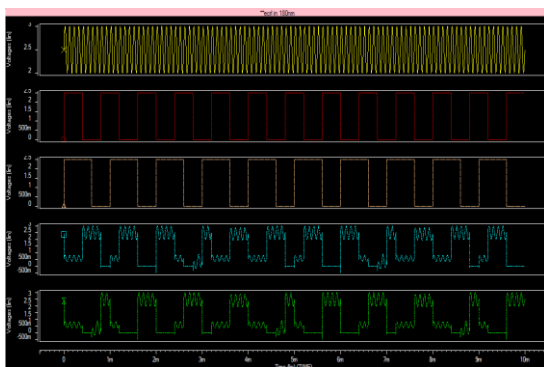


Figure 1.4(b): Simulation result of ECRL Inverter

c) CAL inverter:

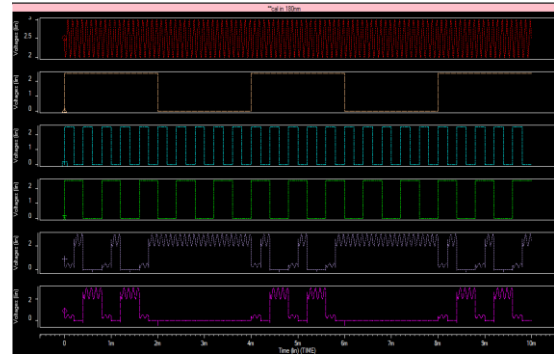


Figure 1.4(c): Simulation result of CAL Inverter

The first waveform in figure 1.4(c) is the sinewave of 10 KHz of 0.5V. The second waveform represents the auxiliary clock Cx. Next two waveforms are the inputs of CAL Inverter i.e 'in' and 'inb' respectively. Their corresponding outputs are 'out' and 'outb' respectively. The simulation time is 10 ms and the average power obtained by CAL Inverter is 1.4688E-04 Watts.

d) SAL inverter:

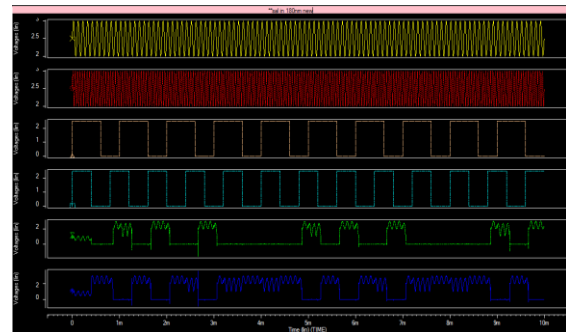


Figure 1.4(d): Simulation result of SAL Inverter

The first waveform in figure 1.4(d) are the sine waves of 10 KHz and 20 KHz respectively and amplitude of 0.5V. This inverter uses seven sine pulses from Vpc\_0 to Vpc\_6. Next two waveforms are the inputs of SAL Inverter i.e 'in' and 'inb' respectively. Their corresponding outputs are 'out' and 'outb' respectively. The simulation time is 10 ms and the average power obtained by SAL Inverter is 3.2969E-05 Watts.

e) 2PC2AL inverter:

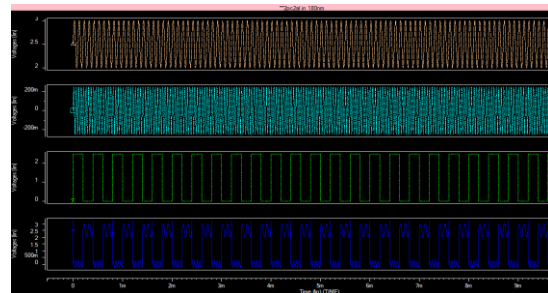
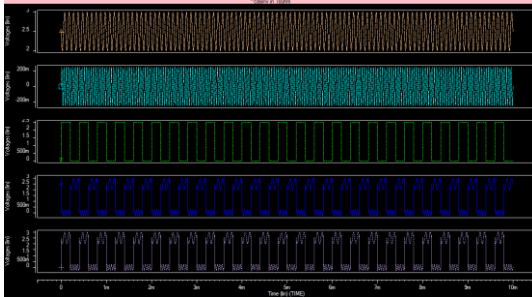


Figure1.4(e): Simulation result of 2PC2AL Inverter

The first two waveforms of figure 1.4(e) are two sine waves of 10 KHz and 20 KHz of 0.5V and 0.25V respectively. The third waveform is the input 'in' of 2PC2AL Inverter. Its corresponding output 'out' is generated with a simulation time of 10 ms. The average power obtained by 2PC2AL Inverter is 4.5892E-07 Watts.

f) Proposed Cascaded Inverter:



**Figure 1.4(f): Simulation result of Proposed Cascaded Inverter**

Similarly, The first two waveforms of figure 1.4(f) are sine waves 10 KHz and 20 KHz and 0.5V and 0.25V respectively. The third waveform is the input 'in' of Cascaded Inverter and fourth waveform is the inverted output 'out1'. The last waveform is the cascaded output 'out2' of the inverter. The simulation time is 10 ms and the average power obtained by Cascaded Inverter is 4.5955E-07 Watts.

g) Power Comparison of Various Adiabatic Logics

It can be concluded that the proposed cascaded inverter and 2PC2AL inverter dissipates less power when compared to other logics [10]. At higher frequencies the power dissipated by cascaded inverter will be less when compared with 2PC2AL inverter [1].

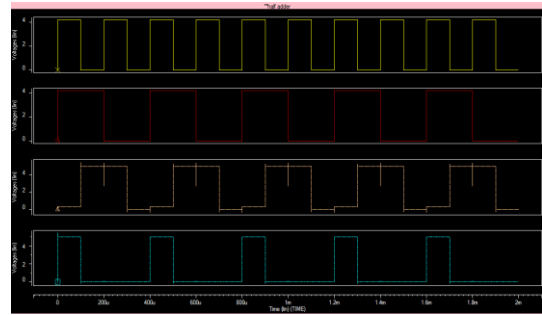
**Table 1.1: Comparison of average power of various Adiabatic Logics**

Adiabatic Logics	Average Power (in Watts)
2N2N2P	4.9147E-05
ECRL	4.1567E-05
CAL	1.4688E-04
SAL	3.2969E-05
2PC2AL	4.5892E-07
Proposed Inverter	4.5955E-07

### IV SIMULATION OF DIGITAL CIRCUITS

Here digital circuits like half adder, full adder [18] and a D-Flipflop are simulated using HSPICE and the average power obtained is tabulated as shown in Table 1.2.

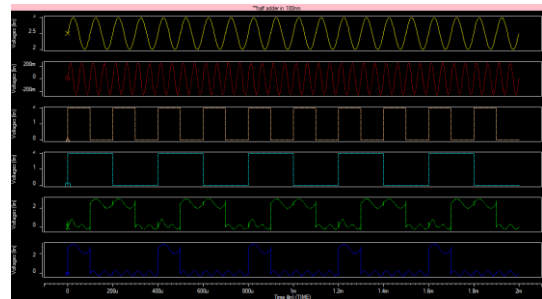
a) Half Adder using CMOS logic:



**Figure 1.5(a): Simulation result of Half Adder using CMOS logic.**

The first two waveforms in figure 1.5(a) are the inputs 'A' and 'B' to the half adder [19],[20]. The sum 'S' and carry 'Cout' are outputs generated by the half adder. The simulation time is 2 ms and the average power calculated was 8.4168E-05 Watts.

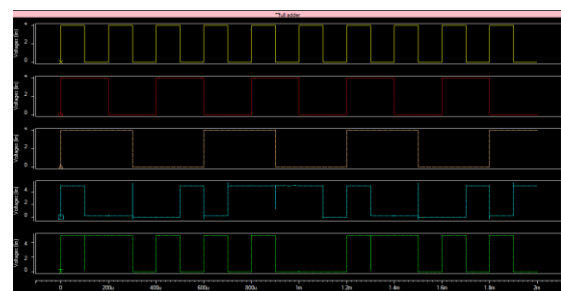
b) Half Adder using Subthreshold Adiabatic logic:



**Figure 1.5(b): Simulation result of Half Adder using Subthreshold Adiabatic logic.**

The first two waveforms in figure 1.5(b) are the sine waves with frequencies 10 KHz and 20 KHz of 0.5V and 0.25V respectively. The next two are the two inputs that are applied to the Half adder are denoted as 'A' and 'B'. The sum 'S' and the carry 'Cout' are outputs generate by the half adder circuit. The simulation time is 2 ms; the average power obtained is 4.5407E-05 Watts.

c) Full adder using CMOS logic:



**Figure 1.5(c) : Simulation result of Full Adder using CMOS logic.**

The first three waveforms in figure 1.5(c) are the inputs 'A', 'B' and 'Cin' to the full adder. The sum 'S' and carry 'Cout' are outputs obtained by the full adder with a simulated time of 2 ms. The average power obtained is 1.4075E-04 Watts.

d) Full adder using Subthreshold Adiabatic logic:

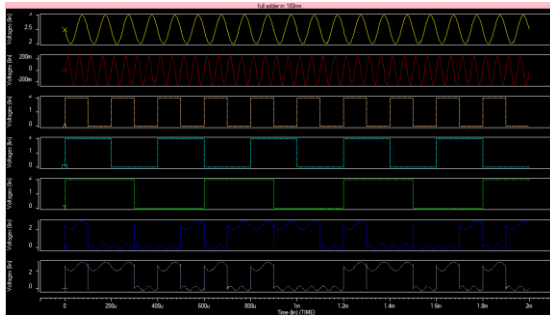


Figure 1.5(d): Simulation result of Full Adder using Subthreshold Adiabatic logic.

The first two waveforms in figure 1.5(d) are the sine waves with frequencies 10 KHz and 20 KHz of 0.5V and 0.25V respectively. The next three are the inputs of the full adder ‘A’, ‘B’ and ‘C’. The sum ‘S’ and carry ‘Cout’ are outputs generated by the full adder. The simulation time is 2 ms; the average power obtained is 7.5174E-05 Watts.

e) D-Flip flop using CMOS logic:

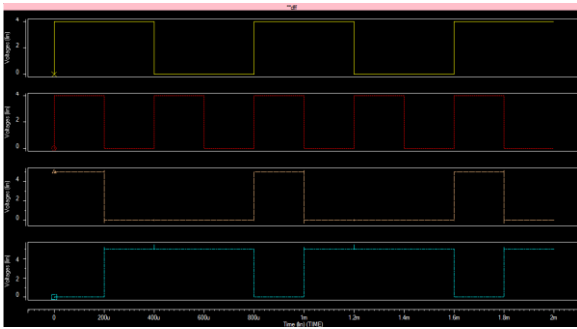


Figure 1.5(e): Simulation result of D-Flipflop using CMOS logic.

The first waveform in figure 1.5(e) is the clock to the D-Flipflop. The second waveform is its input ‘D’. The last two are outputs Q and  $\bar{Q}$  generated by the D-Flipflop. The simulation time is 2 ms and the average power obtained is 5.8285E-05 Watts.

f) D-Flip flop using Subthreshold Adiabatic logic:

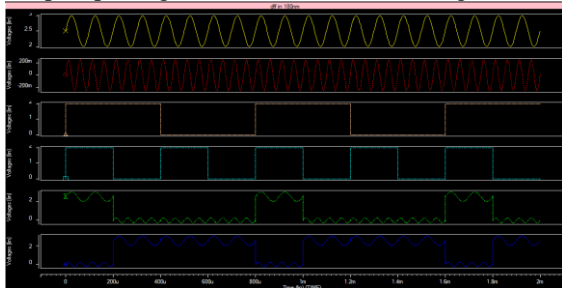


Figure 1.5(f): Simulation result of D-Flipflop using Subthreshold Adiabatic logic.

Similarly, the first two waveforms of figure 1.5(f) are the sine waves of 10 KHz and 20 KHz of 0.5V and 0.25V respectively. The next one is the clock to the D-Flipflop. The third pulse is the input ‘D’ to the D-Flipflop. The last two are the outputs Q and  $\bar{Q}$  generated by the D-Flipflop. The simulation time is 2 ms and the average power obtained is 3.2186E-05 Watts. It is evident from Table 1.2 we can infer

that the average power obtained using Subthreshold Adiabatic logic is less when distinguished with usual CMOS logic.

Table 1.2: Comparing the obtained average power of Digital Circuits

Digital circuits	Power dissipation		Energy dissipation (Joules)	Power saving
	CMOS logic (Watts)	Subthreshold Adiabatic logic (Watts)		
Half adder	8.4168E-05	4.5407E-05	9.0814×10 <sup>-8</sup> J	46.05%
Full adder	1.4075E-04	7.5174E-05	15.0348×10 <sup>-8</sup> J	46.50%
D flipflop	5.8285E-05	3.2186E-05	6.4372×10 <sup>-8</sup> J	44.77%

## V.CONCLUSION

The design of low power CMOS circuits using Two Phase Clocking Subthreshold Adiabatic Logic is implemented for digital circuits and the average power dissipated by them was compared. Adiabatic Logic units, digital circuits were designed in HSPICE using 0.18 μm CMOS standard process technology. It was found that the Two Phase Clocking Subthreshold Adiabatic Logic is beneficial for applications wherever power reduction is the most important criteria. It can also be used in digital low power applications such as sensors.

## REFERENCES

1. Kazunari Kato, Yasuhiro Takahashi, and Toshikazu Sekine “Two Phase Clocking Subthreshold Adiabatic Logic,” 2014 IEEE International Symposium on Circuits and Systems (ISCAS), pp. 598-601.
2. A.P.Chandrakasan, S.Sheng and R.W.Brodersen, “Low Power CMOS Digital Design,” IEEE Journal of Solid-state Circuits, vol.27, no.04, pp.473-484, April 1999.
3. J. M. Rabaey, A. Chandrakasan, and B. Nikolic, “Digital Integrated Circuits: A Design Perspective,” Pearson Education, NJ, 2002.
4. William C. Athas, Lars J. Svensson, Jeffrey G. Koller, Nestoras Tzartzanis, and Eric Ying-Chin Chou, “Low-Power Digital Systems Based on Adiabatic-switching Principles,” IEEE Transactions On Very Large Scale Integration (VLSI) Systems, vol. 2, no. 4, pp. 398-407, December 1994.
5. Nazrul Anuar, Yasuhiro Takahashi, and Toshikazu Sekine, “Two Phase Clocked Adiabatic Static CMOS Logic and its Logic family,” Journal of semiconductor technology and science, vol.10, no.1, March, 2010.
6. Saed G. Younis, “Asymptotically Zero Energy Computing Using Split-Level Charge Recovery Logic,” PhD thesis, June 1994.
7. Sanjay kumar, “Design of Low Power CMOS Cell Structures Based on Adiabatic Switching Principle,” Thapar University, January 2009.
8. Yibin Ye, Kaushik Roy, “Ultra Low Energy Computing Using Adiabatic Switching Principle,” ECE Technical Reports March 1995.
9. A.Kramer, J.S.Denker, B.Flower, J. Moroney, “Second order adiabatic computation with 2N-2P and 2N-2N2P Logic circuits”, AT&T Bell Laboratories.
10. Y. Moon, and D.K. Jeong, “An Efficient Charge Recovery Logic Circuit,” IEEE J. Solid-State Circuits., vol. 31, no. 4, pp. 514–522, April 1996.
11. D. Maksimovic, Vojin G. Oklobdzija, B. Nikolic, and K. W. Current, “Clocked CMOS Adiabatic Logic with Integrated Single-Phase Power clock Supply,” IEEE Trans. VLSI Syst., vol. 8, no. 4, pp. 460–463, August 2000.
12. M. Khatir, and A. Moradi, “Secure Adiabatic Logic: A low-energy DParesistant logic style,” Cryptology ePrint Archive, Report 2008/123, 2008.
13. Samik Samanta, “Study and Analysis of Two Partially Adiabatic Inverters (PADI),” International Journal of Computer Applications iC3S-2012, pp. 17-19.

# Energy Efficient Digital Circuits using Two Phase Clocking Sub-Threshold Adiabatic Logic

14. Robert H. Dennard, Liember, Fritz H. Gaensslen, Hwa-Nien Yu, V. Leo Rideout, Ernest Bassous, And Andre R. Leblanc, "Design of Ion-Implanted MOSFET'S with Very Small Physical Dimensions," January 2009.
15. N.H.E.Weste and D.M. Harris, "CMOS VLSI Design," A Circuits and Systems Perspective, Toronto: Addison-Wesley, 2011.
16. L. Schwiebert, S.Gupta and Wienmann, "Research Challenge in Wireless Networks of Biomedical Sensors," Mobile Computing and Networking, pp.151-165, 2001.
17. Hendrawan Soeleman and Kaushik Roy, "Ultra-Low Power Digital Subthreshold Logic Circuits".
18. C.S.Wallace "A Suggestion for a Fast Multiplier," IEEE Trans. Electron.Comput., vol. EC-13, no.1, pp. 14-17, 2001.
19. P .Samundiswary and K.Anitha, "Design and Analysis of CMOS Based DADDA Multiplier," IJCEM International Journal of Computational Engineering & Management, vol.16, no.6, pp.12-17, 2013.
20. Anju S and Saravanan, "High Performance Dadda Multiplier Implementation using High Speed Carry Select Adder," International Journal of Advanced Research in Computer and Communication Engineering, vol.2,no.3,pp.1572-1575, March 2013.
21. Praveen Kumar Duvvuru and Bharathi.M, "A High Speed Floating Point Multiplier using Vedic Mathematics," i-manager's Journal on Circuits and Systems, vol. 2, no.2, pp.1-9, March- May 2014.
22. Tony R. Kuphaldt, "Lessons In Electric Circuits," copyright (C) 2000-2010.
23. Samik Samanta, Rajat Mahapatra, Ashis Kumar Mal, "Efficient Energy Recovery Logic: Study and Implementation," International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, vol. 2, Issue 9, pp. 4317-4321, Sept., 2013.
24. Xubo Wang, Anh Dinh and Daniel Teng, "Radar Sensing Using Ultra Wide band - Design and Implementation," Wang et al., licensee InTech. pp.41-64.
25. J.S.Denker, "A Review of Adiabatic Computing," Technical Digest IEEE Symposium Low Power Electronics, San Diego, pp. 94-97, October 1994.
26. Synopsys HSPICE@ RF Manual X-2005.09.

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